TEK SERVICE MANUAL

Part No.: 070-6306-00
Product Group 26

2753P
SPECTRUM ANALYZER
VOLUME 1

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY AND SERVICE SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

Please Check for CHANGE INFORMATION at the Rear of This Manual

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Tektronix®
COMMITTED TO EXCELLENCE

Tektronix, Inc.
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Serial Number_____

PREFACE

This manual contains service information for the TEKTRONIX 2753P Spectrum Analyzer. The information is located in two volumes. Volume 1 contains the text and Volume 2 contains the diagrams and parts lists. The Table of Contents in each volume lists the contents of both volumes.

Manuals that describe other aspects of the product are:

- Operator's Manual
- Programmer's Manual

Who Should Use This Manual?

This manual is intended for electronic technicians with experience in servicing digital, analog, and rf circuitry. Circuit analysis is mostly functional and should help isolate most malfunctions to a board or block of circuitry. The technician should then be able, with the aid of test equipment, to isolate the malfunction to a specific component or components.

This instrument contains firmware that provides a thorough instrument check during power up and during operation, and if needed, guides the user through an abbreviated front-panel calibration procedure. If calibration cannot be achieved, a diagnostic test detects and isolates most problems to the system, such as 1st LO. The technician can then run troubleshooting diagnostics to further isolate the problem to the board or block of components. Refer to the Maintenance section for diagnostics information.

Documentation Standards

Most terminology and graphics follow ANSI standards. A glossary of terms is provided as an appendix. Refer to the following standards:

- ANSI Y1.1 — Abbreviations
- ANSI Y32.2 — Graphic Symbols
- IEEE 91 — Logic Symbols

Change/History Information

Sometimes instrument changes occur or manual errors are found that make some of the information in the manual inaccurate. When that happens, Manual Change Information notices are inserted at the rear of the manual. This helps ensure that the manual contains the latest and most accurate information available when the product is sold.

History information, with the updated data, is integrated into the text or diagrams. When a text page is updated, the revised pages are identified by a revision date in the lower inside corner of the page. When a diagram is updated, the revision date is placed at the lower center of the diagram. History information is shown with a gray tint. When a component value is changed, the designator on the drawing is boxed with a grey outline. When a circuit is deleted or changed, the original configuration is shown in grey, drawn either at its original location or to the side of the drawing.

If you have a manual other than the one that came with your instrument it may contain revisions that do not apply to your instrument; however all history information that pertains to the earlier instruments is retained. When a major modification has been made to an assembly or circuit board, the data for the replaced assembly will follow the new information and will be identified with appropriate titles or headings such as instrument serial number range or the assembly or board part numbers.

Also, if your instrument has an assembly replaced with a newer version, documentation for the newer assembly may be supplied. Contact any Tektronix Service Center for information.

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SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

Do Not Wear Jewelry

Remove jewelry prior to servicing. Rings, necklaces, and other metallic objects could come into contact with dangerous voltages and currents.

Use Care When Servicing With Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

X-Radiation

X-ray emission generated within this instrument has been sufficiently shielded. Do not modify or otherwise alter the high voltage circuitry or the crt enclosure.

TERMS

In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

In This Manual

This symbol indicates where applicable cautionary or other information is to be found.

As Marked on Equipment

DANGER — High Voltage.

Protective ground (earth) terminal.

ATTENTION — Refer to manual.

Refer to manual.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Danger Arising From Loss of Ground

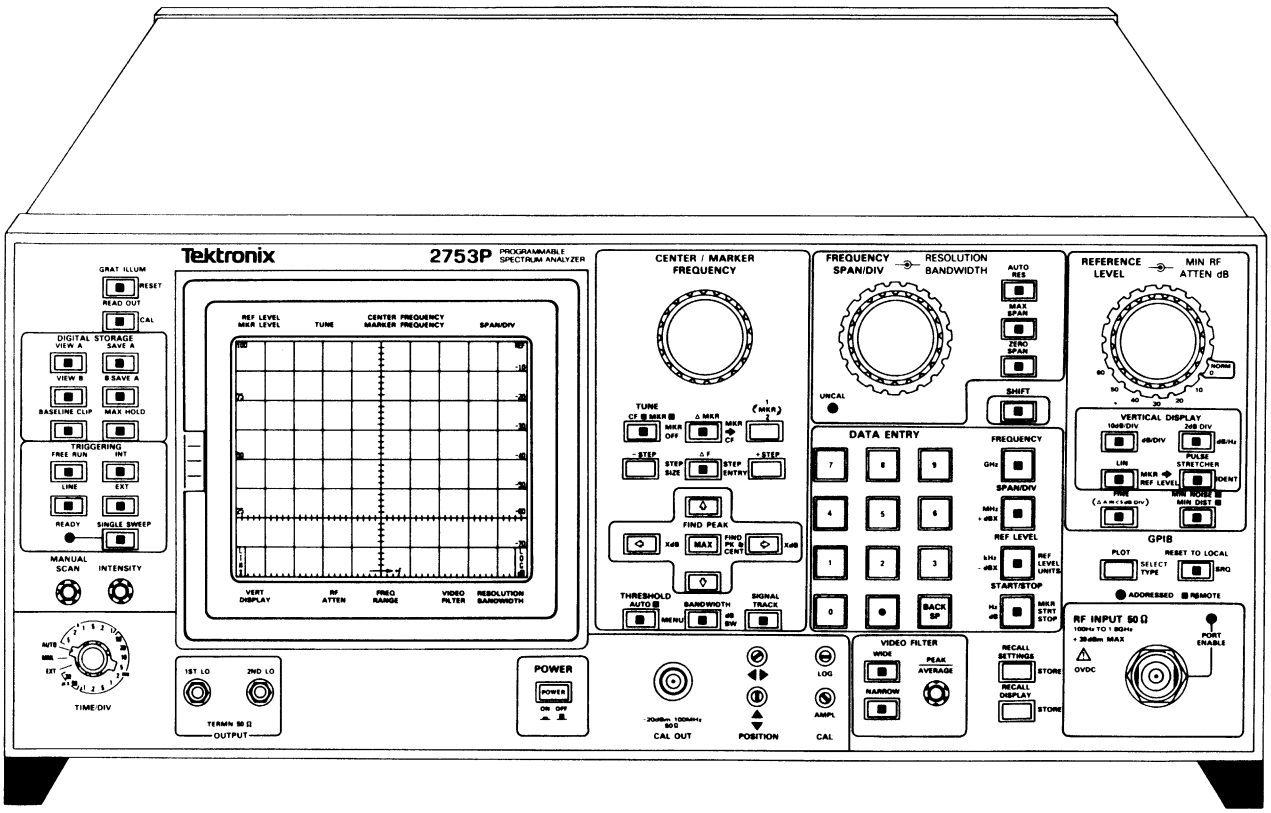
Upon loss of the protective ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Use the Proper Power Cord

Use only the power cord and connector specified for your product.

Use only a power cord that is in good condition.

For detailed information on power cords and connectors see Section 1.



The 2753P Spectrum Analyzer.

GENERAL INFORMATION

Product Description

The 2753P is a high performance, programmable laboratory spectrum analyzer. Microcomputer control of most functions simplifies and enhances operation.

The analyzer features:

- Single and delta marker modes
- Synthesizer frequency accuracy
- Precise amplitude measurement
- Digital storage display
- Battery-operated memory for front-panel settings and displays
- Diagnostic crt messages
- Keypad entry and menu selections

The frequency range is 100 Hz to 1.8 GHz. Resolution bandwidth is 30 Hz to 1 MHz. Digital storage provides flicker-free displays plus functions to compare and subtract displays, and save maximum values. In addition, up to nine separate displays with their readouts can be stored in battery-powered non-volatile memory, then later recalled for additional analysis and comparison. Up to ten different front-panel control setups can also be stored for future recall.

Select center frequency either by the front-panel tuning knob or by the Data Entry pushbuttons. When using the pushbuttons, it is not necessary to alter the Span/Div setting regardless of the frequency selected. Other parameters, such as vertical display and reference level, are also pushbutton selectable.

Marker functions provide direct readout of frequency and amplitude at any point along any displayed trace. Relative (delta) frequency and amplitude information between any two points along any displayed trace is also available. The tuning knob moves the markers, and it can also move the display with a stationary frequency marker. It is possible to fix the marker to a position on the display and use the knob to move both the spectrum and the marker at the same time. Refer to Using the Markers Feature in Section 6 of the Operators Manual.

The instrument can be controlled remotely via the General Purpose Interface Bus. Waveform processing functions are added to do some spectrum analysis locally. Refer to the Programmers Manual for additional information.

Conformance to Industry Standards

This spectrum analyzer complies with the following Industry Safety Standards and Regulatory Requirements:

Safety

CSA — Electrical Bulletin

FM — Electrical Utilization Standard Class 3820

ANSI C39.5 — Safety Requirements for Electrical and Electronic Measuring and Controlling Instrumentation.

IEC 348 (2nd edition) — Safety Requirements for Electronic Measuring Apparatus.

Regulatory

VDE 0871 Class B — Regulations for RFI Suppression of High Frequency Apparatus and Installations.

Product Service

To assure adequate product service and maintenance for our instruments, Tektronix has established Field Offices and Service Centers at strategic points throughout the United States and in countries where our products are sold. Several types of maintenance or repair agreements are available.

For example, for a fixed fee, a maintenance agreement program provides maintenance and recalibration on a regular basis. Tektronix will remind you when a product is due for recalibration and perform the service within a specified time.

Tektronix emergency repair service provides immediate service when the instrument is urgently needed.

Contact your local Tektronix Service Center, representative, or sales engineer for details regarding product service.

Instrument Construction

Modular construction provides ready access to the major circuits. Circuit boards containing sensitive circuits are either mounted on metal castings, each of which provides shielding between adjacent modules, or they are mounted within honeycomb-like castings, with feedthrough connectors through the compartment wall. All boards and assemblies plug onto a common interconnect board. Most adjustments and test points are accessible while the instrument is operational and with the modules or assemblies secured in their normal position.

Extenders are available in an optional Service Kit (see Maintenance section under Service Fixtures and Tools for Maintenance). Any module or board can be removed without disturbing the structural or functional integrity of the other modules. The extenders allow most circuit board assemblies to function in an extended position for service or adjustment. The circuit boards mounted on the metal casting can be removed by removing the securing screws. All other circuit boards (which should require minimal service) are accessible by removing a cover plate over the assembly or module.

NOTE

Disassembly of some modules may require special tools and procedures. These procedures are located in the Maintenance section.

Circuits are isolated in shielded compartments to obtain and maintain the frequency stability, sensitivity, and EMI characteristics. While shielding helps ensure spurious-free response, the closeness of the circuits minimizes losses and interactions with other functions. Compartments are enclosed on both sides by metal plates and interconnections between compartments are made by feedthrough terminals rather than cables. If the compartments are opened, be sure that the shields and covers are properly reinstalled before operating.

Installation and Preparation for Use

The Installation section of the manual provides unpacking information and the procedures to prepare the instrument for use. It also includes repackaging information.

Changing Power Input Range

The procedure for changing the input voltage range is described in the Installation section. Details on how to change the line fuse are also given.

The power cord that is supplied with the instrument and the instrument power voltage requirements depend on the available power source (see Specification section). Power cord options are described in the Options section.

Replacing Fuses

Refer to the Installation section for line fuse replacement and the Maintenance section for replacing the power supply fuses.

Selected Components

Some components are selected, matched, or preconditioned to meet Tektronix specifications. These components are shown in the parts list and may carry a Tektronix Part Number under the Mfr. Part Number column.

Selected value components are identified on the circuit diagram and in the parts list as a "SEL" value. The component description lists either the nominal value or a range of values. Selection criteria is included in the Maintenance section. Selection procedures are included in the Adjustment Procedure or Maintenance sections of the manual as needed.

Assembly and Circuit Numbering

Each assembly and subassembly are assigned assembly numbers. Generally, each component is assigned a circuit number according to its geographic location within an assembly. The Replaceable Electrical Parts list prefixes these circuit numbers with the corresponding assembly and subassembly numbers.

EXAMPLE: R2080 on assembly A20 becomes A20R2080.

EXAMPLE: U1044 on subassembly A1 of assembly A36 is found in the electrical parts list as A36A1U1044.

Power-up Messages

During the power-up cycle, the firmware version appears on the screen for a short time. Also, when a diagnostic routine fails, a message comes on screen describing the error and what can be done to bypass the problem if it can not be immediately corrected.

Options

The Options section of this manual contains detailed information on all the options currently available for the spectrum analyzer.

Accessories

Both service manuals are optional accessories. Their part numbers are 070-6306-00 for Service Volume 1, and 070-6307-00 for Service Volume 2. The Replaceable Mechanical Parts list in the Service Manual, Volume 2, contains the part numbers, descriptions, and ordering information for all standard and optional accessories offered for the spectrum analyzer at this time.

The following list includes all standard accessories currently shipped with each instrument.

- 72 inch, 50Ω coaxial cable (n to n connector)
- 18 inch, 50Ω coaxial cable (bnc to bnc connector)
- Adapter (n male to bnc female)
- 4A fast-blow fuse (2 each)[1]
- Power cord
- Cord clamp
- Amber crt light filter
- Grey crt light filter
- Crt mesh filter
- Rear Connector Shield
- Operators Manual
- Programmers Manual

[1]If the instrument is wired for 220-240 V operation (Options A1, A2, A3, A4, A5) or if Option 52 is installed (North American configuration for 230 V with standard power cord), 2A slow-blow fuses are used.

SPECIFICATION

This section includes the electrical, physical, and environmental characteristics of this instrument. Any instrument specification changes due to options are listed in the Options section of this manual.

ELECTRICAL CHARACTERISTICS

The following tables of electrical characteristics and features apply to the Spectrum Analyzer after a 30-minute warmup and after doing the front-panel CAL adjustments, except as noted. The Performance Requirement statements define characteristics that are essential to the intended application of the product. Performance Requirement characteristics are normally verifiable by following the Performance Check procedure in this manual. The Supplemental Information column provides more explanation about related Performance Requirements, or describes typical performance for characteristics not ordinarily verified by the Performance Check procedure.

The instrument performs an internal processor system check each time power is turned on. The Functional Or Operational Check procedure, which does not require external test equipment or technical expertise, is provided in the Operators manual. This procedure will satisfy most incoming inspections and will help familiarize you with the instrument capabilities.

Verification of Tolerance Values

Perform compliance tests of specified limits, listed in the Performance Requirement column, only after a 30-minute warm-up time (except as noted) and after doing the front-panel CAL procedure. Use measurement instruments that do not affect the values measured. Measurement tolerance of test equipment should be negligible when compared to the specified tolerance and when not negligible, add the error of the measuring device to the specified tolerance.

Table 2-1
FREQUENCY RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Center/Marker Frequency Operating Range		100 Hz to 1.8 GHz Tuned by the CENTER/MARKER FREQUENCY control or the DATA ENTRY keypad.
Accuracy (After front-panel CAL has been performed)		Center/Marker Frequency Accuracy is specified by two characteristics: ● initial accuracy (Firmware corrected) ● center frequency drift during the sweep
Initial (start of sweep) SPAN/DIV >200 kHz (1st LO unlocked)	±{20%D + (F × 10^{-5}) + 15 kHz} Where: D = SPAN/DIV or RESOLUTION BANDWIDTH, whichever is greater F = Center or Marker Frequency	Allow a settling time of one second for each GHz change in F within a band. Over operating temperature range (F × 1.5 × 10^{-5})
SPAN/DIV ≤200 kHz (1st LO locked)	±{20%D + (F × 10^{-5}) + 15 Hz} Where: D = SPAN/DIV or RESOLUTION BANDWIDTH, whichever is greater F = Center or Marker Frequency	Over operating temperature range (F × 1.5 × 10^{-5})
Center Frequency Drift		With constant ambient temperature and fixed center frequency. Any error is observed during sweep time. Correction will occur at the end of sweep or as often as necessary to maintain specifications.
After 30 minute warmup SPAN/DIV >200 kHz (1st LO unlocked)		≤25 kHz per minute of sweep time.
SPAN/DIV ≤200 kHz (1st LO locked)		≤150 Hz per minute of sweep time.
After 1 hour warmup SPAN/DIV >200 kHz (1st LO unlocked)		≤5 kHz per minute of sweep time. Not significant when compared to residual FM per minute of sweep time.
SPAN/DIV ≤200 kHz (1st LO locked)	≤50 Hz per minute	

Table 2-1 (Continued)
FREQUENCY RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Readout Resolution		⩽ 10% of SPAN/DIV to minimum of 1 kHz. 100 Hz in delta mode.
Residual FM		Short term, after 1 hour warmup.
SPAN/DIV >200 kHz (1st LO unlocked)	⩽7 kHz total excursion in 20 ms.	
SPAN/DIV ⩽200 kHz (1st LO locked)	⩽10 Hz total excursion in 20 ms.	
Resolution Bandwidth (6 dB down)	Within 20% of selected bandwidth.	30 Hz, then 100 Hz to 1 MHz in decade steps.
Shape Factor (60 dB/6 dB) 30 Hz Bandwidth All other bandwidths	 12:1 or less 7.5:1 or less	
Noise Sidebands Resolution Bandwidths ⩽ 100 Hz Resolution Bandwidths ⩾ 1 kHz	 ⩽−70 dBc ⩽−75 dBc	 Measured at an offset of 30 × the resolution bandwidth
Marker(s)		When activated, the marker is a bright dot positioned by the CENTER/MARKER FREQUENCY control or the DATA ENTRY keypad.
Normal Accuracy	Identical to center frequency accuracy	For the active trace
Δ MKR Accuracy	±1% of the total span	For the active trace. 5% on stored displays. ΔMKR activates a second marker at the position of the single marker on the trace. Parentheses appear on the marker display line indicating that the delta mode is active. The display shows the difference in frequency and amplitude. 1←MKR→2 selects which marker is tuned.
Δ MKR Resolution		⩽ 10% of Span/Div
Frequency Span/Div Overall Range With SPAN/DIV control		 20 Hz to 100 MHz (in a 1-2-5 sequence)
With the DATA ENTRY keypad.		20 Hz to 170 MHz (to two significant digits) In addition, MAX SPAN sweeps across an entire band and ZERO SPAN provides a 0 Hz display.
Accuracy/Linearity		Measured over the center 8 divisions.
SPAN/DIV ⩾ 50 Hz	Within 5% of the selected Span/Div	
SPAN/DIV @ 20 Hz	Within 10% of the selected Span/Div	

Table 2-2
AMPLITUDE RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Vertical Display Modes		10 dB/Div, 2 dB/Div, and Linear. Any integer between 1–15 dB/Div can also be selected via the DATA ENTRY keypad.
Display Dynamic Range		80 dB maximum for Log Mode. 8 divisions for Linear Mode.
Display Amplitude Accuracy		
10 dB/DIV Mode	±1.0 dB/10 dB to a maximum cumulative error of ±2.0 dB over 80 dB range	
2 dB/DIV Mode	±0.4 dB/2.0 dB to a maximum cumulative error of ±1.0 dB over 16 dB range	
LIN Mode	±5% of full scale	
Marker/s Accuracy		Identical to REF LEVEL accuracy plus cumulative error of display scale (Dependent on vertical position)
Reference Level		Top of the graticule.
Range		
Log Mode		From −117 dBm to +40 dBm; +40 dBm includes 10 dB of IF gain reduction (+30 dBm is the maximum safe input). Alternate reference levels are: ●dBV (−130 dBV to +27 dBV) ●dBmV (−70 dBmV to +87 dBmV) ●dBμV (−10 dBμV to +147 dBμV)
LIN Mode		39.6 nV/Div to 2.8 V/Div (1W maximum safe input)
Steps		
10 dB/DIV Mode		10 dB for the coarse mode. 1 dB for the FINE mode.
2 dB/DIV Mode		1 dB for the coarse mode. 0.25 dB for the FINE mode.
LIN Mode		1-2-5 sequence for coarse mode. 1 dB equivalent steps for FINE mode.
Set via DATA ENTRY Keypad		Steps correspond to the display mode in coarse, except for 2 dB/DIV where steps are 1 dB. In FINE mode: 1 dB when the mode is 5 dB/Div or more 0.25 dB for display modes of 4 dB/Div or less (referred to as ΔA mode)

Table 2-2 (Continued)
AMPLITUDE RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Reference Level (Continued) Accuracy		Dependent on the following characteristics: ●RF Attenuation Accuracy ●IF Gain Accuracy ●Resolution Bandwidth ●Frequency Response ●<SHIFT> CAL routine reduces error between resolution bandwidths at −20 dBm REF LEVEL. Other REF LEVELs may have larger errors. ●Temperature variation (±0.15 dB/°C maximum)
RF Attenuator Range		0–60 dB in 10 dB steps
Accuracy Dc to 1.8 GHz	Within 0.5 dB/10 dB to a maximum of 1 dB over the 60 dB range	
IF Gain Range		87 dB of gain increase, 10 dB of gain decrease (MIN NOISE activated), in 10 dB and 1 dB steps.
Accuracy 1 dB Step	⩽ 0.2 dB/dB step to 0.5 dB/9 dB steps except at the decade transitions.	
Decade Transitions −19 to −20 dBm −29 to −30 dBm −39 to −40 dBm −49 to −50 dBm −59 to −60 dBm	0.5 dB or less	Maximum 1 dB cumulative error over 10 dB.
Maximum Deviation over the 97 dB Range	±2 dB	
Gain Variation Between Resolution Bandwidths		Measurement conditions: ●Measured at −20 dBm. Other reference levels may have larger errors. ●MIN DISTORTION mode ●After CAL routine
With respect to 1 MHz Filter	±0.4 dB (after CAL routine)	
Between Any Two Filters	⩽0.8 dB	

Table 2-2 (Continued)
AMPLITUDE RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Frequency Response About the midpoint between two extremes	±1.0 dB	Measured with 10 dB RF Attenuation. Response is affected by: ● input VSWR ● gain variation
Video Filter Narrow		Reduces video bandwidth to approximately 1/300th of the selected resolution bandwidth and 1/100th for 30 Hz bandwidth
Wide		Reduces video bandwidth to approximately 1/30th or the selected resolution bandwidth and 1/10th for the 30 Hz resolution bandwidth
Pulse Stretcher Fall-Time		30 μs/div of pulse amplitude.
Differential Amplitude Measurement		ΔA mode provides differential measurements in 0.25 dB increments. (This is not related to the ΔMKR mode.)
Range		Maximum range of 57.75 dB dependent of Reference Level when ΔA mode is activated.
Accuracy		**Difference** / **Steps** / **Error** 0.25 dB / 1 / 0.15 dB 2 dB / 8 / 0.4 dB 10 dB / 40 / 1.0 dB 20-57.75 dB / 80-231 / 2.0 dB

Table 2-2 (Continued)
AMPLITUDE RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Sensitivity		Equivalent maximum input noise for each resolution bandwidth. Measured with: ● 0 dB RF attenuation ● Narrow Video Filter ● 2 dB/Div Log mode ● Digital Storage on ● Max Hold off ● Peak/Average in Average ● 1 sec Time/Div ● Zero Span ● Input terminated in 50Ω
30 Hz	−130 dBm	
100 Hz	−125 dBm	
1 kHz	−115 dBm	
10 kHz	−105 dBm	
100 kHz	−95 dBm	
1 MHz	−85 dBm	
Spurious Responses		
Residual	−100 dBm or less	No input signal, referenced to the internal mixer input.
3rd Order Intermodulation Products	−70 dBc or less	From any two on-screen signals within any frequency span. In MIN DISTORTION mode.
Zero Frequency Spur	−24 dBm or less	Referenced to input with 0 dB attenuation, terminated into 50 and into open circuit. Measured at 25°C.
Harmonic Distortion	−60 dBc or less	Measured across entire band With −30 dBm input and 0 dB attenuation.
LO Emission	−70 dBm or less	With 0 dB RF Attenuation.

Table 2-3
INPUT SIGNAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
RF INPUT		Type N female connector. (See Option 07 in the Options section for supplemental specifications concerning an additional 75 Ω input.)
Impedance		50 Ω
VSWR with RF Attenuation ≥10 dB		1.3:1 (typically 1.2:1)
VSWR with 0 dB RF Attenuation		2.0:1 (typically 1.9:1)
Maximum Safe Input (With 0 dB RF Attenuation)		+30 dBm (1W) continuous or 75W peak, pulse width of 1 μs or less with a maximum duty factor of 0.001 (attenator limit). DO NOT APPLY DC VOLTAGE TO THE RF INPUT.
1 dB Compression Point (Minimum) In Min Distortion mode In Min Noise mode	 −20 dBm −10 dBm	With no RF attenuation. Measured at 10 MHz IF Output.
HORIZ|TRIG		Dc coupled input for external horizontal drive (selected by the EXT position of the TIME/DIV control) and ac coupled input for external trigger signals (selected at other positions of the TIME/DIV control).
Sweep Input Voltage Range		0 to +10V (dc + peak ac) for full screen deflection
Trigger Input Voltage Range Minimum	At least 1.0 V peak from 15 Hz to 500 kHz	Typically 1.0 MHz at 1.5V peak.
Maximum dc + peak ac		50V
ac		$30V_{rms}$ to 10 kHz, then derate linearly to $3.5V_{rms}$ at 100 kHz and above.
Pulse Width		0.1 μs minimum

Table 2-3 (Continued)
INPUT SIGNAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
MARKER/VIDEO		External Video input or External Video Marker input, switched by pin 1 of the ACCESSORIES connector.
MARKER Input Level		0 to −10V Interfaces with TEKTRONIX 1405 Sideband Adapter.
VIDEO Input Level		0 to +4 V for full screen display with pin 1 of the ACCESSORIES connector low
ACCESSORY Connector (J104)		25-pin connector (Not RS-232 compatible) Provides bi-directional access to the instrument bus. Also provides external Video select. All lines are TTL compatible. Maximum voltage on all lines is ±15V.
Pin 1		External Video Select Low selects External VIDEO Input. High (default) selects Video MARKER Input.
Pin 2		Not used.
Pin 3		Not used.
Pin 4		Internal Control. High (default) selects internal control. Instrument bus lines are output at the ACCESSORIES connector. Low selects External control. Instrument bus lines at the ACCESSORIES connector accept input from an external controller.
Pin 5		Chassis Ground
Pins 6–13[a]		Instrument Bus Address lines 7–0[a]
Pin14[a]		Instrument Bus Data Valid signal[a]
Pin 15[a]		Instrument Bus Service Request signal[a]
Pin 16[a]		Instrument Bus Poll signal[a]
Pin 17		Data Bus Enable input signal for external controller. High (unasserted) disables external data bus. Low enables external data bus.
Pins 18–25		Instrument Bus Data lines 0–7 Active when External Data Bus Enable (pin 17) is low.

Table 2-4
OUTPUT SIGNAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Calibrator (CAL OUT)	−20 dBm ±0.3 dB at 100 MHz	100 MHz comb of markers provide amplitude calibration at 100 MHz. ±15 PPM over temperature range.
1st LO and 2nd LO OUTPUTs		Provide access to the output of the respective local oscillators. THESE PORTS MUST BE TERMINATED IN 50 Ω AT ALL TIMES.
1st LO OUTPUT Power		+6 dBm to +15 dBm
2nd LO OUTPUT Power		−10 dBm to +15 dBm.
VERT Output		Provides 0.5V ±5% (open circuit) of signal per division of video that is above and below the centerline. Full range −2.0V to +2.0V. Source impedance is approximately 1kΩ.
HORIZ Output		Provides 0.5V/Div (open circuit) either side of center. Full range −2.5V to +2.5V. 250mV Max ripple. Source impedance is approximately 1kΩ.
PEN LIFT		TTL compatible, nominal +5V to lift plotter pen.
10 MHz IF Output		Output level is approximately −5 dBm for a full screen signal at −30 dBm reference level. Nominal impedance is approximately 50Ω.
IEEE STD 488 PORT		In accordance with IEEE 488-78 standard and Tektronix Codes and Formats standard (version 81.1). Implemented as SH1, AH1, T5, L3, SR1, RL1, PP1, DC1, DT1, and C0.
PROBE POWER Outputs Pin 1		Provides operating voltages for active probes. +5V at 100 mA maximum
Pin 2		Ground
Pin 3		−15V at 100 mA maximum
Pin 4		+15V at 100 mA maximum
ACCESSORIES (J104)		All inputs and outputs are listed in Table 2-3 Input Characteristics.

[a]Output when internally controlled (pin 4 high) and input when externally controlled (pin 4 low).

Table 2-5
GENERAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Sweep		Triggered, auto, manual, and external
Sweep Time	20 μs/Div to 5 s/Div in 1-2-5 sequence (10 s/Div available in AUTO)	
Accuracy	±5% over center 8 divisions	
Triggering		INTERNAL, EXTERNAL, FREE RUN, and LINE.
Internal Trigger Level	2 divisions or more of signal	
EXTERNAL Trigger Input Level	1.0V peak, minimum	EXTERNAL is ac-coupled (15 Hz—1 MHz). Maximum external trigger input is 50V (dc + peak ac).
Crt Readout		Displays all parameters listed on the crt bezel, plus operating messages.
Battery-Powered Memory		Instrument settings, displays, and calibration offsets are stored in battery-powered non-volatile RAM.
Battery Life At +55°C Ambient Temperature		1–2 years
At +25°C Ambient Temperature Lithium (Standard)		At least 5 years
Temperature Range for Retaining Data Operating		0°C to +50°C
Non-Operating		−30°C to +75°C

Table 2-6
POWER REQUIREMENTS

Characteristic	Performance Requirement	Supplemental Information
Line Frequency Range	47–63 Hz	47 Hz to 440 Hz. Operation over 63 Hz exceeds protective grounding conductor leakage current of 3.5 mA. A redundant protective grounding means is essential to protect against electric shock.
Line Voltage Range	90 V_{ac} to 132 V_{ac}	115 V nominal
	180 V_{ac} to 250 V_{ac}	230 V nominal
Line Fuse 115V Nominal		4A
230V Nominal		2A Medium-Blow
Input Power	210 W maximum (3.2A)	At 115V and 60 Hz
Leakage Current		5 mA maximum

Table 2-7
ENVIRONMENTAL CHARACTERISTICS

Meets MIL T-28800C, type III class 5, style E specifications as follows.

Characteristic	Description	
Temperature		
Operating	0°C to +50°C	
Non-operating[a]	−40°C to +75°C	
Humidity		
Operating	95% ±5% below +30°C. 75% ±5% above +30°C. 45% ±5% above +40°C.	
Altitude		
Operating	10,000 feet (3050 meters)	
Non-operating	40,000 feet (12000 meters)	
Vibration, Operating (instrument secured to a vibration platform during test)	MIL-Std-810, Method 514 Procedure I (modified). Resonant searches along all three axes at 0.013 inch displacement, for 15 minutes. Dwell for an additional 10 minutes in each axis at the frequency of the major resonance or at 33 Hz if none was found. Resonance is defined as twice the input displacement. Total vibration time is 75 minutes.	
Shock (Operating and Non-operating)	Three 30g, one-half sine, guillotine-type shocks, 11 ms duration in each direction along each major axis; total of 18 shocks.	
Electromagnetic Interference (EMI)	Meets requirements described in MIL-Std-461B Part 4, except as noted.	
	Test Method	**Remarks**
Conducted Emissions	CE01—60 Hz to 15 kHz	1 kHz to 15 kHz only
	CE03—15 kHz to 50 MHz power leads	15 kHz to 50 kHz, relaxed by 15 dB
Conducted Susceptibility	CS01—30 Hz to 50 kHz power leads	Full limits
	CS02—50 kHz to 400 MHz power leads	Full limits
	CS06—spike power leads	Full limits
Radiated Emissions	RE01—30 Hz to 50 kHz magnetic field (measured at 30 cm).	30 — 36 kHz exceptioned.
	RE02—14 kHz to 10 GHz	Full limit

[a]After storage at temperatures below −15°C, the instrument may not reset when power is first turned on. If this happens, allow the instrument to warm up for at least 15 minutes, then turn POWER OFF for 5 seconds and back ON.

Table 2-7 (Continued)
ENVIRONMENTAL CHARACTERISTICS

Characteristic	Description	
Electromagnetic Interference (EMI) (Continued)	Meets requirements described in MIL-Std-461B Part 4, except as noted.	
	Test Method	**Remarks**
Radiated Susceptibility	RS01—30 Hz to 50 kHz	Full limit
	RS02—Magnetic Induction	To 5 A only, 60 Hz
	RS03—14 kHz to 10 GHz	Up to 1 GHz, 1 V/m

Table 2-8
PHYSICAL CHARACTERISTICS

Characteristic	Description
Weight	60 lbs (27 kg), including standard accessories, except manuals.
Dimensions	6.97 × 16.88 × 25.00 inches (17.7 × 43.1 × 63.5 cm)

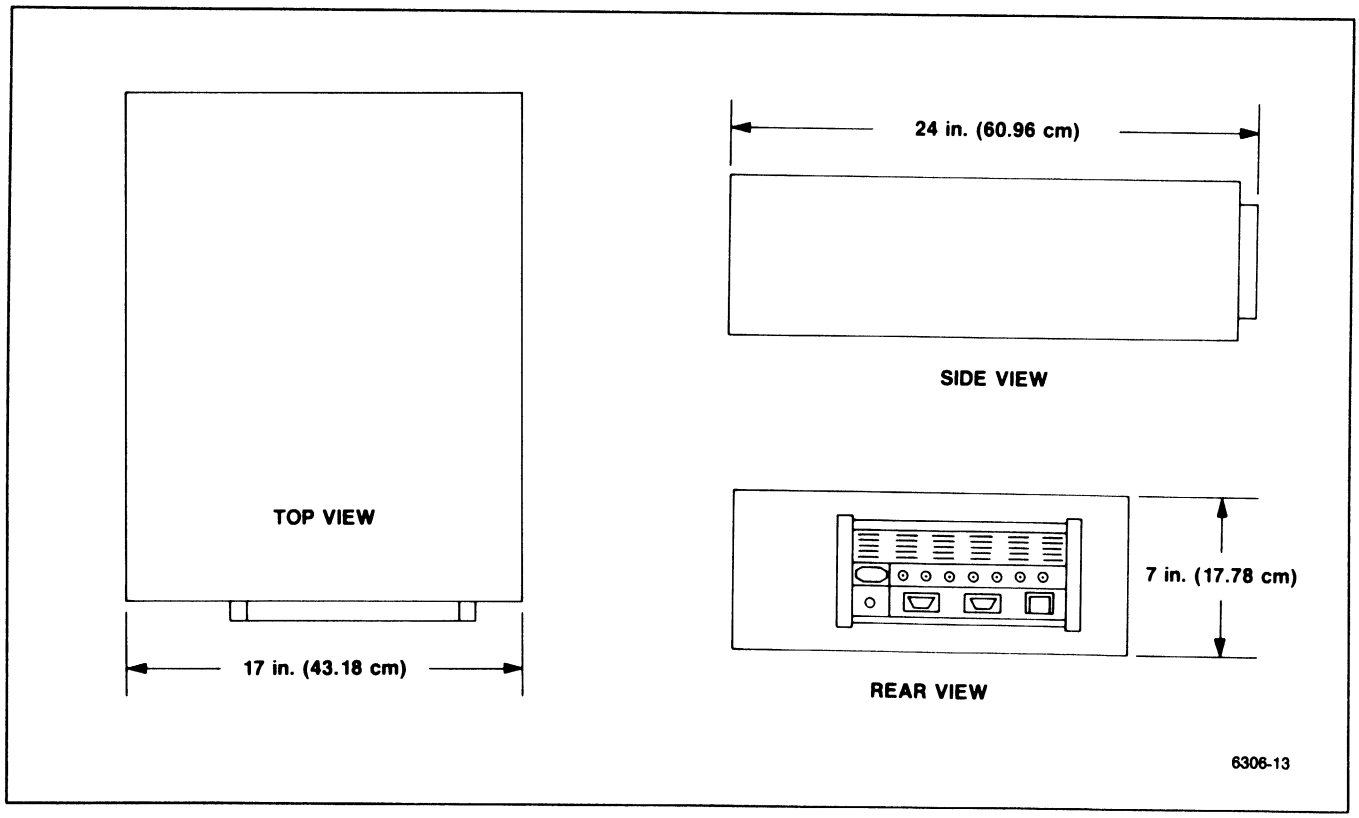


Figure 2-1. Dimensions.

INSTALLATION

This section describes unpacking, installation, power requirements, storage information and repackaging for the spectrum analyzer.

UNPACKING AND INITIAL INSPECTION

Before unpacking the spectrum analyzer, inspect the shipping container for signs of external damage. If the container is damaged, notify the carrier as well as Tektronix, Inc. The shipping container contains the basic instrument and its standard accessories. For a list of the standard accessories, refer to Section 1 of this manual (or, for ordering information, refer to the list following the Replaceable Mechanical Parts list in the Service Manual, Volume 2).

If the contents of the shipping container are incomplete, if there is mechanical damage or defect, or if the instrument does not meet operational check requirements, contact your local Tektronix Field Office or representative.

Keep the shipping container if the instrument is to be stored or shipped to Tektronix for service or repair. Refer to Storage and Repackaging for Shipment later in this section.

The instrument was inspected both mechanically and electrically before shipment, and it should be free of mechanical damage and meet or exceed all electrical specifications. The Operation section of the Operators Manual contains procedures to check functional or operational performance. Perform the functional check procedure to verify that the instrument is operating properly. This check is intended to satisfy the requirements for most receiving or incoming inspections. (A detailed electrical performance verification procedure in the Performance Check section of this manual provides a check of all specified performance requirements, as listed in the Specification section.)

The instrument can be operated in any position that allows air flow in the bottom and out the rear of the instrument. Feet on the four corners allow ample clearance even if the instrument is stacked with other instruments. The air is drawn in by a fan through the bottom and expelled out the back. Avoid locating the instrument where paper, plastic, or any other material might block the air intake.

The spectrum analyzer is equipped with a flipstand to adjust the viewing angle.

WARNING

Removing or replacing the cabinet on the instrument can be hazardous. Only qualified service personnel should attempt to remove the instrument cabinet.

CONNECTING POWER

Power Source and Power Requirements

WARNING

Changing the power input can be dangerous.

- Work safely
- Know the intended power source
- Set the instrument for the power source
- Check the fuse for proper ratings
- Use the power cord and plug intended for the power source

The spectrum analyzer operates from a single-phase power source that has one of its current-carrying conductors (neutral) at ground (earth) potential. Do not operate the spectrum analyzer from power sources where both current-carrying conductors are isolated or above ground potential (such as phase-to-phase on a multi-phase system or across the legs of a 110-220 V single-phase, three-wire system). In this method of operation, only the line conductor has over-current (fuse) protection within the unit. Refer to the Safety Summary at the front of this manual.

The ac power connector is a three-wire, polarized plug with the ground (earth) lead connected directly to the instrument frame to provide electrical shock protection. If the unit is connected to any other power source, connect the unit frame to an earth ground.

Operate the spectrum analyzer from either 115 Vac or 230 Vac nominal line voltage with a range of 90 to 132 or 180 to 250 Vac, at 48 to 440 Hz. Power and voltage requirements are printed on a back-panel plate mounted below the power input jack.

Input power requirements are changed with a switch on the back panel (see Figure 3-1) and by replacing the input line fuse. The instrument uses a 4A fast blow fuse for 115 Vac operation, and a 2A slow blow fuse for 230 Vac operation.

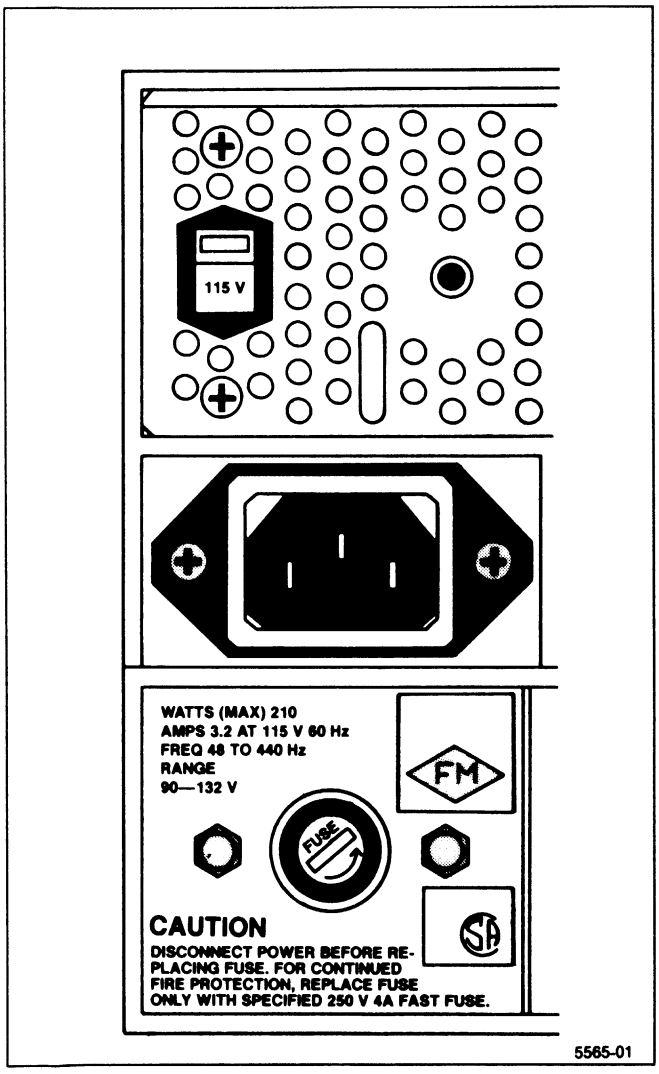


Figure 3-1. Input power selector switch and fuse.

Remove the protective cover and set the line select switch for the appropriate voltage range.

Remove the fuse holder and replace the line fuse with the appropriate fuse for the voltage range selected.

The international power cord and plug configuration is shown in the Options section of this manual.

STORAGE AND REPACKAGING

Storage

Short Term (less than 90 days) — For short term storage, store the instrument in an environment that meets the non-operating environmental specifications in Section 2 of this manual.

Long Term — For instrument storage of more than 90 days, retain the shipping container to repackage the instrument. The battery in the instrument does not require removal. Package the instrument in a vapor barrier bag with a drying agent and store in a location that meets the non-operating environmental specifications in Section 2 of this manual.

If you have any questions, contact your local Tektronix Field Office or representative.

Repackaging for Shipment

When the spectrum analyzer is to be shipped to a Tektronix Service Center for service or repair, attach a tag that shows the owner and address, the name of the individual at your firm that can be contacted, the complete instrument serial number, and a description of the service required. If the original package is unfit for use or not available, use the following repackaging information.

1. To allow for cushioning, use a corrugated cardboard container with a test strength of 375 pounds (140 kilograms) and inside dimensions that are at least six inches more than the equipment dimensions (refer to the Physical Characteristics in Section 2).

2. Install the instrument front cover, and surround the instrument with plastic sheeting to protect the finish.

3. Cushion the equipment on all sides with packing material or plastic foam.

4. Seal the container with shipping tape or an industrial, heavy-duty stapler.

PERFORMANCE CHECK

Introduction

All performance checks are carried out without removing the instrument covers.

The procedures in this section verify that the instrument performance satisfies the performance requirements specified under the Performance Requirement column in Section 2, Specification.

Some parameters and instrument functions that are not explicitly specified are also checked. These checks verify that the instrument performs as described.

Checks should be performed in sequence because some tests rely on the satisfactory performance of related circuits. Also, the check steps have been arranged so that the changing of test equipment setups from one step to the next is minimized.

If a measurement is marginal or below specification, an adjustment procedure to enhance performance will be found, under a similar heading, in Section 5, Adjustment Procedure. After adjustment, recheck the performance. Adjust only those circuits that do not meet performance criteria.

If adjustment fails to return the circuit to specified performance, refer to the Maintenance section for troubleshooting and repair procedures.

Incoming Inspection Test

The Operators manual contains an operational or functional check that checks all functions. This check is recommended for incoming inspections because it requires no external equipment or special expertise and is a reliable indication that the instrument is performing properly.

Option Instrument Checks

Whenever practical, performance checks for option instruments are integrated in the performance check steps for the standard instrument, otherwise special check steps are provided under OPTION INSTRUMENTS towards the back of this section.

Verification of Tolerance Values

Compliance tests, of those limits listed in the Performance Requirement column of the instrument specifications, shall be performed after sufficient warm-up time and completion of preliminary preparation steps (such as front-panel adjustments).

Measurement tolerance of test equipment should be negligible in comparison to the specified tolerance; and, when not negligible, the error of the measuring apparatus shall be added to the tolerance specified.

History Information

The instrument and manual are periodically evaluated and updated. If modifications require changes in the procedures, information applicable to earlier instruments will be included within a step or as a sub-part to a step.

Equipment Required

Table 4-1 lists the test equipment and calibration fixtures recommended for the Performance Check. This equipment is also applicable for the adjustment procedures in Section 5, Adjustment Procedure. The equipment characteristics specified are the minimum required for the checks. Substitute equipment must meet or exceed these characteristics. These fixtures are available from Tektronix, Inc., and may be ordered through your local Tektronix Field Office or representative.

Some checks may not be practical because they may require sophisticated test equipment and/or procedures. In those cases, a compromise may be made in the procedures. When that occurs, a statement or footnote to that fact is added to the step. The more exact method of measuring the characteristic can be supplied by your Tektronix Service Center.

Table 4-1
EQUIPMENT REQUIRED

Test Equipment	Desired Characteristics	Recommendation and Use
Test Oscilloscope	Vertical sensitivity, 50 mV/Div to 5 V/Div; Bandwidth, DC to 100 MHz	Any TEKTRONIX 7000-Series oscilloscope with plug-in units for real-time display such as 7A16A/7B50A, and P6106A 10X Probe
Time Mark Generator	Marker output, 5 s to 20 ns; accuracy 0.001%	TEKTRONIX TG 501 with TM 500-Series Power Module (time/div and span accuracy check)
Frequency Counter	0 to 200 MHz, 1 Hz resolution, 25 mV sensitivity.	TEKTRONIX DC 510 with TM 500-Series Power Module (Calibrator frequency measurement)
Prescaler	Compatible with TEKTRONIX DC 510	TEKTRONIX DP 501 with TM 500-Series Power Module (Center frequency measurement, external reference input power)
Function or Sine-Wave Generator	1 Hz to 1 MHz; 0 to 20 V p-p	TEKTRONIX FG 503 Function Generator (external trigger and horizontal input requirements check)
Signal Generator	10 Hz to 10 MHz, constant output	Hewlett-Packard Model 654A or Model 3336C (frequency response check)
Signal Generator	Two leveled generators, 500 kHz to 2.0 GHz. Output, −100 dBm to +10 dBm; spectral purity 60 dB or more below the fundamental.	TEKTRONIX SG 504, Hewlett-Packard Model 8640A/B and Model 8614A generators (IM, display accuracy, and triggering checks)
Low Loss (WL Gore) RF Cable	Flat to at least 1.8 GHz	Tektronix Part No. 006-7609-00 (used to check frequency response)
Crystal Detector	0.01—1.8 GHz	Hewlett-Packard Model 8473C (frequency response check)
Sweep Oscillator	0.01 to 1.8 GHz; frequency response, ±1.0 dB	Hewlett-Packard Model 8350B with Model 83595A Option 002 Plug-in (Frequency response and RF attenuator checks)
Power Divider	Dc to 1.8 GHz	Weinschel Model 1579B
Power Meter with Power Sensor	−30 dBm to +20 dBm full scale; 100 kHz to 4 GHz	Hewlett-Packard Model 435B or 436A with 8482A Power Sensor (LO emission check)
Low-Pass Filter	Must have rolloff of 40 dB or more at 200 MHz	Texscan or Lark
UHF Comb Generator	Provide comb line to 18 MHz; accuracy 0.01%	TEKTRONIX Calibration Fixture 067-0885-00 with TM 500 Power Module (frequency readout accuracy check)
Spectrum Analyzer	Frequency range, 50 kHz to 2.2 GHz	TEKTRONIX 2755, 494, or 7L14 Option 39 (compression point and Option 42 checks)
Impedance Matching Power Divider	Dc to 1000 MHz	TEKTRONIX 067-1232-00 (Option 07 frequency response)

Table 4-1 (cont)
EQUIPMENT REQUIRED

Test Equipment	Desired Characteristics	Recommendation and Use
Tracking Generator	Frequency range, 100 kHz to 1.8 GHz	TEKTRONIX TR502 (Option 42 check)
1 dB Step Attenuator[a]	0 dB to 10 dB in 1 dB steps ±0.1 dB from dc to 1.8 GHz	Hewlett Packard 8494B (input compression check)
10 dB Step Attenuator[a]	0 dB to 110 dB in 10 dB steps ±0.7 dB from dc to 1.8 GHz	Hewlett Packard 8496B (input compression check)
10 dB Step Attenuator	0 dB to 120 dB in 10 dB steps ±1.5 dB at 1 GHz to 90 dB	Hewlett Packard 355D (dynamic range check)
Step Attenuator	Range, 0 dB — 12 dB, in 1 dB steps; dc — 1 GHz, accuracy ±0.25 dB to 0.5 GHz	Hewlett Packard 355C (input compression check)
50Ω Terminator		Tektronix Part No. 011-0049-01
10 dB/50Ω Attenuator	dc to 1.8 GHz; ±1 dB accuracy	Hewlett Packard 33340A Option 10 (RF attenuator accuracy check)
20 dB/50Ω Attenuator	dc to 1.8 GHz; ±1 dB accuracy	Hewlett Packard 33340A Option 20 (RF attenuator accuracy check)
2 N Male to APC 3.5 Male Adapters		Maury Model 8023D (RF attenuator accuracy check)
APC 3.5 Male to APC 3.5 Male Adapter		Maury Model 8021B2 (RF attenuator accuracy check)
APC 3.5 Female to APC 3.5 Female Adapter		Maury Model 8021D1 (RF attenuator accuracy check)
Attenuator (SMA Connectors)	3 dB, 50Ω; dc to 1.8 GHz	Weinschel Model 4M. Tektronix Part No. 015-1053-00
Two Attenuators (bnc connectors)	20 dB, 50Ω; dc to 2.0 GHz	Tektronix Part No. 011-0059-02
(50Ω Coaxial Cable with sma connectors)	5 ns	Tektronix Part No. 015-1006-00
N Male to SMA Male Adapter		Tektronix Part No. 015-0369-00
N Male to BNC Female Adapter		Tektronix Part No. 103-0045-00
BNC T Adapter		Tektronix Part No. 103-0030-00
Two 50Ω Coaxial Cables		Tektronix Part No. 015-1006-00
75/50Ω Barrel Connector		Tektronix Part No. 103-0254-00

PRELIMINARY PREPARATION

During initial power-up cycle, the instrument type, instrument operating system processor firmware version, and the front panel processor firmware versions are displayed on the crt for approximately two seconds. The Replaceable Electrical Parts List in Service manual Volume 2 lists the ROMs used for each version. The service manual also lists the firmware operating notes associated with each firmware version.

If the microcomputer detects a hardware failure, a failure report will come on screen and remain for about 2 seconds. A status message will then appear and remain for the duration of the failure. Press <SHIFT> . (decimal point) to bring error messages to the screen.

[a] The 10 dB step attenuator, 1 dB step attenuator, and interconnect kit must be calibrated together as a single unit, using precision standard attenuators such as Weinschel Model AS-6 attenuator.

a. Connect the spectrum analyzer power cord to an appropriate power source (refer to Power Source and Power Requirements in Section 3, Installation) and switch POWER on.

b. When POWER is switched on, the input PORT ENABLE indicator (a green LED) should come on.

c. The microprocessor runs a memory and I/O test. If no processor system problems are found, the power-up program will complete in approximately 10 seconds, and the instrument will be ready to operate. After the power-up routine, the crt will initialize as shown in Figure 4-1.

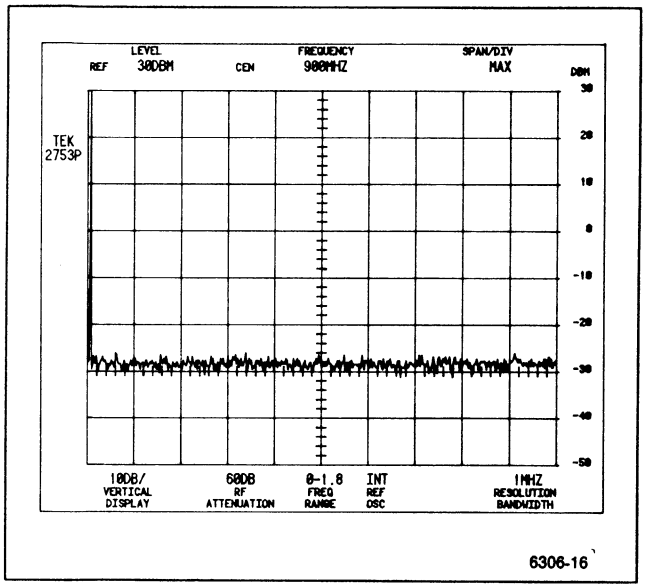


Figure 4-1. Crt display at initial power-up.

d. The operating functions and modes should initialize to the following state:

Readout	On
REF LEVEL	30DBM
CENTER FREQUENCY	900MHZ
MARKER FREQUENCY	0MHZ
SPAN/DIV	MAX
VERT DISPLAY	10DB/
RF ATTEN	60DB
FREQ RANGE	0—1.8
RESOLUTION BANDWIDTH	1MHZ
Readout	On
TRIGGERING	FREE RUN
AUTO RES	On
DIGITAL STORAGE	VIEW A & VIEW B on
THRESHOLD	AUTO
All other pushbuttons	Inactive or off

e. Set the MIN RF ATTEN dB control to 0 (NORM) and the PEAK/AVERAGE control fully counterclockwise. Set the TIME/DIV control to AUTO, REF LEVEL to read −20DBM, and adjust the INTENSITY control for the desired brightness. Note that the RF ATTEN readout is now 10DB.

f. Apply the CAL OUT signal to the RF INPUT through a 50Ω cable.

g. A dot marker will appear in the upper portion of the screen in the MAX frequency mode. This marker indicates the location on the display to which the spectrum analyzer frequency is tuned. With a frequency readout of 0MHZ, the marker will be in the upper left portion of the screen. Rotate the CENTER/MARKER FREQUENCY control and watch the dot marker move across the display. Notice that the CENTER FREQUENCY readout (top line) remains at 900 MHz, and that the MARKER FREQUENCY readout (second line) changes according to the position of the marker (dot).

h. Harmonics of the 100 MHz calibrator signal will be displayed as shown in Figure 4-2. To select 100 MHz center frequency, press the pushbutton sequence of FREQUENCY 100 MHz.

i. To change the SPAN/DIV to 100 MHz, press the pushbutton sequence of SPAN/DIV 100 MHz. The dot marker is now horizontally centered, and the 100 MHz calibrator signal is at center screen.

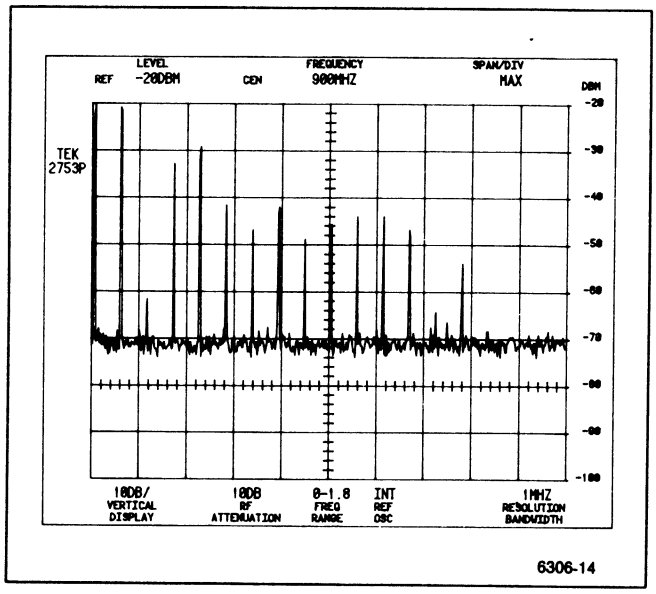


Figure 4-2. Typical display of calibrator signal in Max Span/Div.

Calibrate Position, Center/Marker Frequency, Reference Level, and Dynamic Range

NOTE

When <SHIFT> CAL is pressed, the microcomputer performs a center frequency and reference level calibration. Prompts appear on the screen to guide the user step-by-step through the procedure.

This calibration should be done at regular intervals so the instrument can meet its center frequency and reference level accuracy performance specifications. It should also be done each time the ambient temperature of the instrument is changed.

To observe the results after the microcomputer has completed a calibration routine, press the <SHIFT> 1 sequence. A message will appear on the screen that shows the correction factor used by the microcomputer to center the resolution bandwidth filters to produce a calibrated center frequency. It also shows the correction that was required to bring the amplitude level within 0.4 dB of the 1 MHz filter.

Press the <SHIFT> CAL sequence to start the calibration routine. A prompt message on the screen will guide you through setting the four front-panel adjustments of vertical and horizontal POSITION, and AMPL and LOG CAL. This sets the absolute reference level for the 1 MHz resolution bandwidth filter. An automatic calibration is then done, which measures and corrects for absolute frequency and amplitude (relative to 1 MHz) errors of the filters. This takes approximately 60 seconds. If a message appears on the screen, refer to Error Message Readout earlier in this section. The correction factors are held in memory. Press FINE to continue calibration as instructed or <SHIFT> to exit the routine.

If any amplitude correction factor, at room temperature, for a filter is greater than 1 dB, the filter in the VR assembly should be readjusted. Refer to Section 5, Adjustment Procedure.

PERFORMANCE CHECK PROCEDURE

1. Check Center/Marker Frequency Accuracy

This is a two part procedure; Part I checks center/marker frequency accuracy with the 1st LO unlocked, Part II checks accuracy with the 1st LO phase locked. A front panel CAL should be done before performing this check.

In Option 05 instruments check the reference oscillator accuracy first. A procedure for this check is provided at the end of this section.

Part I – 1st LO not Phase Locked

Accuracy with 1st LO unlocked is ±{(20% of the Span/Div or Resolution Bandwidth, whichever is greater) + (CF × 10^{-5}) + 15 kHz}. In Option 05 instruments, accuracy with 1st LO unlocked is ±{(20% of the Span/Div or Resolution Bandwidth, whichever is greater) + (CF × Reference Frequency Error) + 15 kHz}

a. Use a Frequency Counter and a Prescaler to measure the fundamental output frequency of the Comb Generator (Comb Generator source output excluding the Comb Generator Module).

b. Make a note of the measured frequency, which is approximately 500 MHz. This is the fundamental frequency referred to in Table 4-2, and will be used to determine each center frequency checked.

c. Connect the test equipment as shown in Figure 4-3.

d. Set the Spectrum Analyzer controls as follows:

REF LEVEL	−10 dB
SPAN/DIV	210 kHz
AUTO RES	On
VERTICAL DISPLAY	10 dB/DIV
MIN RF ATTEN dB	0
PEAK/AVERAGE	Fully Clockwise
TIME/DIV	AUTO

e. Use the Data Entry keypad to set the FREQUENCY to the fundamental frequency noted in part b (rounded off to the nearest kHz).

f. Check that the displayed signal is within 0.295 divisions (62 kHz) of center screen.

g. Continue checking frequencies using the data in Table 4-2. Here is an example:

Check Center/Marker Frequency Accuracy at 1.5 GHz

Fundamental = 499.99831 MHz.

Determine Center/Marker Frequency to the nearest kHz:

Fundamental × 3 (from Table 4-2)

0.499998 GHz × 3 = 1.499994 GHz

Use Data Entry keypad to set FREQUENCY to 1.499994 GHz.

Check that the displayed signal is within 0.343 divisions (72 kHz) of center screen.

NOTE

If a particular check should fail, measure the fundamental frequency and recheck.

Part II – 1st LO Phase Locked

Accuracy with 1st LO phase-locked is ±{(20% of the Span/Div or Resolution Bandwidth, whichever is greater) + (CF × 10^{-5}) + 15 Hz}. In Option 05 instruments, accuracy with 1st LO phase-locked is ±{(20% of the Span/Div or Resolution Bandwidth, whichever is greater) + (CF × Reference Frequency Error) + 15 Hz}.

NOTE

The frequency counter must be clocked by an external reference standard.

a. Apply the CAL OUT signal to the RF INPUT.

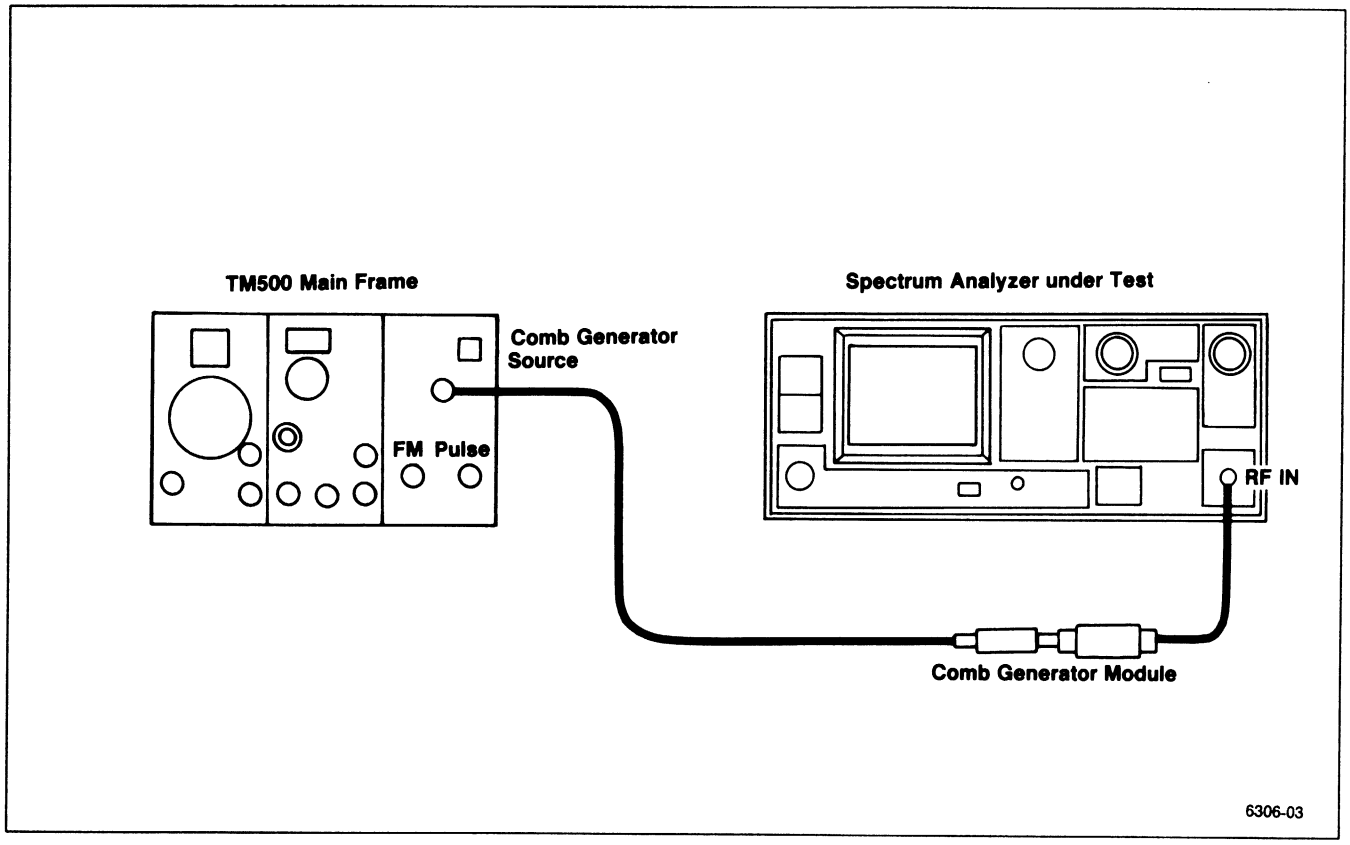


Figure 4-3. Test equipment setup for checking center/marker frequency accuracy.

Table 4-2
CENTER/MARKER FREQUENCY ACCURACY CHECK POINTS
(1st LO UNLOCKED)

Approximate Frequency	Keypad Entry CENTER FREQUENCY	Frequency Span/Div	Maximum Error
0.5 GHz	Fundamental	210 kHz	±0.295 (±62 kHz)
1.0 GHz	Fundamental × 2	210 kHz	±0.319 (±67 kHz)
1.5 GHz	Fundamental × 3	210 kHz	±0.343 (±72 kHz)

b. Set the Spectrum Analyzer controls as follows:

CENTER/MARKER FREQUENCY	100 MHz
REF LEVEL	−20 dBm
MIN RF ATTEN dB	0
SPAN/DIV	50 Hz
TIME/DIV	AUTO
VERTICAL DISPLAY	2 dB/DIV
AUTO RES	On
TRIGGERING	FREE RUN

c. Reset the REFERENCE LEVEL to bring the top of the signal below the dot marker.

d. Check 100 MHz center/marker frequency accuracy by measuring the deviation of the 100 MHz signal from the dot marker. Error must not exceed ±{(20% of the span/div) + 15 Hz} or ±25 Hz. The factor (CF × 10^{-5}) is cancelled when the CAL OUT signal is used.

e. Repeat this procedure to check the center/marker frequency accuracy to 1.8 GHz in 100 MHz increments. Reset the REF LEVEL as necessary to observe the comb of 100 MHz markers at the upper end of the range.

Check Δ marker accuracy.

a. Set the Spectrum Analyzer controls as follows:

CENTER/MARKER FREQUENCY	0.60 GHz
SPAN/DIV	100 MHz
AUTO RES	On
REF LEVEL	−20 dBm
VERTICAL DISPLAY	10 dB/DIV
TIME/DIV	AUTO
TRIGGERING	FREE RUN

b. Enable Δ markers by pressing Δ MKR, and tune one marker to the peak of a harmonic of the calibrator signal. Press MKR 1↔MKR 2, and tune the second marker to another harmonic peak of the calibrator signal.

c. Check that the Δ marker frequency readout is within 1% of the indicated span between the markers.

2. Check Center Frequency Stability

{Drift is 50 Hz/min or less with 1st LO locked (SPAN/DIV≤200 kHz) after 1 hour of warmup time in a stable ambient temperature}.

a. Apply the Calibrator signal to the RF INPUT.

b. Set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	100 MHz
SPAN/DIV	50 Hz
RESOLUTION BANDWIDTH	30 Hz
REF LEVEL	−23 dBm
RF ATTEN	0 dB
VERTICAL DISPLAY	2 dB/DIV
TRIGGERING	FREE RUN
VIEW A and VIEW B	On
TIME/DIV	AUTO

c. Set the CENTER FREQUENCY control such that one side of the signal intersects the sixth graticule line, from the left edge, then activate SINGLE SWEEP. Activate SAVE A to save the display.

d. Select the NARROW Video Filter, and press SINGLE SWEEP again to start the sweep. The sweep will now run at a 10 s/div rate.

e. Note the frequency difference between the two displays, at the 6th graticule line as (Δ F).

f. Check that the frequency drift is no more than 50 Hz per minute.

3. Check Residual FM

(Within 7 kHz over 20 ms with SPAN/DIV greater than 200 kHz, and within 10 Hz over 20 ms with FREQ SPAN/DIV of 200 kHz or less)

a. Apply the Calibrator signal to the RF INPUT.

b. Set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	100 MHz
SPAN/DIV	1 MHz
RESOLUTION BANDWIDTH	1 MHz
VERTICAL DISPLAY	2 dB/DIV
MIN RF ATTEN dB	0
REF LEVEL	−23 dBm
TIME/DIV	AUTO
TRIGGERING	FREE RUN
VIEW A and VIEW B	On

c. Disable the 1st LO synthesis and phase lock by pressing <SHIFT> 7. A message "FREQUENCY CORRECTIONS DISABLED: PRESS 7" will be displayed on the CRT.

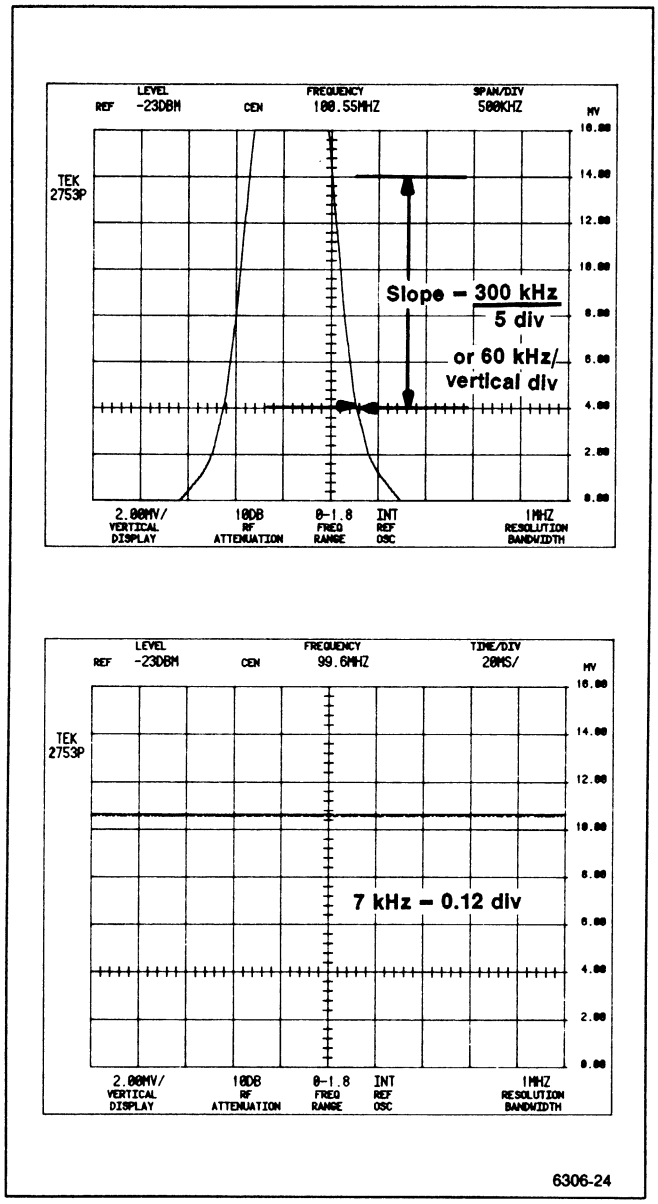


Figure 4-4. Typical display for measuring residual FM.

d. Reset the SPAN/DIV to 500 kHz, and recenter the 100 MHz calibrator signal on screen with the CENTER/MARKER FREQUENCY control.

e. Set the VERTICAL DISPLAY to LIN. Position the signal so the slope (horizontal versus vertical excursion) of the response can be determined as illustrated in Figure 4-4A. Slope determination may be made easier by switching VIEW B off, and using SINGLE SWEEP and SAVE A to freeze the display at a convenient position on the graticule.

f. If SAVE A was used in part d, de-activate SAVE A and reactivate VIEW B. Activate ZERO SPAN, set TIME/DIV to 20 ms, and set CENTER FREQUENCY control to position the display near center screen as shown in Figure 4-4B. Use SAVE A to freeze the display for ease in measuring FM. The peak-to-peak amplitude of the display (number of vertical divisions) within any given horizontal division, is the FM. Residual FM must not exceed 7 kHz for 20 ms.

g. Press <SHIFT> 7 to re-enable the phase lock, then set the FREQUENCY to 100 MHz and switch the TIME/DIV to AUTO. Reduce the FREQ SPAN/DIV to 20 Hz and RESOLUTION BANDWIDTH to 30 Hz.

h. Tune the CENTER FREQUENCY control to position the signal so its slope can be determined. Slope determination may be made easier by switching VIEW B off, and using SINGLE SWEEP and SAVE A to freeze the display at a convenient position on the graticule.

i. Deactivate SAVE A and SINGLE SWEEP and switch the TIME/DIV to 20 ms. Activate ZERO SPAN and position the display near center screen so the vertical excursions per horizontal division (20 ms) can be measured. Residual FM must not exceed 10 Hz within any one horizontal division.

4. Check Frequency Span/Div Accuracy

(±5% of the selected span/div over the center 8 divisions of a 10 division display with SPAN/DIV setting ⩾50 Hz; within 10% of the selected span/div with SPAN/DIV setting @ 20 Hz)

Span accuracy is checked by noting the displacement of calibrated markers from their respective graticule lines over the center eight divisions of the screen.

FREQUENCY SPAN/DIV range is 20 Hz to 100 MHz, in a 1–2–5 sequence when selected via the SPAN/DIV control, or up to 170 MHz when selected via the Data Entry keyboard.

a. Set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	1 GHz
SPAN/DIV	100 MHz
RESOLUTION BANDWIDTH	AUTO
REF LEVEL	−30 dBm
TIME/DIV	AUTO
VERTICAL DISPLAY	10 dB/DIV

b. Apply the CAL OUT signal to the RF INPUT and set the CENTER FREQUENCY to align the 100 MHz markers so the 100 MHz/div accuracy can be measured over the center eight divisions of the display. It may be necessary to change the REF LEVEL to obtain adequate marker amplitude. Maximum deviation (see Figure 4-5) must not exceed 5 MHz/div.

c. Remove the CAL OUT signal from the RF INPUT and connect the output of a Time Mark Generator to the RF INPUT. Set the CENTER FREQUENCY to 300 MHz, SPAN/DIV to 50 MHz, REF LEVEL to 20 dBm, and apply 20 ns time markers from the Time Mark Generator.

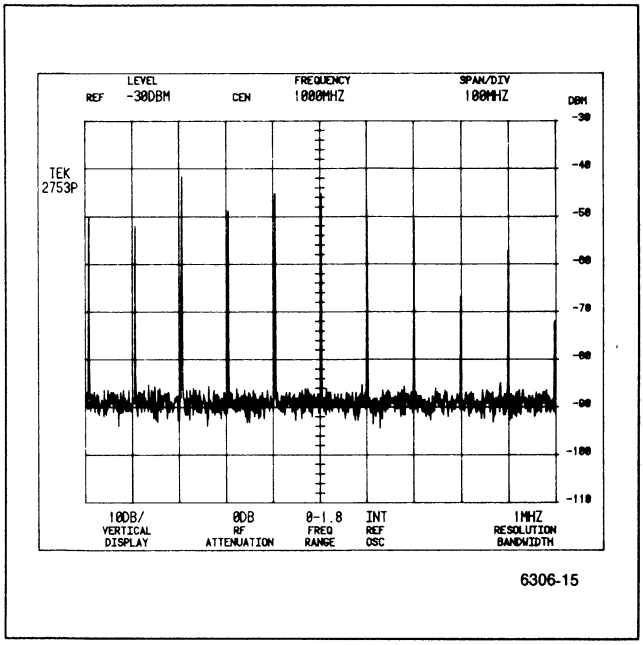


Figure 4-5. Typical marker display for measuring Span/Div accuracy.

d. Reset the REF LEVEL for the best marker definition, and the CENTER FREQUENCY to align the markers so accuracy can be checked for the 50 MHz span/div setting.

e. Set the CENTER FREQUENCY to 100 MHz, reduce the SPAN/DIV to 20 MHz, and apply 50 ns (20 MHz) markers.

f. Check the 20 MHz SPAN/DIV accuracy.

g. Repeat the procedure and check the SPAN/DIV accuracy from 10 MHz down to 10 kHz. Use Table 4-3 as a guide to relate time markers to SPAN/DIV settings. Increase the REF LEVEL as each setting is checked to maintain marker amplitude.

h. Set the CENTER FREQUENCY to 30 kHz and REF LEVEL as needed. Active the WIDE VIDEO FILTER. Repeat the above procedure to check the 5 kHz to 20 Hz SPAN/DIV selections.

5. Check Sweep Time Accuracy

(Within 5% over the center 8 divisions)

a. Connect the output of the Time Mark Generator to the rear-panel MARKER/VIDEO input. Connect pin 1 of J104 ACCESSORY connector to ground (connect pin 1 to pin 5).

Table 4-3
SPAN/DIV VERSUS TIME MARKERS FOR SPAN/DIV ACCURACY CHECK

FREQUENCY SPAN/DIV	Time Mark Generator Marker Output
20 MHz	50 ns
10 MHz	.1 μs
5 MHz	.2 μs
2 MHz	.5 μs
1 MHz	1 μs
500 kHz	2 μs
200 kHz	5 μs
100 kHz	10 μs
50 kHz	20 μs
20 kHz	50 μs
10 kHz	.1 ms
5 kHz	.2 ms
2 kHz	.5 ms
1 kHz	1 ms
500 Hz	2 ms
200 Hz	5 ms
100 Hz	10 ms
50 Hz	20 ms
20 Hz	20 ms

b. Set the Spectrum Analyzer TIME/DIV to 20 μs, and activate ZERO SPAN and INT TRIGGERING.

NOTE

Disable digital storage for sweep times faster than 2 ms.

c. Set the Time Mark Generator controls for 20 μs time marks.

d. Use the horizontal POSITION control to align a marker on the 1st graticule line (see Figure 4-6), then check the displacement of markers from their respective positions over the center eight divisions. Individual marker displacement must not exceed 5% or 2 minor divisions.

e. Check the accuracy of the 20 μs to 5 s TIME/DIV settings by applying appropriate markers for each TIME/DIV setting and noting the displacement as described in part d of this step.

f. Disconnect the test equipment, and the shorting strap from pin 1 of J104 ACCESSORY connector.

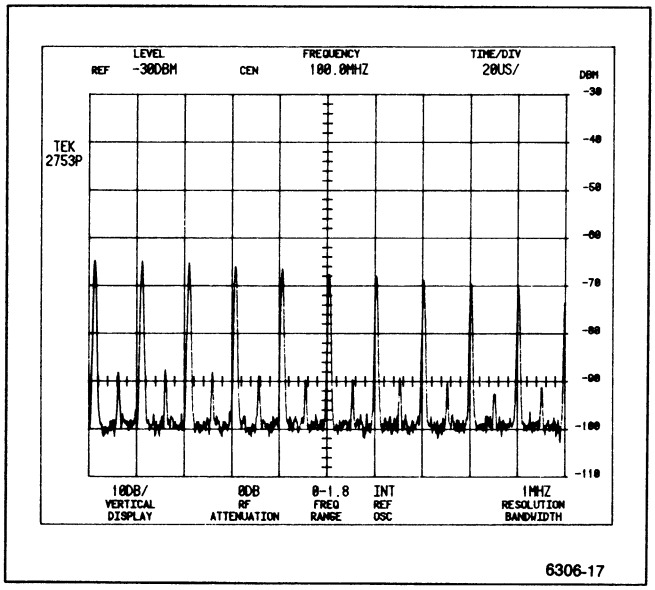


Figure 4-6. Typical display for measuring Time/Div accuracy.

6. Check Pulse Stretcher

(not a performance requirement)

a. Apply .1 ms time marks from the Time Mark Generator to the RF INPUT. Set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	2.0 MHz
ZERO SPAN	On
RESOLUTION BANDWIDTH	100 kHz
VERTICAL DISPLAY	10 dB/DIV
REF LEVEL	0 dBm
TIME/DIV	.1 ms
VIEW A and VIEW B	Off
TRIGGERING	INT

b. Activate PULSE STRETCHER and note that this mode extends the fall time of the markers.

c. Remove the test equipment.

7. Check Resolution Bandwidth and Shape Factor

(6 dB bandwidth within 20% of the selected bandwidth; shape factor is 7.5:1 or less for all bandwidths other than the 30 Hz bandwidth which is 12:1 or less)

NOTE

In Option 07 instruments the 100 kHz filter has been replaced by a 300 kHz filter.

a. Apply the CAL OUT signal to the RF INPUT. Set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	100 MHz
SPAN/DIV	500 kHz
RESOLUTION BANDWIDTH	1 MHz
VERTICAL DISPLAY	2 dB/DIV
REF LEVEL	−20 dBm
MIN NOISE	Activated
PEAK/AVERAGE	Fully Clockwise
TIME/DIV	AUTO
TRIGGERING	FREE RUN

b. Measure the 6 dB down bandwidth (see Figure 4-7A). Bandwidth should equal 1 MHz ±200 kHz.

c. Reset the VERTICAL DISPLAY to 10 dB/DIV and measure the 60 dB down bandwidth (see Figure 4-7B).

d. Check that the shape factor is 7.5:1 or less. The shape factor is the ratio of −60 dB/−6 dB bandwidths (see Figure 4-7).

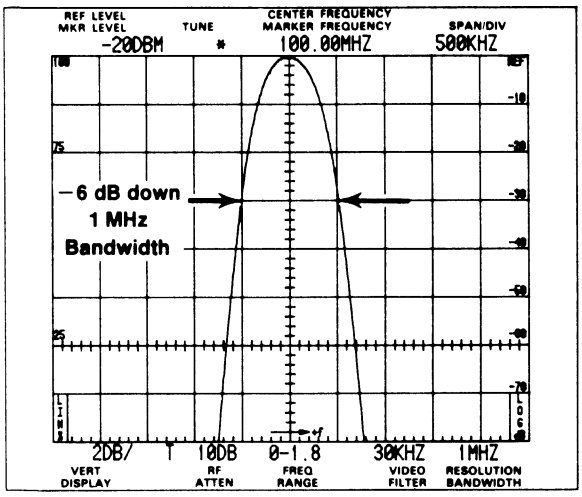
e. Reset the RESOLUTION BANDWIDTH to 100 kHz, SPAN/DIV to 100 kHz, and VERTICAL DISPLAY to 2 dB/DIV.

f. Check the resolution bandwidth and shape factor of the 100 kHz filter by repeating parts b through d.

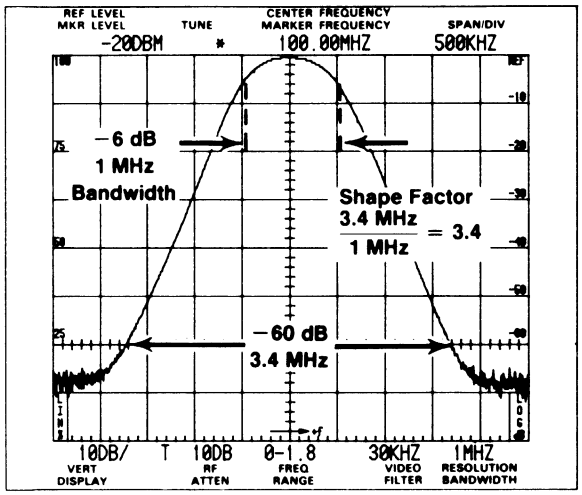
g. Check the resolution bandwidths and shape factors for the 10 kHz, 1 kHz, and 100 Hz filters. Shape factor should be 7.5:1 or less.

h. Reset the RESOLUTION BANDWIDTH to 30 Hz, SPAN/DIV to 50 Hz, and VERTICAL DISPLAY to 2 dB/DIV.

i. Check the resolution bandwidth and shape factor of the 30 Hz filter. Shape factor should be 12:1 or less.



A. Measuring 6dB down bandwidth.



B. Measuring 60dB down bandwidth and computing shape factor.

5562-18

Figure 4-7. Typical display for measuring bandwidth and shape factor.

8. Check Calibrator Output

(−20 dBm ±0.3 dB at 100 MHz)

a. Apply a 100 MHz signal to the power meter through a 3 dB attenuator and a 50Ω cable. Set the generator output level for a reading of −20 dBm on the power meter.

b. Disconnect the power meter from the signal generator, and connect the reference signal established in part a to the RF INPUT, through the same 50Ω cable and 3 dB attenuator.

c. Set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	100 MHz
SPAN/DIV	100 kHz
RESOLUTION BANDWIDTH	1 MHz
REF LEVEL	−18 dBm
VERTICAL DISPLAY	2 dB/DIV
TIME/DIV	AUTO
PEAK/AVERAGE	Fully Clockwise

d. Set the spectrum analyzer VERTICAL DISPLAY factor to the Δ A mode by pressing FINE. Set the REF LEVEL such that the top of the signal is on a graticule line near the top of the crt. Reset the REF LEVEL to 0.00 dB by pressing FINE twice. Store the display by activating SAVE A.

e. Remove the reference signal from the RF INPUT and connect the CAL OUT signal in its place using the same cable that was used in part b of this step.

f. Activate VIEW B and VIEW A.

g. Check that the amplitude difference between the VIEW B and SAVE A displays (CAL OUT signal and the reference) does not exceed 0.3 dB.

9. Check Noise Sidebands

(−70 dBc or more at 30 times the 100 Hz and 30 Hz resolution bandwidths, and −75 dBc or more for all other resolution bandwidths)

a. Apply the CAL OUT signal to the RF INPUT. Set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	100 MHz
SPAN/DIV	10 kHz
AUTO RES	On
REF LEVEL	−40 dBm
VERTICAL DISPLAY	10 dB/DIV
TIME/DIV	AUTO
WIDE VIDEO FILTER	On

b. Check that the amplitude of the noise sidebands are 55 dB or more down from the reference level at 30 times the resolution bandwidth (3 divisions away from the center frequency position). See Figure 4-8.

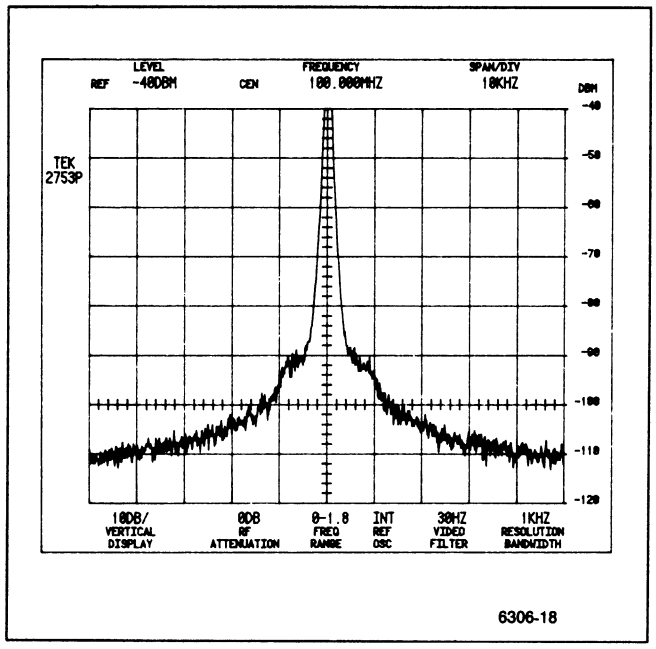


Figure 4-8. Typical display for measuring noise sidebands.

c. Decrease the SPAN/DIV to 1 kHz. RESOLUTION BANDWIDTH should go to 100 Hz.

d. Check that the amplitude of the noise sidebands 3 kHz away from the center frequency position is at least 70 dB below the signal level or 50 dB below the top of the screen.

e. Use the Data Entry keypad to reset the SPAN/DIV to 300 Hz. Set the RESOLUTION BANDWIDTH to 30 Hz.

f. Check that the amplitude of the noise sidebands 900 Hz away from the center frequency position is at least 70 dB below the signal level or 50 dB below the top of the screen.

10. Check Frequency Response

(Response, about the midpoint between two extremes, measured with 10 dB of RF attenuation is ±1.0 dB)

If the instrument is a rackmount version with semi-rigid cables to the rear panel (Option 31), frequency response may degrade at the high end of the frequency range.

a. Check frequency response from 0.01 GHz to 1.8 GHz.

(1) Connect the CAL OUT signal to the RF INPUT, and perform the <SHIFT> CAL routine.

(2) Set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	500 MHz
SPAN/DIV	100 MHz
RESOLUTION	1 MHz
REF LEVEL	−20 dBm
VERTICAL DISPLAY	1 dB/DIV
MIN RF ATTEN dB	0
TIME/DIV	AUTO
PEAK/AVERAGE	Fully ccw

(3) Connect the test equipment as shown in Figure 4-9.

(4) Set the sweep oscillator controls for a cw output with an amplitude of approximately −20 dBm.

(5) Set the CAL AMPL adjustment for 5 divisions on the Spectrum Analyzer display, then activate MAX HOLD.

(6) Reset the sweep oscillator controls for a sweep output from 0.01 GHz—1 GHz. Enable single sweep on the sweep oscillator.

(7) Make a note of the highest and lowest peaks for later comparison.

(8) Deactivate MAX HOLD, and reset the CENTER FREQUENCY to 1.5 GHz.

(9) Reset the sweep oscillator controls for a sweep output from 1 GHz—1.8 GHz. Activate MAX HOLD, then enable single sweep on the sweep oscillator.

(10) Calculate the halfway point between the highest and the lowest peak from the peak data noted in part (7) and this part.

(11) Check that swept frequency flatness is within ±1.0 dB.

b. Check frequency response from 100 Hz to 10 MHz.

(1) Reconnect the test equipment as shown in Figure 4-10. Reset CENTER FREQUENCY to 10 MHz.

(2) Set the generator output for −20 dBm at 10 MHz, and set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	10 MHz
SPAN/DIV	500 kHz
RESOLUTION	1 MHz
REF LEVEL	−18 dBm
VERTICAL DISPLAY	1 dB/DIV
MIN RF ATTEN dB	0
TIME/DIV	AUTO
PEAK/AVERAGE	Fully ccw

(3) Manually tune the Signal Generator towards 50 kHz while simultaneously tuning the CENTER FREQUENCY control to hold the signal at center screen. Note amplitude deviation, and the highest and lowest peaks.

NOTE

As the Signal Generator is tuned towards 50 kHz, the RESOLUTION on the Spectrum Analyzer must be reset to 100 kHz when the generator output frequency reaches 2 MHz. Also, at approximately 200 kHz, the Spectrum Analyzer SPAN/DIV and RESOLUTION BANDWIDTH must be reset to 50 kHz and 10 kHz respectively to prevent the 0 Hz spur from interfering with the signal.

Continue resetting the SPAN/DIV and RESOLUTION as the generator frequency is tuned down towards 100 Hz. Below 100 Hz, it is difficult to obtain a definitive reading because the 0 Hz spur interferes with the signal in this region.

(4) Check that flatness is within ±1 dB.

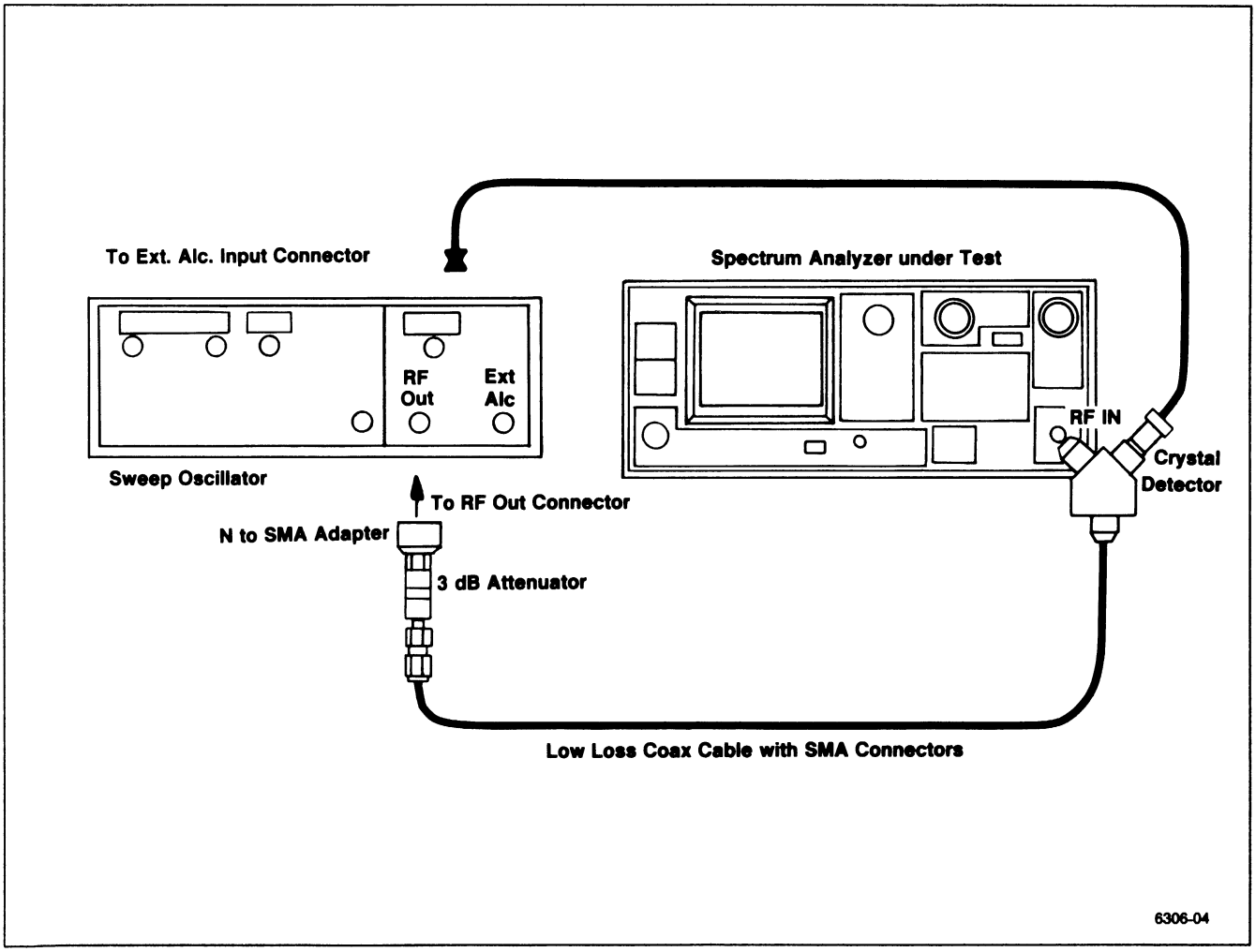


Figure 4-9. Test equipment setup for measuring 0.01 GHz to 1.8 GHz frequency response.

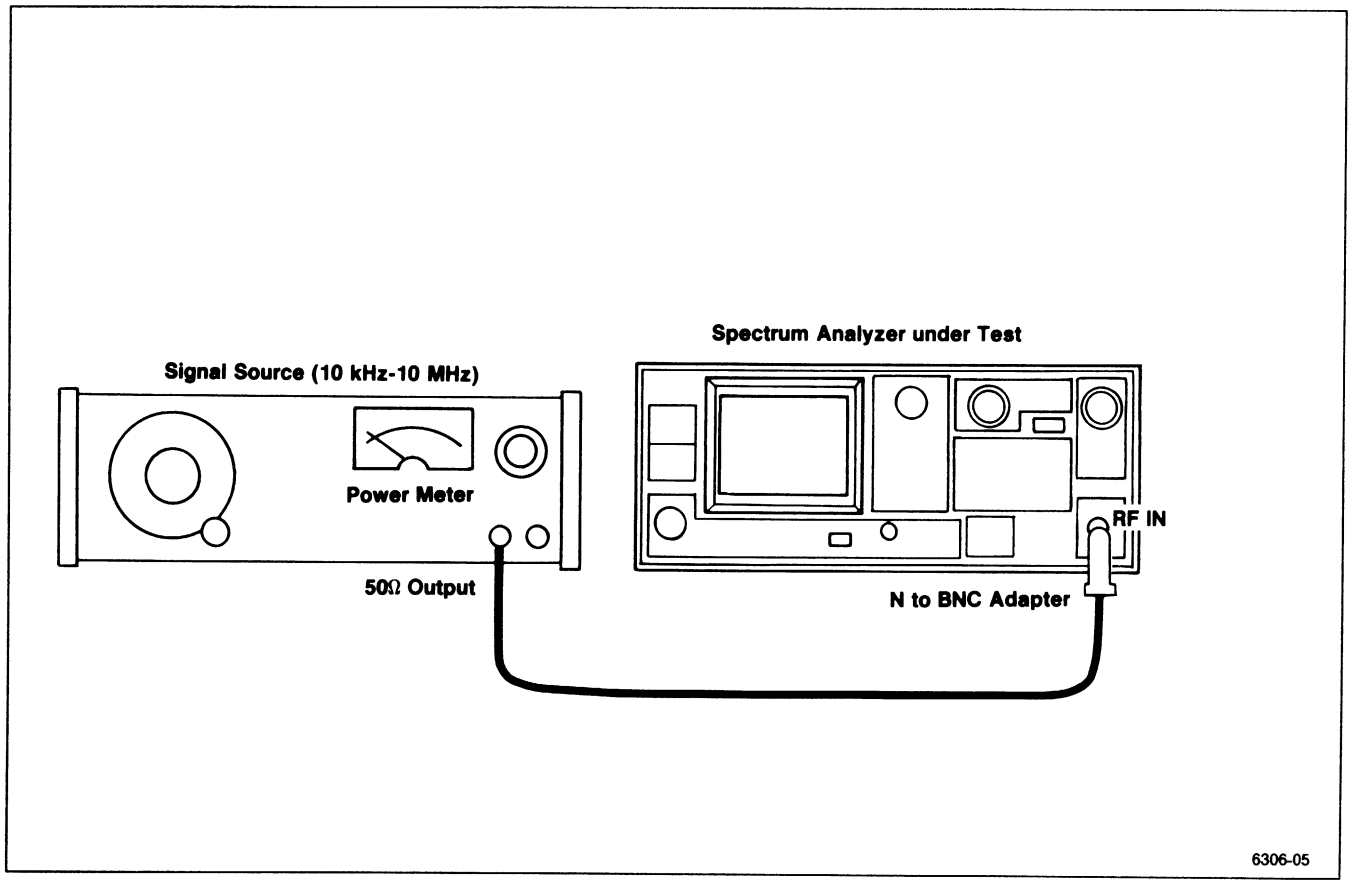


Figure 4-10. Test equipment setup for measuring 100 Hz to 10 MHz frequency response.

11. Check Display Dynamic Range and Accuracy

(80 dB in 10 dB/DIV mode, with an accuracy of ±1.0 dB/10 dB to a maximum cumulative error of ±2.0 dB over the 80 dB window; 16 dB in 2 dB/DIV mode with an accuracy of ±0.4 dB/2 dB to a maximum cumulative error of ±1.0 dB over the 16 dB window; Lin mode is ±5% of full scale)

a. Connect the test equipment as shown in Figure 4-11, using the 10 dB and 1 dB step attenuators. Set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	100 MHz
SPAN/DIV	20 kHz
AUTO RES	On
REF LEVEL	10 dBm
MIN RF ATTEN dB	0
VERTICAL DISPLAY	10 dB/DIV
NARROW VIDEO FILTER	On
PEAK/AVERAGE	Fully Clockwise
TIME/DIV	AUTO

b. Set the attenuators for 0 dB attenuation. Set the generator controls for a 100 MHz output frequency, and carefully set the output level such that the signal peak is at the top graticule line.

c. Add 80 dB of external attenuation in 10 dB steps and note that the signal steps down in 10 dB steps.

d. Check that the signal steps down in 10 dB (±1.0 dB) steps as attenuation is added. Maximum cumulative error should not exceed 2.0 dB over the 80 dB range.

e. Deactivate the NARROW VIDEO FILTER, return the external attenuation to 0 dB, and change the VERTICAL DISPLAY to 2 dB/DIV. Set the signal peak at the reference (top) graticule line, with the generator output control.

f. Add 16 dB of external attenuation in 2 dB steps, and note that the display steps down in 2 dB steps.

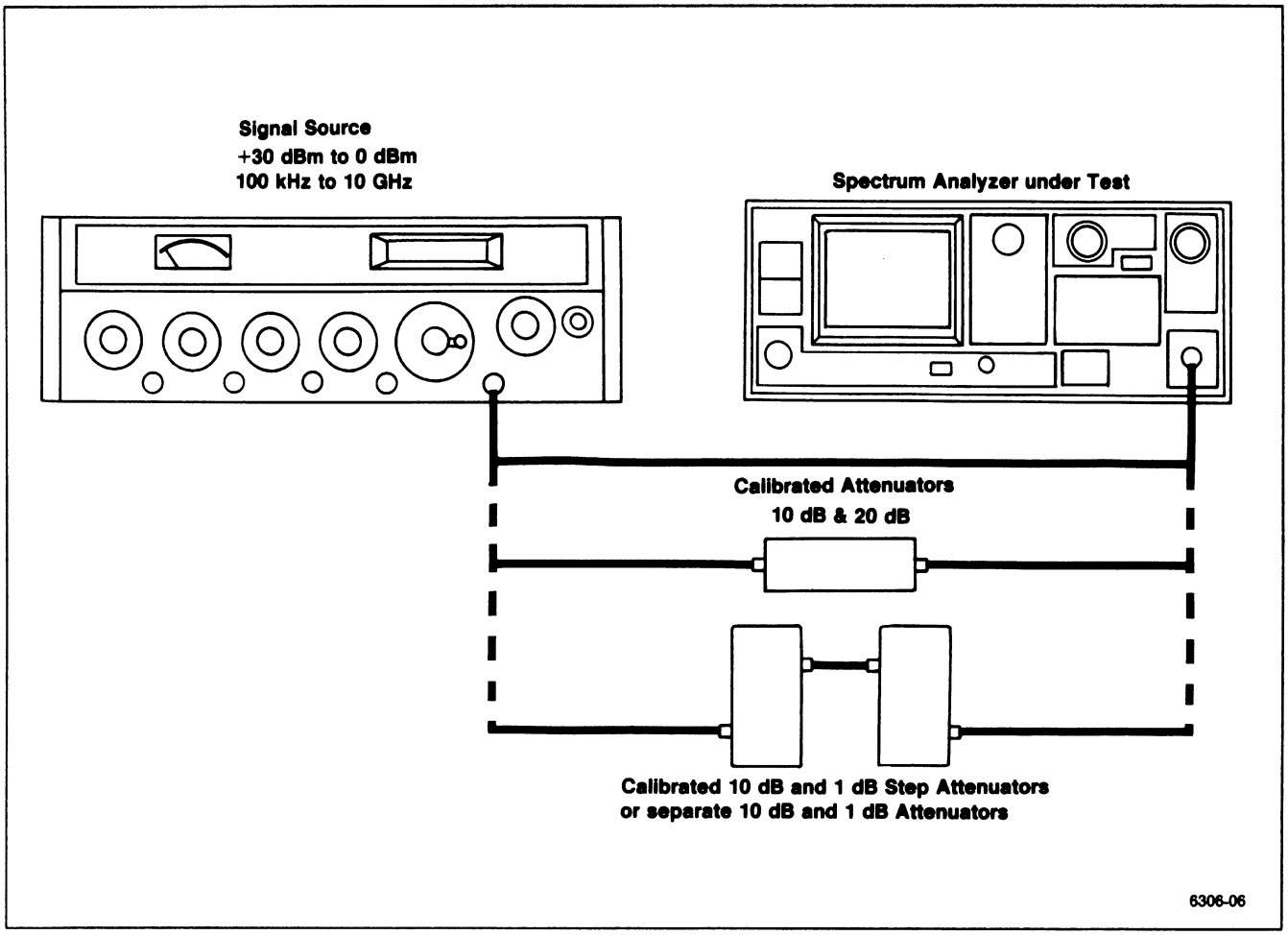


Figure 4-11. Test equipment setup for checking dynamic range and accuracy.

g. Check the display accuracy as attenuation is added. Error should not exceed ±0.4 dB/2 dB step, or exceed a cumulative error of ±1.0 dB over the 16 dB window.

h. Return the external attenuation to 0 dB. Change the VERTICAL DISPLAY to LIN. Set the signal generator output for a full screen display.

i. Check that the signal amplitude decreases to within ±0.4 divisions of half screen as 6 dB of external attenuation is added.

j. Check that the signal amplitude decreases to within ±0.4 divisions of 1/4 screen or half the previous amplitude as an additional 6 dB of attenuation is added.

k. Check that the signal amplitude decreases to within ±0.4 divisions of 1/8 screen or half the last amplitude as an additional 6 dB of attenuation is added (for a total of 18 dB).

l. Return the VERTICAL DISPLAY to 10 dB/DIV and disconnect the generator from the RF INPUT.

12. Check RF Attenuator Accuracy

(Within 0.5 dB/10 dB to a maximum of 1 dB over the 60 dB range)

NOTE

This is a two part procedure. Part I checks the first 30 dB (0—30 dB) range of the rf attenuator, and Part II checks the remaining 30 dB (30 dB—60 dB) range.

PART I

a. Connect the test equipment as shown in Figure 4-12. Set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	Test Frequency
SPAN/DIV	200 kHz
RESOLUTION BANDWIDTH	100 kHz
REF LEVEL	−30 dBm
MIN RF ATTEN dB	0
MIN NOISE	On
VERTICAL DISPLAY	2 dB/DIV
NARROW VIDEO FILTER	On
TIME/DIV	AUTO
PEAK/AVERAGE	Fully Clockwise
VIEW A and VIEW B	On

b. Set the power meter controls as follows:

Mode	Watts
Range Hold	Out
Power Reference	Out

c. Disconnect the power sensor from the power divider, and connect it to the the 1 mW/50 MHz reference output port through an appropriate adapter. Be sure that the 50 MHz reference is turned off.

d. On the power meter, press Sensor Zero and wait for the zero light to turn off. Repeat until a zero is attained.

e. On the power meter, set the 50 MHz reference on and set the Cal Factor switch to the 50 MHz reference. Set the power meter Cal Adj for a 1.000 mW reading.

f. Turn off the 50 MHz reference on the power meter, and reconnect the power sensor to the power divider.

g. Reset the power meter controls as follows:

Cal Factor	Test frequency
Mode	dBm
Range Hold	Out

h. Set the signal generator (HP 8350B/83595A) controls as follows:

Frequency Mode	CW
Frequency	Test Frequency
Output Level	≃−5 dBm

i. Set the generator controls for a −15 dBm power meter reading (approximately −5 dBm generator output level).

j. Tune the CENTER FREQUENCY control to bring the signal to center screen.

k. The Spectrum Analyzer should be displaying a signal of approximately −35 dBm.

l. Use the Spectrum Analyzer's AMPL CAL control to position the signal peak at a convenient graticule line, then activate SAVE A.

m. Establish a reference setting for the first 10 dB increment by pressing dB[Ref on the power meter.

n. Reset the MIN RF ATTEN dB control to 10 and the REFERENCE LEVEL to −20 dBm. Reset the generator output level for a power meter reading of +10 dB (10 dB increase in output level).

o. Check that the difference between the SAVE A and VIEW B displays is less than 0.5 dB. Make a note of the level difference between the SAVE A and VIEW B displays.

p. To check the next 10 dB step, reset the generator for a 0 dB power meter reading, and replace the 20 dB attenuator with a 10 dB attenuator.

q. Repeat parts m through o, except that the next MIN RF ATTEN dB setting will be 20 and the reference level will be −10 dB (Table 4-4).

r. Repeat the procedure for the third 10 dB step using Table 4-4 as a guide for setup information for the third MIN RF ATTEN dB setting.

PART II

a. The 30—60 dB range is checked in the same fashion as the 0—30 dB range using different power levels because of the output level limitation of the signal generator.

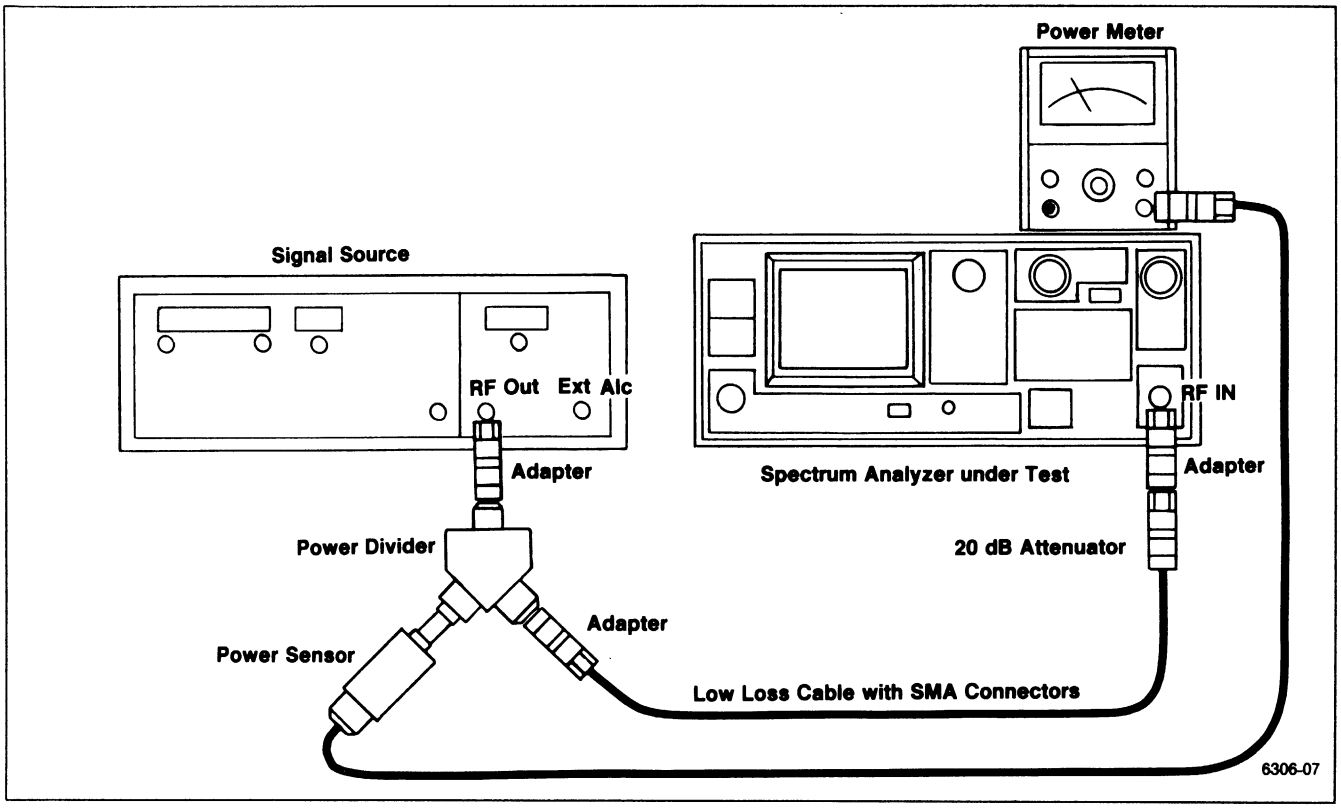


Figure 4-12. RF attenuator test equipment setup.

Table 4-4
0 TO 30 dB RF ATTENUATOR TEST SETTINGS

Spectrum Analyzer Reference Level	MIN RF ATTEN dB Setting	External Attenuator	Power Meter dB(Rel)	Power Meter dBm
−30 dBm	0 dB	20 dB	0 dB=Ref	≃−15 dBm
−20 dBm	10 dB	20 dB	+10 dB	≃−5 dBm
−20 dBm	10 dB	10 dB	0 dB=Ref	≃−15 dBm
−10 dBm	20 dB	10 dB	+10 dB	≃−5 dBm
−10 dBm	20 dB	0 dB	0 dB=Ref	≃−15 dBm
−0 dBm	30 dB	0 dB	+10 dB	≃−5 dBm

b. Connect the test equipment as shown in Figure 4-12. Set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	Test Frequency
SPAN/DIV	200 kHz
RESOLUTION BANDWIDTH	100 kHz
REF LEVEL	−25 dBm
MIN RF ATTEN dB	30
MIN NOISE	On
VERTICAL DISPLAY	2 dB/DIV
NARROW VIDEO FILTER	On
TIME/DIV	AUTO
PEAK/AVERAGE	Fully Clockwise
VIEW A and VIEW B	On

c. Set the power meter controls as follows:

Mode	Watts
Range Hold	Out
Power Reference	Out

d. Disconnect the power sensor from the power divider, and connect it to the 1 mW/50 MHz reference output port through an appropriate adapter. Be sure that the 50 MHz reference is turned off.

e. On the power meter, press Sensor Zero and wait for the zero light to turn off. Repeat until a zero is attained.

f. On the power meter, set the 50 MHz reference on and set the Cal Factor switch to the 50 MHz reference. Set the power meter Cal Adj for a 1.000 mW reading.

g. Turn off the 50 MHz reference on the power meter, and reconnect the power sensor to the power divider.

h. Reset the power meter controls as follows:

Cal Factor	Test frequency
Mode	dBm
Range Hold	Out

i. Set the generator controls for a maximum power meter reading, then reduce the generator output level until the meter reads 11 dB less than the maximum.

j. Tune the CENTER FREQUENCY control to bring the signal to center screen. The REF LEVEL may have to be varied slightly to obtain a convenient on-screen display.

k. Use the Spectrum Analyzer's AMPL CAL control to position the signal peak at a convenient graticule line, then activate SAVE A.

l. Establish a reference setting for the first 10 dB increment by pressing dB{Ref} on the power meter.

m. Incease the MIN RF ATTEN dB setting by 10 and reset the REFERENCE LEVEL 10 dB higher than the level set in part j. Reset the generator output level for a power meter reading of +10 dB. Refer to Table 4-5 for setup information at each rf attenuator setting.

n. Check that the difference between the SAVE A and VIEW B displays is less than 0.5 dB. Make a note of the level difference between the SAVE A and VIEW B displays.

o. Continue to check the second and third attenuator steps using Table 4-5 as a guide for setup information. Make a note of the level difference at each step setting between the SAVE A and VIEW B displays.

p. Using the data noted in step o of Part I and steps n and o of Part II, check that deviation over the entire 60 dB range is less than 1 dB.

Table 4-5
30 TO 60 dB RF ATTENUATOR TEST SETTINGS

Spectrum Analyzer Reference Level	MIN RF ATTEN dB Setting	External Attenuator	Power Meter dB(Rel)	Power Meter dBm
−25 dBm	30 dB	20 dB	0 dB=Ref	(Maximum − 11 dBm)
−15 dBm	40 dB	20 dB	+10 dB	(Maximum − 1 dBm)
−15 dBm	40 dB	10 dB	0 dB=Ref	(Maximum − 11 dBm)
−5 dBm	50 dB	10 dB	+10 dB	(Maximum − 1 dBm)
−5 dBm	50 dB	0 dB	0 dB=Ref	(Maximum − 11 dBm)
+5 dBm	60 dB	0 dB	+10 dB	(Maximum − 1 dBm)

Table 4-6
CORRECTION FACTOR TO DETERMINE TRUE SIGNAL LEVEL

dB Ratio of Signal Plus Noise	3.0	4.0	5.0	6.0	7.0	8.0	9.0	10.0	12.0	14.0
Deduct Correction Factor	3.0	2.20	1.65	1.26	0.97	0.75	0.58	0.46	0.28	0.18

13. Check IF Gain Accuracy

(±0.2 dB/dB Step to a maximum of ±0.5 dB/9 dB except at the decade transitions of −19 dBm to −20 dBm, −29 dBm to −30 dBm, −39 dBm to −40 dBm, −49 dBm to −50 dBm, and −59 dBm to −60 dBm where an additional 0.5 dB can occur for a total of 1 dB/decade. Maximum deviation over the full 87 dB range is within ±2 dB)

This check requires calibrated attenuators to check the 10 dB and 1 dB steps. When making measurements within 10 dB of the noise floor, a correction factor should be used to correct for the logarithmic addition of noise in the system, as shown in Table 4-6.

a. Connect the test equipment as shown in Figure 4-11, using the calibrated 10 dB and 1 dB attenuators (or connect the output of the generator directly to the RF INPUT if individual fixed attenuators are to be used as the standard). Set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	100 MHz
SPAN/DIV	10 kHz
RESOLUTION BANDWIDTH	10 kHz
REF LEVEL	−10 dBm
MIN RF ATTEN dB	0
VERTICAL DISPLAY	1 dB/DIV
WIDE VIDEO FILTER	On
TIME/DIV	AUTO
SAVE A	Off

b. Set the generator controls for a 100 MHz output frequency, and a signal amplitude of six divisions.

c. Activate MIN NOISE and note signal level shift. Level shift must not exceed ±0.8 dB, or 4 minor divisions (attenuator plus gain accuracies).

d. Set the output of the signal generator to reposition the signal level at the 6th graticule line.

e. Switch the REF LEVEL from −10 dBm to −20 dBm in 1 dB steps, adding 1 dB of external attenuation at each step. Note incremental accuracy and the 10 dB gain accuracy. Incremental accuracy must be within 0.2 dB/dB. Maximum cumulative error must not exceed 0.5 dB except when stepping from the 9 dB to 10 dB increment, where the error could be an additional 0.5 dB. This exception does not apply when stepping from −69 dBm to −70 dBm, −79 dBm to −80 dBm, etc.

f. Deactivate MIN NOISE. Return the 1 dB step attenuator to 0 dB, decrease the output of the signal generator by 10 dB or add 10 dB of external attenuation. Reset the generator output so the signal level is again at the 6th graticule line.

g. Change the REF LEVEL from −20 dBm to −30 dBm, in 1 dB increments, with the 1 dB step attenuator, and note incremental and 10 dB step accuracies.

h. Return the 1 dB step attenuator to 0 dB. Decrease the signal level by 10 dB with external attenuation, or with the signal generator output level control, then re-establish the signal reference amplitude.

i. Check the −30 dBm to −40 dBm gain accuracies as in part e.

j. Repeat the procedure checking gain accuracies to −60 dBm.

k. Establish a signal reference amplitude of −60 dBm, activate NARROW VIDEO FILTER, then check gain accuracy to −70 dBm.

l. Decrease the RESOLUTION BANDWIDTH and SPAN/DIV to 1 kHz. Re-establish a signal reference level of −70 dBm as described previously.

m. Check the −70 dBm to −80 dBm gain accuracies by repeating the process previously described.

n. Decrease the RESOLUTION BANDWIDTH to 100 Hz and SPAN/DIV to 50 Hz, re-establish the signal reference level and check the −80 dBm to −90 dBm and −90 dBm to −100 dBm gain accuracies. These ranges are directly related to the −60 dBm to −70 dBm check (parts d through m).

14. Check Gain Variation Between Resolution Bandwidths

(Less than ±0.4 dB with respect to the 1 MHz filter and less than 0.8 dB between any two filters)

Before performing this check, do a front panel CAL procedure by pressing <SHIFT> CAL and performing the steps prompted by the spectrum analyzer.

a. Apply the CAL OUT signal to the RF INPUT, and set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	100 MHz
SPAN/DIV	100 kHz
RESOLUTION BANDWIDTH	1 MHz
REF LEVEL	−18 dBm
MIN RF ATTEN dB	0
VERTICAL DISPLAY	1 dB/DIV
MIN NOISE	On
TIME/DIV	AUTO

b. Activate the Δ A mode by pressing FINE.

c. Reset the REFERENCE LEVEL control to position the calibrator signal at the 7th graticule line (1 major division from the top), then activate SAVE A to store the 1 MHz amplitude.

d. Change the RESOLUTION BANDWIDTH to 100 kHz and SPAN/DIV to 10 kHz.

e. Check that amplitude deviation from the 1 MHz reference is no more than ±0.4 dB.

f. Change the RESOLUTION BANDWIDTH to 10 kHz and the FREQ SPAN/DIV to 1 kHz.

g. Check that amplitude deviation from the 1 MHz reference level is no more than ±0.4 dB.

h. Repeat the procedure to check the remaining filters (1 kHz, 100 Hz, and 30 Hz) to verify that the signal amplitude does not change more than ±0.4 dB from the 1 MHz reference level.

i. Check variation between any two filters (0.8 dB) by finding the filter that has the lowest amplitude, saving it on the A-trace, then comparing the other filters to the saved trace.

j. Deactivate SAVE A.

Table 4-7
SENSITIVITY
EQUIVALENT INPUT NOISE VERSUS RESOLUTION BANDWIDTH[a]

	1 MHz	300 kHz[b]	100 kHz	10 kHz	1 kHz	100 Hz	30 Hz
50Ω INPUT	−85 dBm	−90 dBm	−95 dBm	−105 dBm	−115 dBm	−125 dBm	−130 dBm
75Ω INPUT (Option 07)	−36 dBmV	−41 dBmV	NA	−56 dBmV	−66 dBmV	−76 dBmV	−81 dBmV

15. Check Sensitivity

(Refer to Table 4-7)

a. Connect the CAL OUT signal to the RF INPUT, and perform the <SHIFT> CAL routine. Remove the CAL OUT signal from the RF INPUT, and terminate the RF INPUT in its characteristic impedance. Set the Spectrum Analyzer controls as follows:

SPAN/DIV	MAX
RESOLUTION BANDWIDTH	10 kHz
REF LEVEL	−100 dBm
MIN RF ATTEN dB	0
VERTICAL DISPLAY	2 dB/DIV
NARROW VIDEO FILTER	On
VIEW A & VIEW B	On
PEAK/AVERAGE	Fully Clockwise
TIME/DIV	1 s

NOTE

The UNCAL light will be on with the above front-panel control settings.

b. Enable a marker by pressing TUNE CF/MKR. Tune the marker to the highest point on the noise floor. Activate ZERO SPAN, and change the RESOLUTION BANDWIDTH to 1 MHz and the REFERENCE LEVEL as necessary to view the baseline.

c. Check that the noise floor (level) is down as per Table 4-7 (at least −85 dBm down if checking the standard instrument, or −36 dBmV if checking the 75Ω input on an Option 07 instrument).

d. Reduce the RESOLUTION BANDWIDTH one step at a time (and reset the REF LEVEL each time) and check that the noise floor for the respective filters is down as per Table 4-7.

16. Check Residual Spurious Response

(With no input signal, −100 dBm or less)

a. Remove any signal connected to the RF INPUT, and terminate the RF INPUT in 50Ω. Set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	50 MHz
SPAN/DIV	10 MHz
RESOLUTION BANDWIDTH	10 kHz
REF LEVEL	−50 dBm
MIN RF ATTEN dB	0
VERTICAL DISPLAY	10 dB/DIV
TIME/DIV	AUTO
PEAK/AVERAGE	ccw

b. Press <SHIFT> STEP ENTRY and enter 100 MHz. This will allow changing center frequency in 100 MHz increments by use of the +STEP and −STEP pushbuttons.

c. Scan the frequency range in 100 MHz increments. Note the amplitude of any spurious response. Spurious response amplitudes must not exceed −100 dBm.

d. When spurious responses are displayed, center the response on the display. Reduce the SPAN/DIV to 10 kHz, set the REFERENCE LEVEL to −100 dBm, and VERTICAL DISPLAY to 2 dB/Div. Check that the response amplitude is <−100 dBm.

17. Check Zero Frequency Spur

(−24 dBm or less)

a. Set the Spectrum Analyzer controls as follows

CENTER FREQUENCY	0 Hz
SPAN/DIV	2 MHz
RESOLUTION BANDWIDTH	1 MHz
REF LEVEL	−20 dBm
MIN RF ATTEN dB	0
MIN NOISE	On
VERTICAL DISPLAY	10 dB/DIV
VIEW A & VIEW B	On
TIME/DIV	AUTO

[a] Equivalent maximum input noise (average noise for each resolution bandwidth).

[b] Option 07 replaces the 100 kHz filter with a 300 kHz filter.

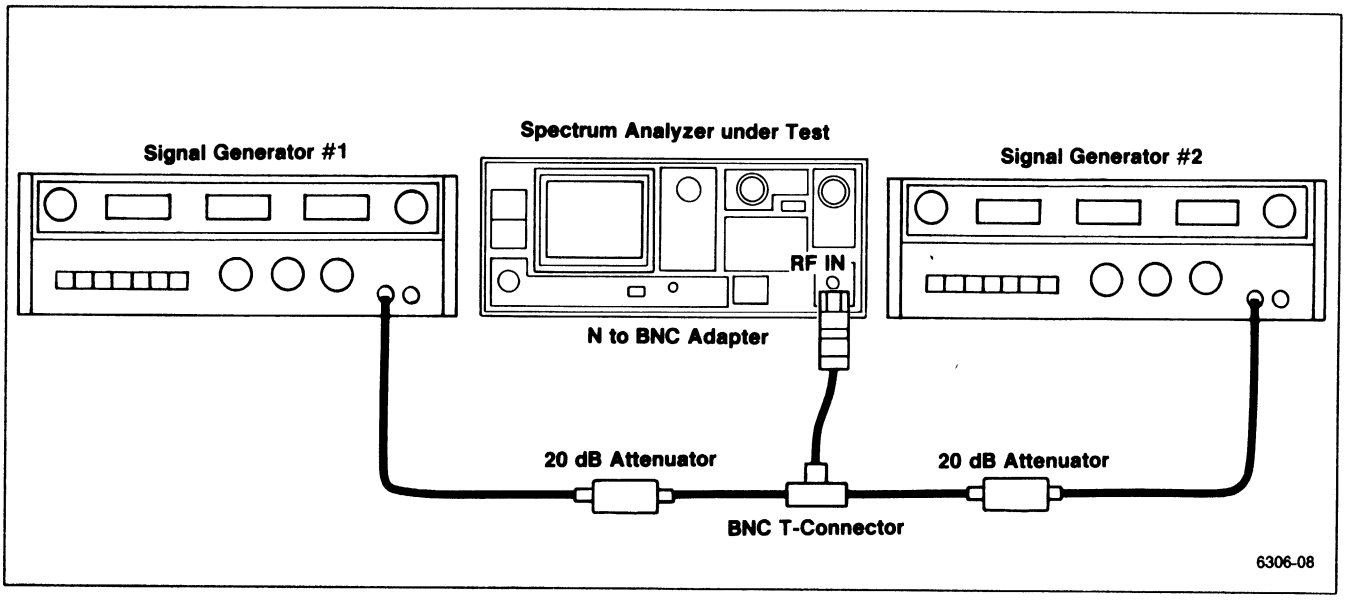


Figure 4-13. Test equipment setup for checking intermodulation distortion.

b. Apply the CAL OUT signal to the RF INPUT and initiate the AUTOCAL routine by pressing <SHIFT> CAL and following the instructions displayed on the crt.

c. Remove the calibrator signal from the RF INPUT, and terminate the RF INPUT in its characteristic impedance.

d. Check that the amplitude of the 0 Hz spur is less than −24 dBm.

18. Check Intermodulation Distortion

(Third order products at least 70 dB down from any two on-screen signals, within any frequency span)

a. Connect the test equipment as shown in Figure 4-13, and set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	Within 2 MHz of Test Generators
SPAN/DIV	5 MHz
RESOLUTION BANDWIDTH	100 kHz
REF LEVEL	−30 dBm
MIN RF ATTEN dB	0
VERTICAL DISPLAY	10 dB/DIV
TIME/DIV	AUTO

b. Set the generator outputs approximately 2 MHz apart, and set the output levels for full screen signals.

c. Decrease the separation of the generator frequencies to 1 MHz. Reset the SPAN/DIV to 500 kHz and RESOLUTION BANDWIDTH to 10 kHz.

d. Check that the third order IM products are at least 70 dB down from the input signal level. See Figure 4-14.

NOTE

Use the Video Filter and very slow sweep rates to help resolve these sidebands.

e. Decrease the signal separation and SPAN/DIV settings and re-check for sidebands. Check for IM products at other spans of the frequency range. IM products should be −70 dBc or more.

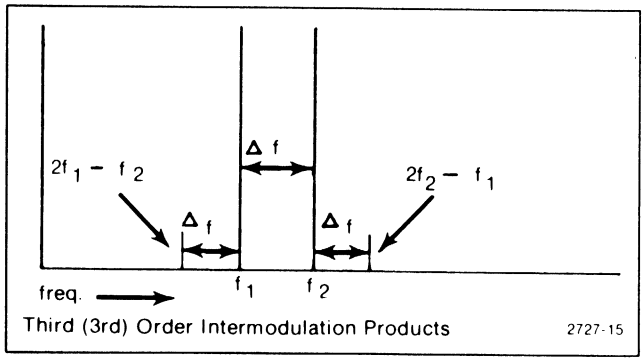


Figure 4-14. Intermodulation products.

19. Check Harmonic Distortion

(−60 dBc or less measured across the entire RF range with −30 dBm input and 0 dB attenuation)

a. Connect the test equipment as shown in Figure 4-15, and set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	same as generator
SPAN/DIV	5 MHz
AUTO RES	On
REF LEVEL	−30 dBm
MIN RF ATTEN dB	0
VERTICAL DISPLAY	10 dB/DIV
WIDE VIDEO FILTER	On
MIN DISTORTION	On
VIEW A and VIEW B	On
TIME/DIV	AUTO

b. Adjust the generator frequency for maximum amplitude, and set the generator output level for a full screen (−30 dBm) signal.

NOTE

In Figure 4-15, the filter shown must have a minimum of 40 dB rolloff to attenuate multiples of the generator frequency, and the frequency of the signal generator depends on the frequency characteristics of the filter.

c. Set the CENTER FREQUENCY to (2 X Input Frequency), FREQ SPAN/DIV to 500 kHz, and RESOLUTION BANDWIDTH to 10 kHz.

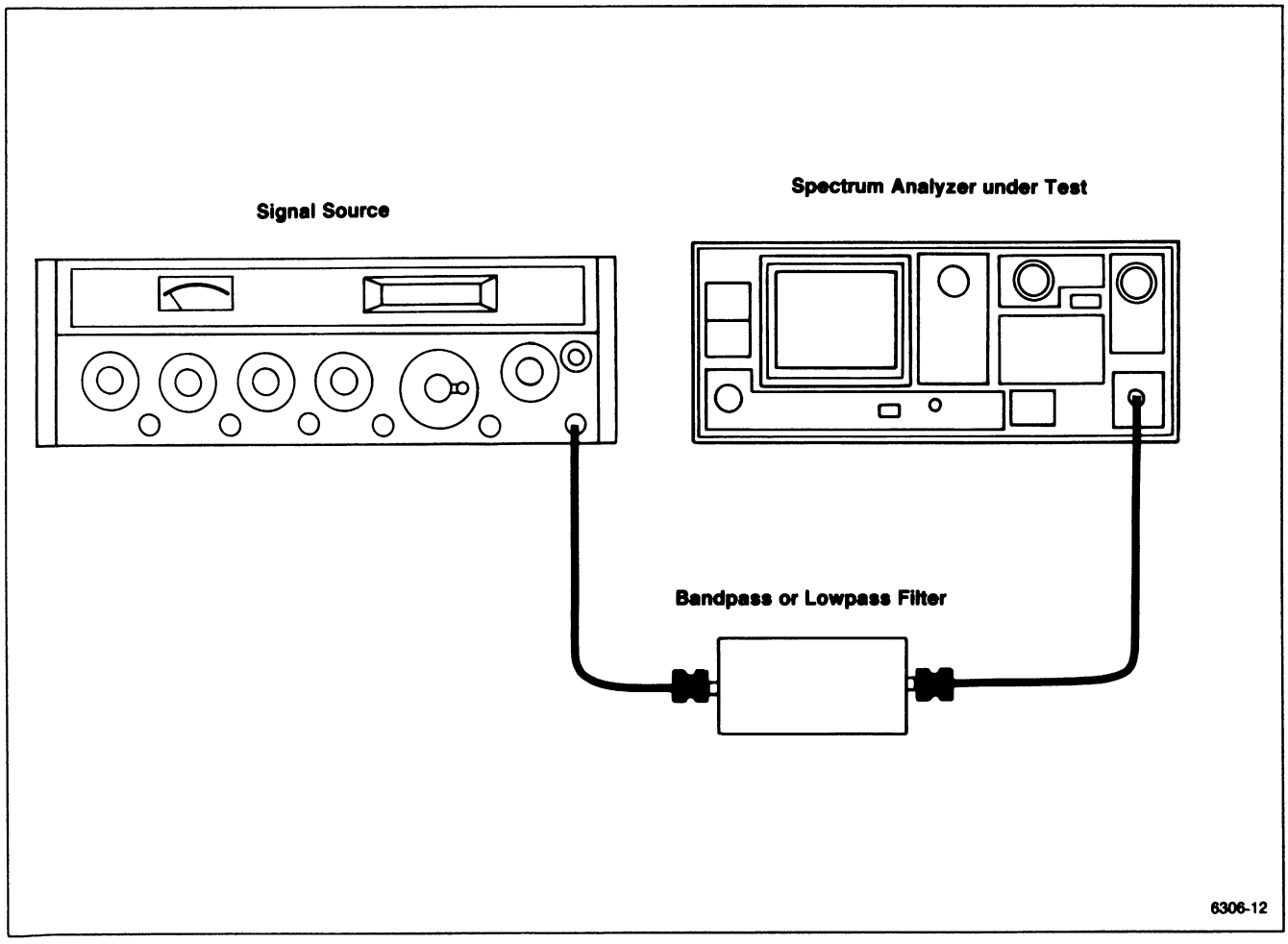


Figure 4-15. Test equipment setup for checking harmonic distortion.

d. Check that the second harmonic of the input signal is at least 60 dB below the −30 dBm carrier.

e. Set the CENTER FREQUENCY to the 3rd harmonic.

f. Check that the third harmonic of the input signal is at least 60 dB down from the −30 dBm carrier.

20. Check LO Emission

(−70 dBm or less)

a. Monitor the RF INPUT with a high frequency spectrum analyzer such as a 2755 or 492A. Set the test spectrum analyzer controls as follows:

Center Frequency	2072 MHz
Span/Div	2 MHz
Min RF Atten dB	0
Vertical Display	10 dB/DIV
Time/Div	Auto
Triggering	Free Run
Baseline Clip	Off
Reference Level	−70 dBm
Auto Resolution	On
View A and View B	On
Video Filter	Wide
Peak/Average	Fully Clockwise

b. Set the Spectrum Analyzer under test as follows:

CENTER FREQUENCY	0 Hz
REF LEVEL	−30 dBm
SPAN/DIV	100 kHz
MIN RF ATTEN dB	0
PEAK/AVERAGE	Fully Clockwise

c. Check for any indication of LO emission. LO emission must be less than −70 dBm.

21. Check 1 dB Compression Point

(−20 dBm)

NOTE

Calibrate the power meter before making this measurement.

a. Use the power meter to set the output level of a signal generator to 0 dBm at 1.7 GHz. Be sure not to disturb the output level setting of the generator.

b. Connect the test equipment as shown in Figure 4-16, using the generator with the calibrated output level. Set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	1.7 GHz
SPAN/DIV	100 kHz
AUTO RES	On
REF LEVEL	−30 dBm
MIN RF ATTEN dB	0
VERTICAL DISPLAY	10 dB/DIV
VIEW A and VIEW B	On
TIME/DIV	AUTO

c. Set the attenuators for 30 dB of attenuation.

d. Monitor the 10 MHz IF output on the rear panel with a test spectrum analyzer through a 1 dB step attenuator. Set this step attenuator for 0 dB of attenuation.

e. Set the test spectrum analyzer controls as follows:

Center Frequency	10 MHz
Frequency Span/Div	1 MHz
Resolution	Auto
Ref Level	0 dBm
Vertical Display	2 dB/Div
Time/Div	Auto

f. Use the test spectrum analyzer Center Frequency control to center the 10 MHz signal on the test spectrum analyzer.

g. Activate ZERO SPAN and set the CENTER FREQUENCY control to maximize the 10 MHz signal on the test spectrum analyzer display.

h. Reset the test spectrum analyzer reference level for a four division excursion of the signal.

i. Increase the input signal level to the Spectrum Analyzer by switching out 1 dB of attenuation between the signal generator and the RF INPUT. Add 1 dB of attenuation between the 10 MHz IF output and the test spectrum analyzer.

j. Check that the 10 MHz IF output level on the test spectrum analyzer display remains constant as 1 dB of attenuation is removed from the generator output path and inserted in the 10 MHz IF output path.

k. Continue to increase the input signal level to the RF INPUT by 1 dB increments while increasing the attenuation between the 10 MHz IF output and the test spectrum analyzer until the signal amplitude decreases 1 dB (0.5 division). This is the 1 dB compression point.

l. Check that the 1 dB compression point occurs at −20 dBm or less (20 dB or less attenuation between the generator and the RF INPUT).

22. Check Triggering Operation and Sensitivity

(Internal trigger: 2 divisions or more)
(External trigger: 1.0 V peak from 15 Hz to 500 kHz)

a. Connect the test equipment as shown in Figure 4-17.

b. Set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	100 MHz
SPAN/DIV	10 kHz
RESOLUTION BANDWIDTH	1 MHz
REF LEVEL	−30 dBm
VERTICAL DISPLAY	LIN
TRIGGERING	INT
TIME/DIV	5 ms
VIEW A and VIEW B	Off

c. Set the signal source output amplitude for −30 dBm, and an output frequency of 100 MHz. Note that the signal source will be modulated by the function generator.

d. Decrease the output of the signal source so the display is half screen, then modulate the signal source with a 1 kHz sine wave.

e. Activate ZERO SPAN and, if necessary, reset the CENTER FREQUENCY control for maximum response.

f. Set the function generator output for a modulation amplitude of two divisions.

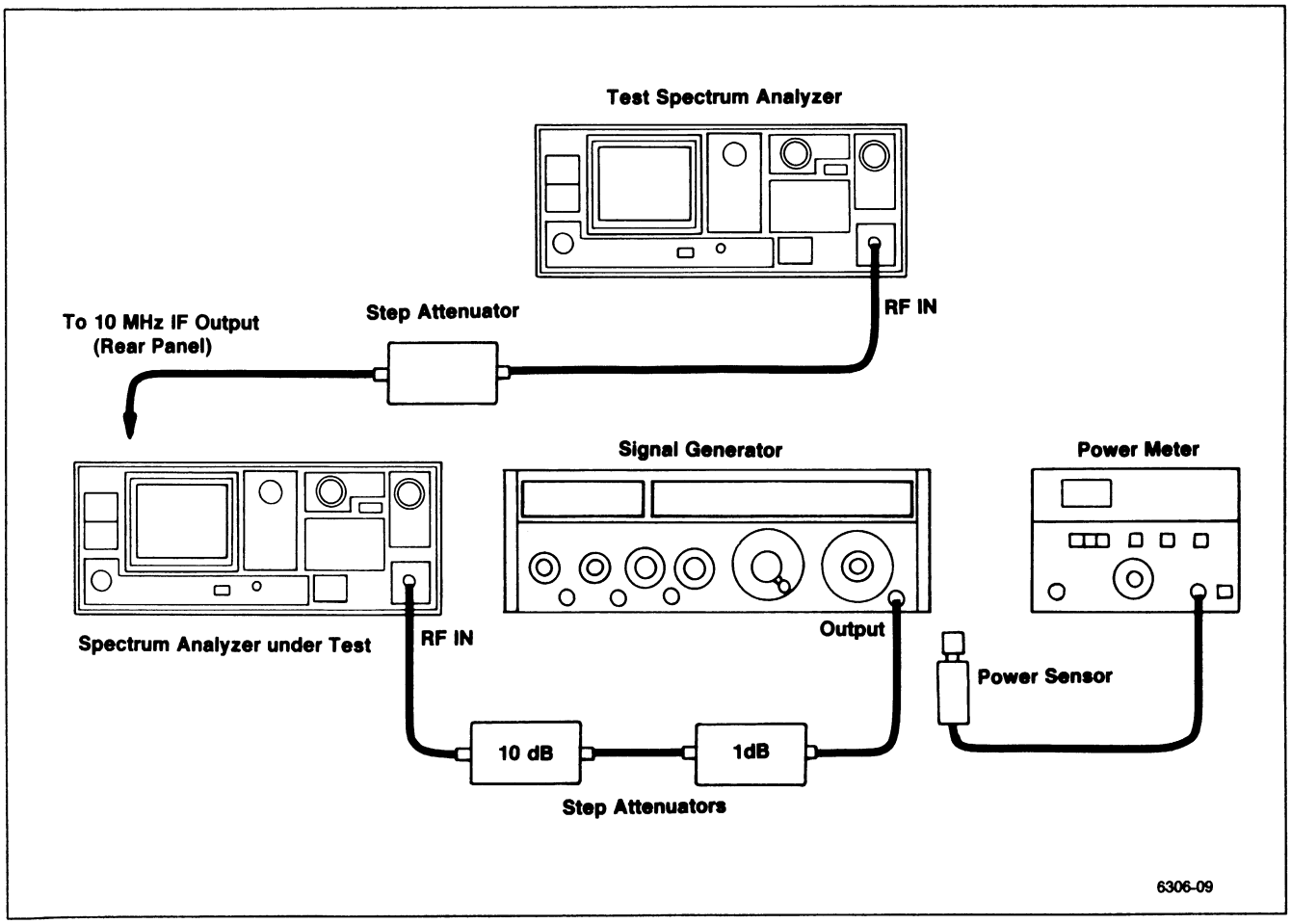


Figure 4-16. Test equipment setup for checking 1 dB input compression point.

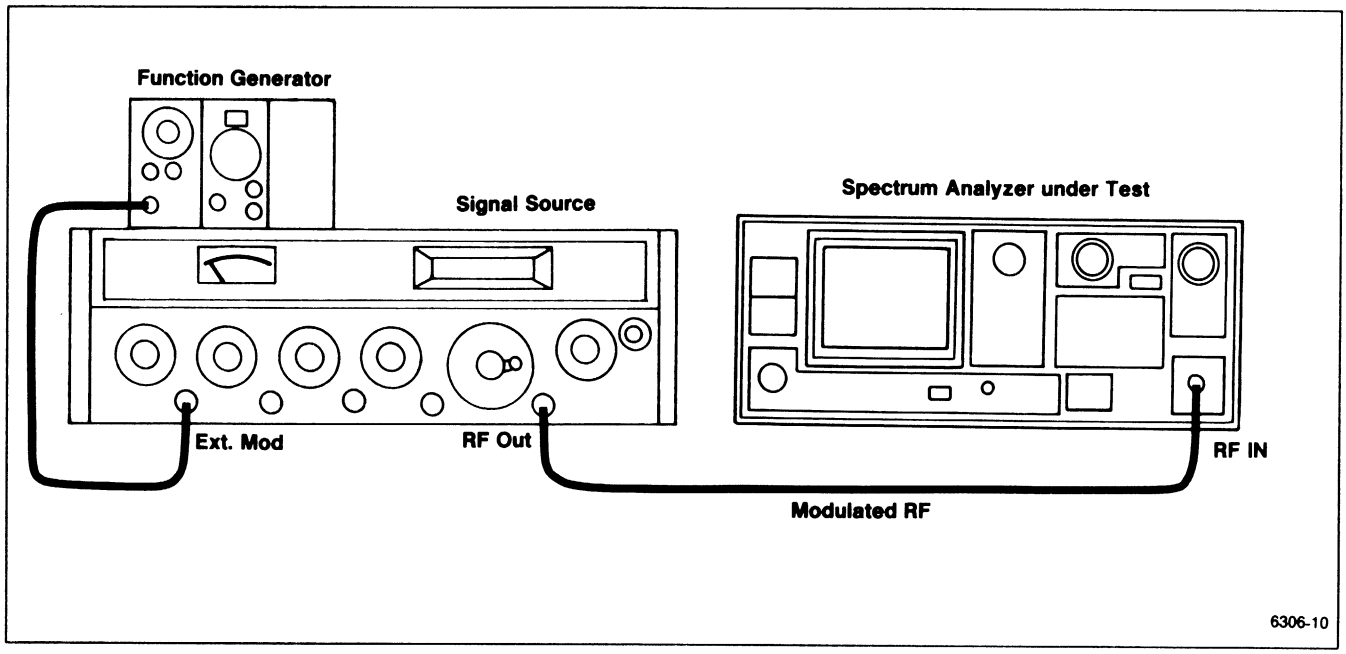


Figure 4-17. Test equipment setup for checking internal trigger characteristics.

g. Check the internal trigger operation in the 15 Hz through 500 kHz frequency range.

NOTE

Because of deflection amplifier response, the display amplitude will decrease at the high frequency end. The triggering signal can also be applied to the MARKER/VIDEO connector on the rear panel if a jumper is connected between pins 1 and 5 (Video Select) of the rear-panel ACCESSORIES connector (Figure 4-18).

h. Connect the test equipment as shown in Figure 4-19.

i. Set the function generator output frequency at 1 kHz, and output level at 2 V peak-to-peak, as indicated on the test oscilloscope.

j. Activate EXT TRIGGERING.

k. Check that the sweep is triggered over the frequency range of 15 Hz to 500 kHz.

l. Return the TRIGGERING to FREE RUN and the input signal level to 0 V.

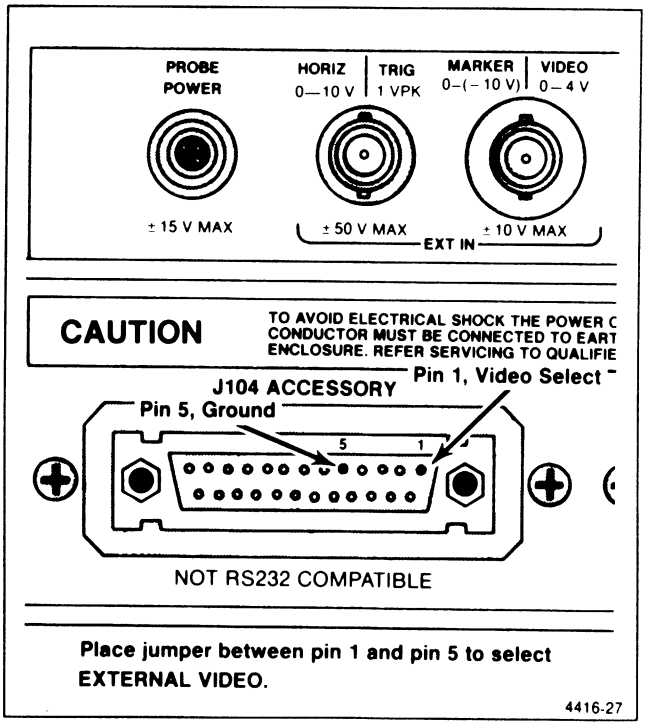


Figure 4-18. External video select pins on ACCESSORIES connector and input to the MARKER | VIDEO for signal to check internal triggering.

23. Check External Sweep Operation

(not a performance requirement)

{0 to 10 V (dc + peak ac) ±1 V for a full screen deflection}

a. Connect the test equipment as shown in Figure 4-19. Set the Spectrum Analyzer controls as follows:

VERTICAL DISPLAY	2 dB/DIV
TIME/DIV	EXT
VIEW A and VIEW B	Off

b. Set the function generator controls for no output (0 V).

c. Use the POSITION control to position the crt beam on the left graticule edge. This establishes the 0 V reference.

d. Reset the function generator output frequency to 1 kHz, and increase its output level for a full 10-division sweep on the Spectrum Analyzer.

e. Check that the function generator output level is 20 V peak-to-peak ±2 V.

NOTE

A variable voltage source can be used in place of the function generator to check external sweep operation. If used, the range would be 0 V to +10 V.

f. Disconnect and remove the test equipment. Return TIME/DIV to AUTO.

24. Check VERT OUTPUT Signal

(not a performance requirement)

(0.5 V ±5% per division of display from the center line)

a. Monitor the VERT OUTPUT with a dc-coupled test oscilloscope.

b. Set the test oscilloscope controls for a sensitivity of 1 V/div and a sweep rate of 10 ms.

c. Set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	100 MHz
SPAN/DIV	100 kHz
RESOLUTION BANDWIDTH	100 kHz
REF LEVEL	−20 dBm
VERTICAL DISPLAY	2 dB/DIV
VIEW A and VIEW B	Off
TRIGGERING	FREE RUN
TIME/DIV	AUTO

d. Apply the CAL OUT signal to the RF INPUT and verify that the signal amplitude is full screen. If not, perform the <SHIFT> CAL routine.

e. Check that the amplitude of the VERT OUTPUT signal is 4 V peak-to-peak ±0.2 V centered around 0 Vdc as displayed on the test oscilloscope. See Figure 4-20.

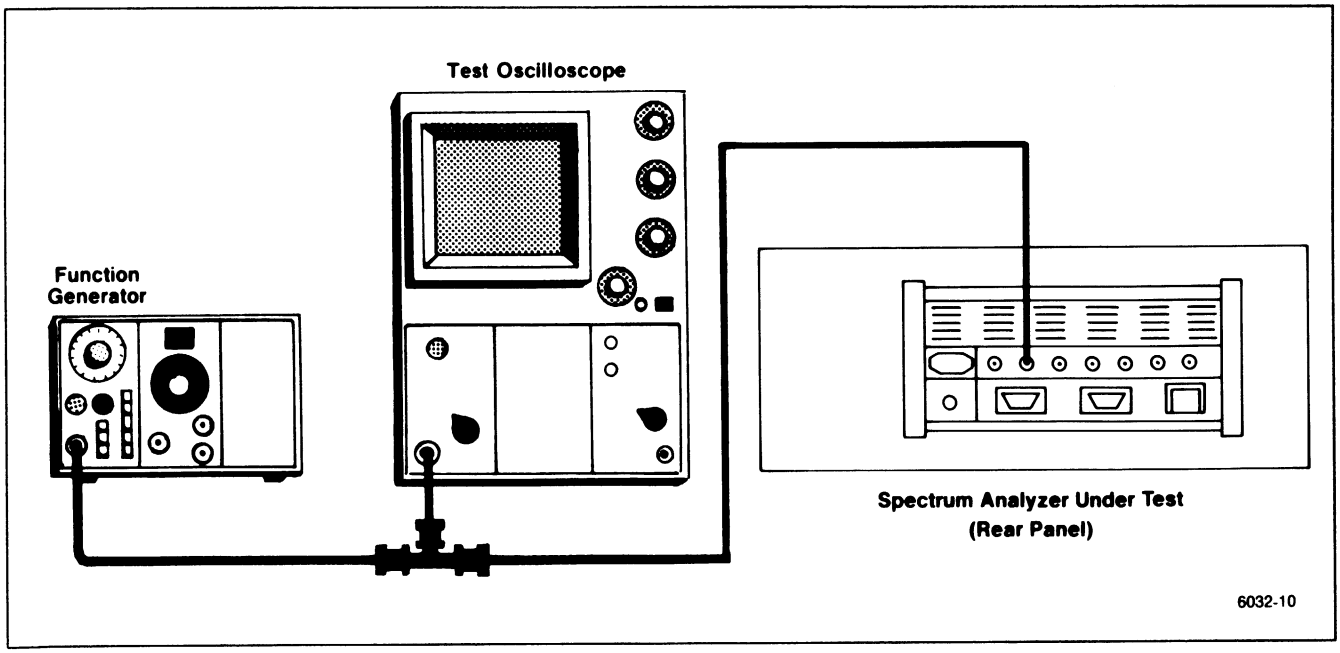


Figure 4-19. Test equipment setup for checking external triggering and horizontal input characteristics.

25. Check HORIZ OUTPUT Signal Level

(not a performance requirement)
(0.5 V/division ±5% either side of center)

a. Monitor the HORIZ OUTPUT with a dc-coupled test oscilloscope.

b. Set TIME/DIV to MNL, and vary the MANUAL SCAN control for a five division beam deflection left and right of center screen. Note the voltage sweep on the test Oscilloscope as the MANUAL SCAN control is varied.

c. Check that the output voltage varies 5 V ±10% peak-to-peak, centered around 0 Vdc.

d. Reset the TIME/DIV to AUTO. Disconnect and remove the test equipment.

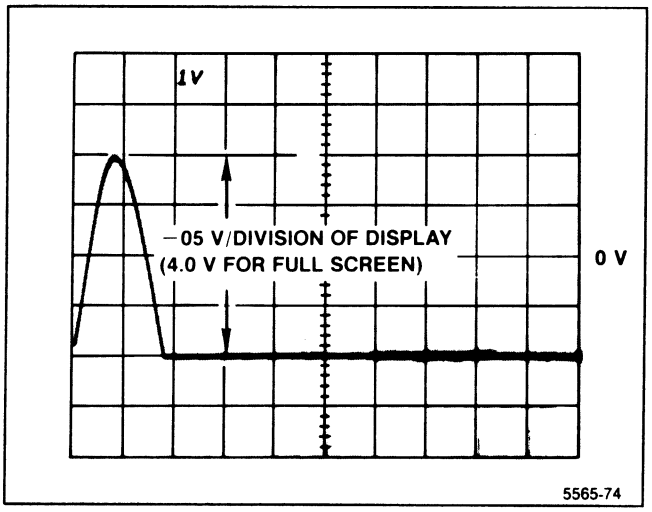


Figure 4-20. Test oscilloscope display of VERT output with a full screen display on the Spectrum Analyzer.

OPTION INSTRUMENTS

26. Check Option 05 Reference Oscillator Accuracy

(Aging rate is $\leq 1 \times 10^{-7}$)

The 10 MHz Reference Oscillator accuracy is not a performance requirement; however, it must be checked so the center frequency accuracy can be verified. Since the Calibrator is locked to the 10 MHz Oscillator this procedure verifies accuracy by counting the frequency of the calibrator signal.

a. Connect the CAL OUT signal to the frequency counter. (Counters with a frequency range above 200 MHz may require a 150 MHz low pass filter to ensure a stable trigger on the 100 MHz CAL OUT signal).

NOTE

The Tektronix DC 510 must be modified to accept an external oscillator reference. Refer to the TM500/TM5000 Series Rear Interface Data Book, Part No. 070-2088-04 for modification instructions.

b. Connect the frequency standard to the External Frequency Standard Input of the frequency counter.

c. Check that the frequency of the CAL OUT signal is 100 MHz ±10 Hz.

d. Disconnect the counter from the CAL OUT connector.

27. Check Option 05 Counter Accuracy

(CF × Reference Frequency Error + 12 Hz + 1 count)

a. Set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	500 MHz
SPAN/DIV	20 kHz
AUTO RES	On
REF LEVEL	−30 dBm
VERTICAL DISPLAY	10 dB/DIV
TIME/DIV	AUTO
TRIGGERING	FREE RUN

b. Apply the CAL OUT signal to the RF INPUT, and center the 500 MHz marker calibrator harmonic.

c. Press <SHIFT> CNT RES and enter 1 Hz via the Data Entry keypad.

d. Press COUNT and note that the error over several counts does not exceed 13 Hz. The factor (CF × Reference Frequency Error) is cancelled when the CAL OUT signal is used.

e. Reset SPAN/DIV to 500 kHz.

f. Press <SHIFT> CNT RES and enter 1 kHz for a counter resolution of 1 kHz.

g. Press COUNT and note that the error over several counts does not exceed 1 kHz.

h. Reset the SPAN/DIV to 200 kHz and repeat part g.

i. Set the CENTER FREQUENCY to 1.8 GHz or 1.7 GHz and repeat the counter accuracy check for this end of the band.

28. Check Option 05 Counter Sensitivity

(At least 20 dB above the average noise level at center screen or at marker, and no more than 60 dB down from the reference level)

a. Apply the CAL OUT signal to the RF INPUT via a 1 dB and a 10 dB step attenuator. Set both attenuators for 0 dB attenuation.

b. Set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	100 MHz
SPAN/DIV	1 MHz
RESOLUTION BANDWIDTH	1 MHz
REF LEVEL	0 dBm
NARROW VIDEO FILTER	On
VERTICAL DISPLAY	10 dB/DIV
TIME/DIV	AUTO
TRIGGERING	FREE RUN

c. Set the 1 dB and 10 dB attenuators such that the signal amplitude is approximately 20 dB above the noise floor.

d. Press <SHIFT> CNT RES and enter 1 Hz via the Data Entry keypad.

e. Press COUNT and note that the counter is counting the signal with the accuracy noted in performance check step 2.

f. Reset SPAN/DIV and RESOLUTION BANDWIDTH to 100 Hz, REF LEVEL to -30 dBm, and activate WIDE VIDEO FILTER.

g. Reset the 1 dB and 10 dB attenuators such that the signal amplitude is approximately 60 dB down from the reference level.

h. Press COUNT and note that the counter is counting the signal with the accuracy noted in performance check step 2.

29. Check Option 05 External Reference Input Power and Frequency

(+15 dBm to −15 dBm; 1, 2, 5, or 10 MHz, ±5 ppm)

a. Equipment setup is shown in Figure 4-21. Connect the output of the signal generator to a frequency counter and set the generator frequency to 10 MHz, ±50 Hz.

b. Disconnect the counter and apply the generator output to the EXTERNAL REFERENCE input connector on the rear panel of the spectrum analyzer. Set the generator output to +15 dB.

c. Check that the crt readout for Reference Oscillator reads "E".

d. Connect the spectrum analyzer CAL OUT connector to the counter and note that the counter readout is 100 MHz, ±500 Hz.

e. Decrease the signal generator output to −15 dBm and note that the crt readout is still "E" and the frequency counter still reads 10× the reference signal frequency. If the crt readout changes to "E-U", recheck the external reference source for 10 MHz ±50 Hz at −15 dBm.

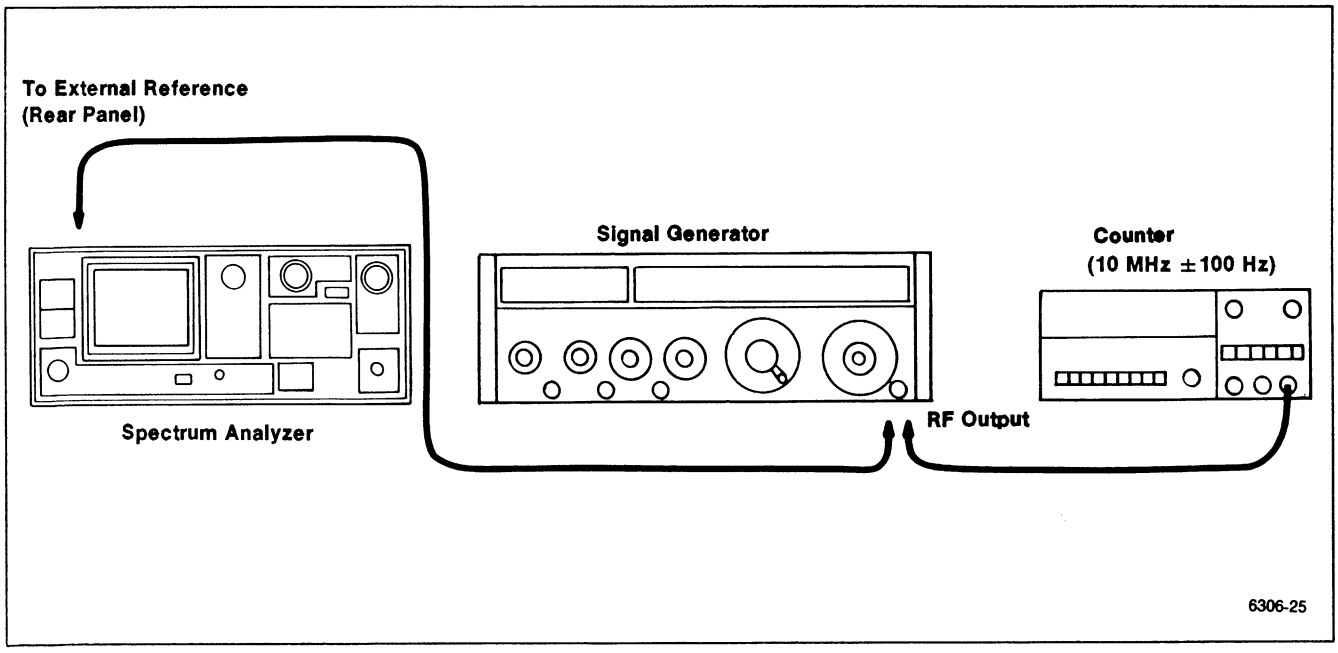


Figure 4-21. Test equipment setup for checking Option 05 external reference input power.

30. Check Option 07 Calibrator Output
(+20 dBmV ±0.5 dB)

a. Connect the 50Ω port of the 75Ω to 50Ω Minimum Loss Attenuator to a 100 MHz 50Ω source.

b. Monitor the 75Ω port of the 75Ω to 50Ω Minimum Loss Attenuator with the power meter.

c. Set the generator output level for a reading of −28.95 dBm on the power meter.

d. Disconnect the power meter from the 75Ω port and connect the 75Ω port to the 75Ω INPUT of the Spectrum Analyzer via a 75Ω cable.

e. Set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	100 MHz
SPAN/DIV	500 kHz
RESOLUTION BANDWIDTH	1 MHz
REF LEVEL	+18 dBmV
MIN RF ATTEN dB	0
VERTICAL DISPLAY	1 dB/DIV
TIME/DIV	AUTO
PEAK/AVERAGE	Fully Clockwise

f. Set the AMPL CAL control on the Spectrum Analyzer for a 6-division excursion of the signal.

g. Remove the 75Ω cable from the 75Ω port of the 75Ω to 50Ω Minimum Loss Attenuator and connect it to the CAL OUT connector on the Spectrum Analyzer (CAL OUT to 75Ω INPUT).

h. Check that the display is 6 divisions ±0.5 dB.

i. Set the Spectrum Analyzer REF LEVEL to +20 dBmV and reset the the AMPL CAL control for an 8-division excursion of the signal.

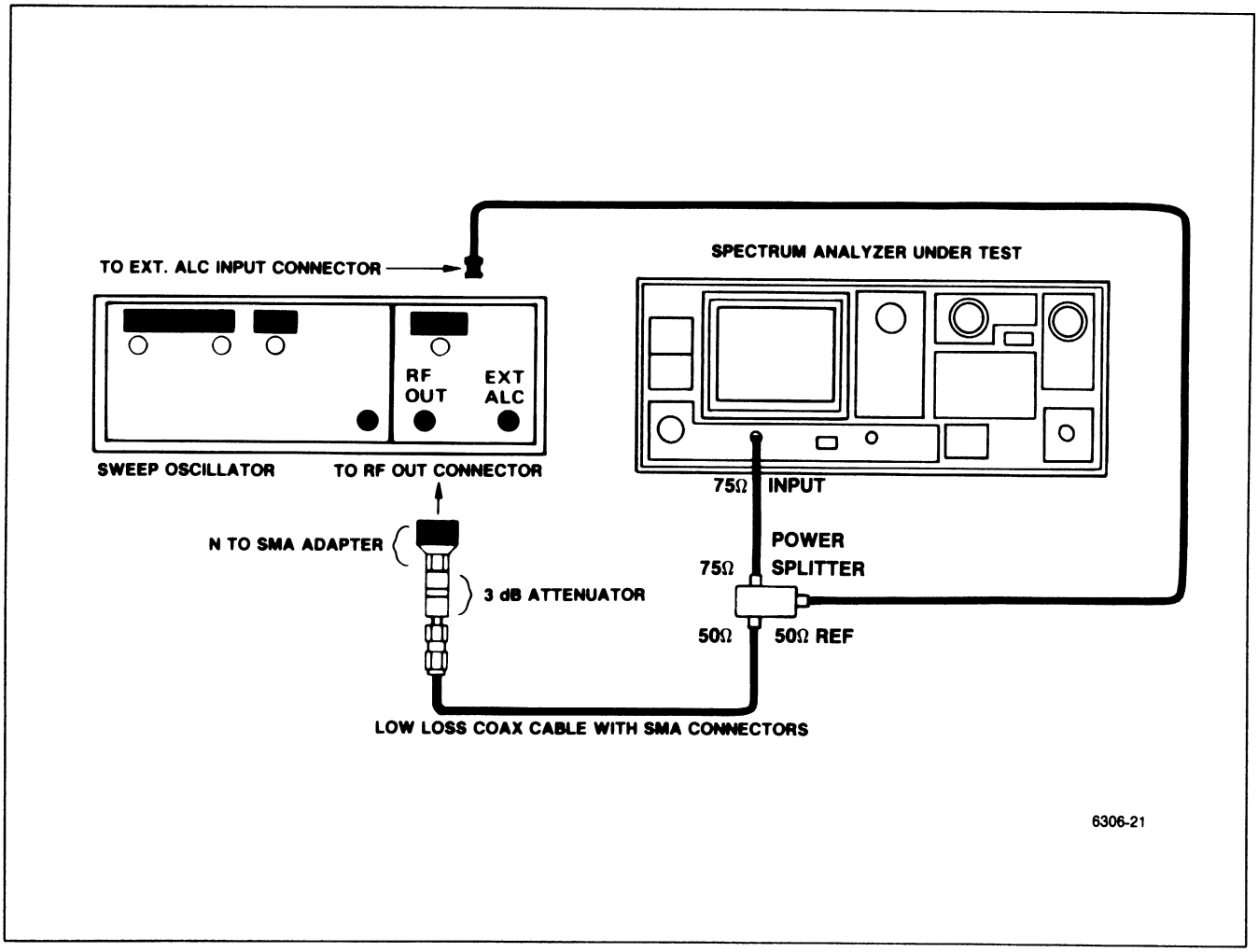


Figure 4-22. Test equipment setup for measuring 0.01 GHz to 1.8 GHz frequency response.

30. Check Option 07 Frequency Response

(Response, about the midpoint between two extremes, measured with 10 dB of RF Attenuation, is ±2 dB from 5 MHz to 1000 MHz)

If the instrument is a rackmount version, with semi-rigid cables to the rear panel (Option 31), frequency response may degrade at the high end of the frequency range.

NOTE

Parts a through f check frequency response from 10 MHz to 1 GHz, and parts g through i check frequency response from 5 MHz to 10 MHz.

a. Connect the test equipment as shown in Figure 4-22.

b. Set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	500 MHz
SPAN/DIV	100 MHz
RESOLUTION	1 MHz
REF LEVEL	−20 dBm
VERTICAL DISPLAY	1 dB/DIV
MAX HOLD	On
MIN RF ATTEN dB	0
TIME/DIV	AUTO
PEAK/AVERAGE	Fully Counterclockwise

c. Set the sweep oscillator controls for a cw output frequency of 500 MHz and an amplitude of approximately −20 dBm).

d. Set the AMPL CAL adjustment for 5 divisions on the Spectrum Analyzer display.

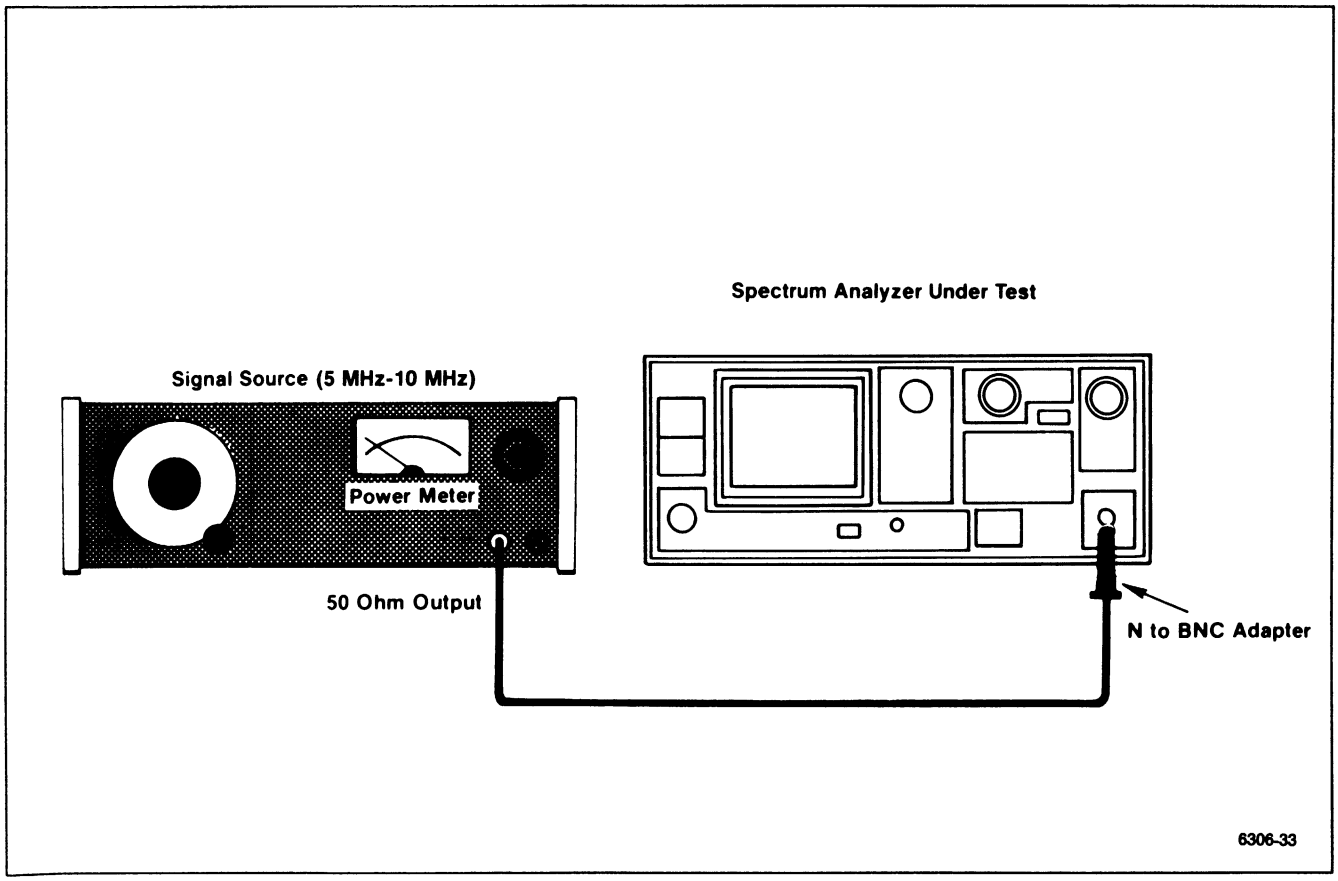


Figure 4-23. Test equipment setup for measuring 100 Hz to 10 MHz frequency response.

e. Reset the sweep oscillator controls for a sweep output from 0.01 GHz—1 GHz. Enable single sweep on the sweep oscillator.

f. Make a note of the highest and lowest peaks for later comparison.

g. Reconnect the test equipment as shown in Figure 4-23. Reset CENTER FREQUENCY to 10 MHz.

h. Set the generator output for −20 dBm at 10 MHz, and set the Spectrum Analyzer controls as follows:

CENTER FREQUENCY	10 MHz
SPAN/DIV	500 kHz
RESOLUTION	1 MHz
REF LEVEL	−18 dBm
VERTICAL DISPLAY	1 dB/DIV
MIN RF ATTEN dB	0
TIME/DIV	AUTO
PEAK/AVERAGE	Fully Counterclockwise

i. Manually tune the Signal Generator towards 5 MHz while simultaneously tuning the CENTER FREQUENCY control to hold the signal at center screen. Make a note of the highest and lowest peaks.

j. Calculate the halfway point between the highest and the lowest peak from the peak data noted in parts f and i.

k. Check that flatness is within ±2 dB from 5 MHz to 1000 MHz.

32. Check Option 42 110 MHz OUT Level

(⩽0 dBm)

a. Tune the Spectrum Analyzer CENTER FREQUENCY to 100 MHz.

b. Connect a signal generator to the RF INPUT. Set the signal generator output frequency to 100 MHz, and output level to −30 dBm.

c. Set the REF LEVEL to −30 dBm, and RF ATTENUATION to 0 dB.

d. Switch the FREQUENCY SPAN/DIV control towards zero span while keeping the signal centered with the CENTER FREQUENCY control. The crt SPAN/DIV readout will indicate 10 ms when zero span is reached.

e. Monitor the 110 MHz OUT with a test spectrum analyzer.

f. Set the CENTER FREQUENCY control to peak the signal displayed on the test spectrum analyzer.

g. Check that the 110 MHz IF OUT output level is ⩽0 dBm typically −8 dBm.

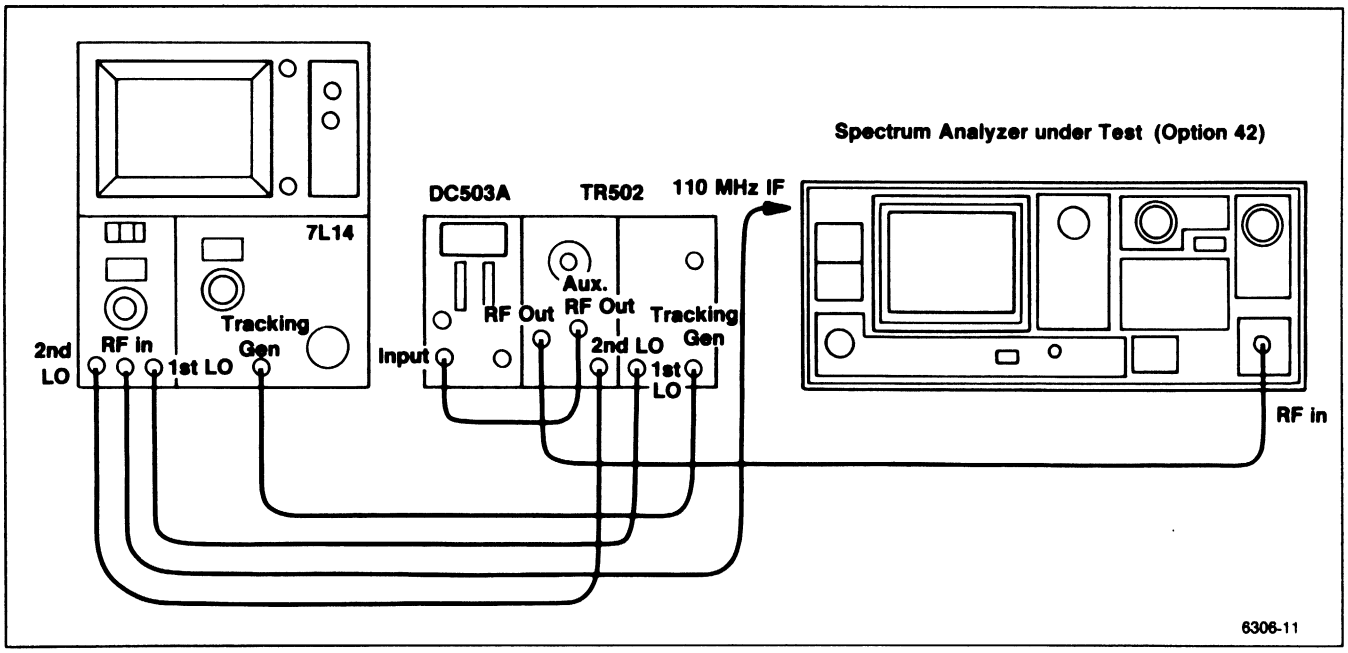


Figure 4-24. Test equipment setup for checking Option 42 frequency characteristics.

33. Check Option 42 110 MHz IF Output Bandwidth, Center Frequency, Bandpass Ripple, and Symmetry About 110 MHz

(Bandwidth: >5 MHz)
(Center Frequency: 108.5 MHz—111.5 MHz)
(Bandpass Ripple: ≤0.5 dB)
(Symmetry: ±1.0 MHz)

a. Connect the test equipment as shown in Figure 4-24

b. Set the test equipment controls as follows:

TR502

Output Level in −dBm	30
Var dB	0
Dot Intensity	Off

7L14

Center Frequency	110 MHz
Freq Span/Div	1 MHz
Hz Resolution	3 MHZ
Reference Level	0 dBm
Vertical Mode	2 dB/Div
Digital Storage	Off
Time/Div	Manual
Triggering	
Source	Free Run
Mode	Norm
Video Filter	On

DC503A

Function	Frequency A
Auto Trig	On
Channel A	
Attn	X1
Coupl	dc
Term	50Ω

Option 42 SPECTRUM ANALYZER

CENTER FREQUENCY	110 MHz
FREQUENCY SPAN/DIV	1 MHz
REF LEVEL	−30 dBm
RESOLUTION BANDWIDTH	1 MHz
VERTICAL DISPLAY	2 dB/DIV
MIN RF ATTEN dB	0

c. Set the 7L14 Time/Div to Mnl and set the dot to center screen with the Manual Scan control.

d. Set the 7L14 Center Frequency control for an indication of 110.0 on the Frequency Counter.

e. Switch the FREQUENCY SPAN/DIV control towards zero span while keeping the signal centered with the CENTER FREQUENCY control. The crt SPAN/DIV readout will indicate 10 ms when zero span is reached.

f. Set the 7L14 Time/Div for a calibrated display, and set the Reference Level and TR502 Var dB for full screen signal.

g. Switch the TR502 Dot Intensity "on", and reset the 7L14 Center Frequency for an indication of 110.0 on the Frequency Counter.

h. Check that the 3 dB bandwidth (1.5 divisions from the peak of the signal) is ≥5 MHz.

i. Check that any ripple present on the display is ≤0.5 dB (0.25 divisions or less).

j. Check that the waveform symmetry is ±1.0 MHz (±1.0 division) by checking that the 3 dB and 6 dB points on the waveform are equidistant from center screen. (The peak of the signal may not be at center screen).

k. Reset the 7L14 Resolution Bandwidth to 0.3 MHz.

l. Set the 7L14 Center Frequency control such that the intensified dot is at the peak of the 7L14 display.

m. Check that the frequency counter indicates a frequency between 108.5 MHz and 111.5 MHz.

GPIB VERIFICATION PROGRAM

This verification program can be used with a TEKTRONIX 4050-Series Computer Terminal to check the functional operation of the GPIB interface in the Spectrum Analyzer. All interface lines are verified as well as all interface messages, except those for parallel poll. In addition, the instrument interface is checked for operation on other primary addresses, as well as the talk-only and listen-only modes.

The program is written in TEKTRONIX 4050 BASIC, and is divided into individual tests, each for a specific interface line, message, or function. The tests start on even 1000 line numbers to allow easy modification of the program.

The following describes the function of each test in the program.

Lines 1-5000: Interfaces to user definable keys for recovery from a failed test.

Lines 5000-6000: Inputs the primary address of the Spectrum Analyzer under test (1 should be used).

Lines 6000-7000: ID query response test. The instrument must be able to talk and listen, to send out its ID? response and manipulate all eight of the DIO Lines for the test to be successful.

Lines 7000-8000: Local lock-out test. Tests correct operation of the interface message that should disable all programmable front-panel controls.

Lines 8000-9000: Go to LOCAL test. Tests correct operation of the interface message that should enable all front-panel controls.

Lines 9000-10000: Group Execute Trigger test. Checks that a GET message does cause the Spectrum Analyzer to abort the present sweep and re-arm the trigger, causing a sweep to start and end, sending out an End-of-Sweep SRQ. Thus, the SRQ line and GET message are verified.

Lines 10000-11000: Selected Device Clear Test. This test verifies that an SDC message resets the Spectrum Analyzer's GPIB output buffer clearing out it's ID? response.

Lines 11000-12000: Device clear test. This test is identical to the selected device clear test, except the universal command DCL is used instead.

Lines 12000-13000: Addressed as listener, talker test. This test checks that the microprocessor correctly recognizes that the GPIA chip has been addressed to listen or talk, and sends the appropriate character to the crt readout (L or T).

Lines 13000-14000: Serial Poll test. This checks correct operation of the serial poll enable (SPE) and serial poll disable (SPD) interface messages. The status byte is read, and if anything other than ordinary operation is indicated, the instrument fails the test.

Lines 14000-15000: GPIB rear panel switch test. All five primary address switches are checked for correct operation. Three subroutines are called in the process of testing one address switch. The first two send a formatted message to the 4050 display, and the third performs the address switch test.

Lines 15000-16000: Line feed or EOI switch test. Checks for correct selection of line feed as a termination when selected by this switch by sending an ID? terminated only by a line feed.

Lines 16000-17000: Talk-only mode test. When selected, this mode should cause the instrument to send a SET? response and (optionally) a CURVE? response whenever the RESET-TO-LOCAL button is pressed. The string received from the instrument is thus examined for existence of a portion of the correct SET? response after the RESET-TO-LOCAL button is pressed.

Lines 17000-18000: Listen-only mode test. When selected, this mode will cause the instrument to respond to any message on the bus, since it is always addressed to listen. The command REF 0 is sent to the bus without addressing the instrument, then the listen-only mode is deselected and the instrument interrogated to see if it did respond to the REF command while in the listen-only mode.

Lines 18000-19000: Interface clean (and Remote Enable) test. This IFC line on the GPIB will unaddress the instrument's interface. This is verified by noting that the L is not present in the crt readout, indicating that the IFC line worked; also the REN line will be unasserted when the end statement is executed (except for some early 4052 and 4054's). Thus, a front panel in the local mode indicates that the REN line was successfully unasserted. (Evidence it was asserted is that the instrument was able to execute commands sent to it by previous tests.)

Lines 19000-end: Utility routines. Rear panel interface switch test text routine puts headers on the interface switch test display. The rear panel test text routine tells the operator what to do after changing the address switches. Test address switch acquires an ID? response from the instrument on its new address during the address switch test.

The SRQ handler will handle SRQ's that occur, although none would be expected, except the power-up SRQ. (The end of sweep SRQ during the GET test is handled by another SRQ handler.)

Delay Generator generates delays for other tests. The Failure Decision Handler allows the program to be restarted with the user-definable keys if any test fails.

```
1 GO TO 5000
4 B2=1
5 RETURN
20 B2=5
21 RETURN
5000 REM *** 275XP GPIB VERIFICATION PROGRAM ***
5030 INIT
5040 ON SRQ THEN 19280
5050 DIM V$(400),W$(400)
5060 I7=0
5070 PAGE
5080 PRINT "JJJENTER 275XP'S PRIMARY ADDRESS  (DEFAULT = 1) ";
5090 INPUT T$
5100 IF T$<>"" THEN 5130
5110 A1=1
5120 GO TO 5180
5130 A1=VAL(T$)
5140 IF A1>0 AND A1<31 THEN 5180
5150 PRINT "JJJGERROR!! ";A1;" IS NOT A VALID ADDRESS";
5160 PRINT " ONLY 0 THRU 30 ARE VALID ADDRESSESKK"
5170 GO TO 5080
5180 PAGE
5190 REM
5200 REM
5210 REM
5220 REM
5230 REM
6000 REM ***"ID" QUERY RESPONSE ***
6010 PRINT "*** ""ID"" QUERY RESPONSE ***"
6020 PRINT @A1:"INIT;ID?;SIG"
6030 INPUT @A1:T$
6040 V$=SEG(T$,1,9)
6050 IF V$="ID TEK/275" THEN 6080
6060 PRINT "JJJ*** ""ID"" QUERY RESPONSE *** FAIL ***G"
6070 GO TO 19530
6080 WBYTE @32+A1:64,128,-127
6090 PRINT @A1:"WFM ENC:BIN;CUR?"
6100 PRINT @37,0:37,255,255
6110 INPUT %A1:T$
6120 WBYTE @64+A1:
6130 RBYTE R,R,R,T6
6140 WBYTE @95:
6150 IF R=>128 AND T6<128 THEN 7000
6160 PRINT "JJJ*** DIO8 TEST *** FAIL ***G"
6170 GO TO 19530
6180 REM
6190 REM
6200 REM
6210 REM
6220 REM
7000 REM *** LOCAL LOCK-OUT.....LLO ***
7010 PRINT "*** LOCAL LOCK-OUT.....LLO ***"
7020 WBYTE @32+A1,17:
7030 PRINT @A1:"SET?"
```

```
7040 INPUT @A1:V$
7050 PRINT "_|_|275XP IN LOCAL LOCK-OUT MODE (LLO)"
7060 PRINT "_|_|ATTEMPT TO USE 275XP CONTROLS"
7070 PRINT "_|_|PRESS RETURN <CR> WHEN DONE ";
7080 INPUT T$
7090 PRINT @A1:"SET?"
7100 INPUT @A1:W$
7110 IF W$<>V$ THEN 7130
7120 GO TO 8000
7130 PRINT "J*** LOCAL LOCK-OUT.....LLO *** FAIL ***G"
7140 GO TO 19530
7150 REM
7160 REM
7170 REM
7180 REM
7190 REM
8000 REM *** GO TO LOCAL.....GTL ***
8010 PRINT @A1:"INIT;TIM?"
8020 INPUT @A1:R
8030 PRINT @A1:"TIM INC"
8040 PRINT "**** GO TO LOCAL.....GTL ***"
8050 WBYTE @32+A1,1:
8060 PRINT @A1:"TIM?"
8070 INPUT @A1:T6
8080 IF R<>T6 THEN 8100
8090 GO TO 9000
8100 PRINT "J**** GO TO LOCAL.....GTL *** FAIL ***G"
8110 GO TO 19530
8120 REM
8130 REM
8140 REM
8150 REM
8160 REM
9000 REM *** GROUP EXECUTE TRIGGER.....GET ***
9010 PRINT "**** GROUP EXECUTE TRIGGER...GET ***"
9020 ON SRQ THEN 9120
9030 I7=0
9040 PRINT @A1:"INIT;TIM 100M;SIG;EOS ON"
9050 WBYTE @32+A1,8:
9060 T6=3
9070 GOSUB 19390
9080 PRINT @A1:"EOS OFF"
9090 IF I7<>1 THEN 9150
9100 ON SRQ THEN 19280
9110 GO TO 10000
9120 WBYTE @20:
9130 I7=1
9140 RETURN
9150 PRINT "GROUP EXECUTE TRIGGER...GET *** FAIL ***G"
9160 GO TO 19530
9170 REM
9180 REM
9190 REM
9200 REM
9210 REM
10000 REM *** SELECTED DEVICE CLEAR...SDC ***
10010 PRINT "**** SELECTED DEVICE CLEAR...SDC ***"
10020 PRINT @A1:"ID?"
10030 WBYTE @32+A1,4:
10040 WBYTE @64+A1:
```

```
10050 RBYTE R
10060 IF ABS (R)<>255 THEN 10080
10070 GO TO 11000
10080 PRINT "*** SELECTED DEVICE CLEAR.....SDC *** FAIL ***G"
10090 GO TO 19530
10100 REM
10110 REM
10120 REM
10130 REM
10140 REM
11000 REM *** DEVICE CLEAR.....DCL ***
11010 PRINT "*** DEVICE CLEAR.....DCL ***"
11020 PRINT @A1:"ID?"
11030 WBYTE @20:
11040 WBYTE @64+A1:
11050 RBYTE R
11060 IF ABS (R)<>255 THEN 11080
11070 GO TO 12000
11080 PRINT "*** DEVICE CLEAR.....DCL *** FAIL ***G"
11090 GO TO 19530
11100 REM
11110 REM
11120 REM
11130 REM
11140 REM
12000 REM **  ADDRESSED AS LISTENER, TALKER ***
12010 PRINT "*** 275XP ADDRESSED AS LISTENER..***"
12020 WBYTE @32+A1:76,79,82,68,79,-63
12030 T6=1
12040 GOSUB 19390
12050 INPUT @A1:V$
12060 T$=SEG (V$,16,1)
12070 IF T$="L" THEN 12100
12080 PRINT "J*** 275XP ADDRESSED AS LISTENER *** FAIL ***G"
12090 GO TO 19530
12100 PRINT "*** 275XP ADDRESSED AS TALKER....***"
12110 PRINT @A1:"INIT;TIM 50M;SIG;SIG;WAI;LORDO?"
12120 INPUT @A1:V$
12130 T$=SEG (V$,16,1)
12140 IF T$="T" THEN 13000
12150 PRINT "*** 275XP ADDRESSED AS TALKER *** FAIL ***"
12160 GO TO 19530
12170 REM
12180 REM
12190 REM
12200 REM
12210 REM
13000 REM *** SERIAL POLL ***
13010 PRINT "*** SERIAL POLL.....SPD/SPE ***"
13020 WBYTE @95,63,24,64+A1:
13030 RBYTE R
13040 WBYTE @95,25:
13050 IF R=0 OR R=16 THEN 13080
13060 PRINT "J*** SERIAL POLL *** FAIL ***G"
13070 GO TO 19530
13080 T6=3
13090 GOSUB 19390
13100 REM
13110 REM
13120 REM
```

```
13130 REM
13140 REM
14000 REM *** GPIB INTERFACE REAR PANEL SWITCH TEST ***
14010 PAGE
14011 WBYTE @32+A1, 20, 63:
14020 A1=2
14030 GOSUB 19000
14040 PRINT "  0 |_0 |_0 |_0 0 0 1 0"
14050 GOSUB 19070
14060 GOSUB 19190
14070 PAGE
14080 A1=4
14090 GOSUB 19000
14100 PRINT "  0 |_0 |_0 |_0 0 1 0 0"
14110 GOSUB 19070
14120 GOSUB 19190
14130 PAGE
14140 A1=8
14150 GOSUB 19000
14160 PRINT "  0 |_0 |_0 |_0 1 0 0 0"
14170 GOSUB 19070
14180 GOSUB 19190
14190 PAGE
14200 A1=16
14210 GOSUB 19000
14220 PRINT "  0 |_0 |_0 |_1 0 0 0 0"
14230 GOSUB 19070
14240 GOSUB 19190
14250 REM
14260 REM
14270 REM
14280 REM
14290 REM
15000 REM *** "LF" OR "EOI" SWITCH ***
15010 PAGE
15020 A1=1
15030 GOSUB 19000
15040 PRINT "  0 |_0 |_  1 |_0 0 0 0 1"
15050 GOSUB 19070
15060 PRINT "J_JTESTING" "LF" "OR" "EOI" "SWITCH"
15070 GOSUB 19190
15080 WBYTE @32+A1:73,68,63,10
15090 INPUT @A1:T$
15100 T$=SEG (T$,1,9)
15110 IF T$="ID TEK/275" THEN 15140
15120 PRINT "J""LF" "OR" "EOI" "SWITCH *** FAIL ***G"
15130 GO TO 19530
15140 T6=2
15150 GOSUB 19390
15160 REM
15170 REM
15180 REM
15190 REM
15200 REM
16000 REM *** TALK ONLY MODE ***
16010 PAGE
16020 GOSUB 19000
16030 PRINT "  0  |_ 1  |_0 |_0 0 0 0 1"
16040 GOSUB 19070
16050 PRINT "J_J_JTESTING TALK ONLY"
```

```
16060 INPUT @A1:V$
16070 I7=POS (V$,"FINE OFF",1)
16080 IF I7<>0 THEN 17000
16090 PRINT "JJJTALK ONLY MODE *** FAIL ***G"
16100 GO TO 19530
16110 REM
16120 REM
16130 REM
16140 REM
16150 REM
17000 REM *** LISTEN ONLY MODE ***
17010 PAGE
17020 GOSUB 19000
17030 PRINT "  1 I  0 I  0  I 0 0 0 0 1"
17040 GOSUB 19070
17050 PRINT "JJJTESTING LISTEN ONLY"
17060 PRINT @A1:"INI"
17070 T6=0.5
17080 GOSUB 19390
17090 WBYTE 82,69,70,32,-48
17100 PAGE
17110 GOSUB 19000
17120 PRINT "  0 I  0 I  0 I 0 0 0 0 1"
17130 GOSUB 19070
17140 PRINT @A1:"REF?"
17150 INPUT @A1:V$
17160 IF V$<>"REFLVL +0.0" THEN 17180
17170 GO TO 18000
17180 PRINT "JJJLISTEN ONLY MODE *** FAIL ***G"
17190 GO TO 19530
17200 REM
17210 REM
17220 REM
17230 REM
17240 REM
18000 REM *** INTERFACE CLEAR AND REMOTE ENABLE TEST.....IFC & REN ***
18010 PAGE
18020 PRINT "JJJTESTING IFC (INTERFACE CLEAR), AND REN (REMOTE ENABLE)"
18030 WBYTE @32+A1:
18040 T6=3
18050 GOSUB 19390
18060 PRINT "JJCHECK THE 275XP CRT, FOR AN ""L"" BETWEEN THE VERTICAL"
18070 PRINT "DISPLAY AND THE MIN RF ATTEN READOUTS."
18080 PRINT "JPRESS RETURN TO CONTINUE.";
18090 INPUT P$
18100 INIT
18110 PRINT "JIF AN" "L" "IS STILL PRESENT, THE IFC LINE IS FAULTY,"
18120 PRINT "IF THE" "L" "VANISHED, IFC TESTED OK."
18130 PRINT "JJCHECK ALSO THE 275XP FRONT PANEL FOR PROPER LOCAL CONTROL"
18140 PRI "IF THE FRONT PANEL IS LOCKED OUT, THE REN LINE IS FAULTY, IF"
18150 PRINT "NOT, REN TESTED OK"
18160 PRINT "JJJGPIB VERIFICATION COMPLETEG"
18170 END
18180 REM
18190 REM
18200 REM
19000 REM *** REAR PANEL INTERFACE SWITCH TEST TEXT ROUTINE ***
19010 PRINT "SET GPIB ADDRESS SWITCHES TO:"
19020 PRINT "JJLISTENITALKILF ORI ADDRESS"
19030 PRINT " ONLYIONLYIEOIII16 8 4 2 1"
```

```
19040 PRINT "------|----|-----|----------"
19050 RETURN
19060 REM
19070 REM *** REAR PANEL TEST TEXT ROUTINE ***
19080 PRINT "JJAFTER CHANGING THE SWITCHES, ";
19090 PRINT "PRESS THE REMOTE/LOCAL BUTTON ONCEJJ"
19100 PRINT "|(NOTE: IF YOU GET A GPIB INTERFACE ERROR MESSAGE,"
19110 PRINT "|      IT MEANS THAT THE SWITCH(ES) WERE'NT "
19120 PRINT "|      READ CORRECTLY. TO RE-TEST, TYPE"
19130 PRINT "|      ""RUN"" FOLLOWED BY THE LINE NUMBER IN THE"
19140 PRINT "|      ERROR MESSAGE) "
19150 PRINT "JJ|PRESS RETURN <CR> WHEN DONE ";
19160 INPUT T$
19170 RETURN
19180 REM
19190 REM *** TEST ADDRESS SWITCH ***
19200 PRINT @A1:"ID?"
19210 INPUT @A1:T$
19220 T$=SEG (T$,1,9)
19230 IF T$="ID TEK/275X" THEN 19260
19240 PRINT "ADDRESS SWITCH TEST FAIL"
19250 GO TO 19530
19260 RETURN
19270 REM
19280 REM *** SRQ HANDLER ***
19290 T6=3
19300 GOSUB 19390
19310 POLL Z1,Z1;A1
19320 PRINT @A1:"ERR?"
19330 INPUT @A1:S$
19340 PRINT "GGAN INTERRUPT OCCURRED ON THE BUS, THE 275XP RETURNS ";S$
19350 PRINT "JPRESS RETURN <CR> TO CONTINUE ";
19360 INPUT T$
19370 RETURN
19380 REM
19390 REM *** DELAY GENERATOR ***
19410 REM *** T6 GIVEN IN SEC (GLOBAL) *** I9 SCRATCH ***
19420 IF T6<0 THEN 19510
19430 IF RND (0)>0.5 THEN 19490
19440 REM *** 4051 ***
19450 T6=T6*220
19460 FOR I9=1 TO T6
19470 NEXT I9
19480 GO TO 19510
19490 REM *** 4052
19500 CALL "WAIT",T6
19510 T6=0
19520 RETURN
19530 REM **** FAILURE DECISION HANDLER ****
19540 PRINT "JJISELECT A UDK:"
19550 PRINT "|  (1) RE-START"
19560 PRINT "|  (5) END"
19570 SET KEY
19580 B2=0
19590 IF B2<>1 AND B2<>5 THEN 19590
19600 IF B2=5 THEN 19630
19610 PAGE
19620 GO TO 6000
19630 END
```

ADJUSTMENT PROCEDURE

Introduction

If the instrument performance is not within specified requirements for a particular characteristic, determine the cause, repair if necessary, then use the appropriate adjustment procedure to return the instrument operation to performance specification. After any adjustment, verify performance by repeating that part of the Performance Check.

Allow the instrument to warm up for at least one hour, in an ambient temperature of +20° C to +30° C before making any adjustments. Waveform illustrations in the adjustment procedure may be idealized and should not be construed as being representative of specification tolerances.

Adjustment steps that interact are flagged and references made to the affected circuit or steps.

CAUTION

STATIC DISCHARGE CAN DAMAGE MANY SEMICONDUCTOR COMPONENTS USED IN THIS INSTRUMENT.

Many semiconductor components, especially MOS types, can be damaged by static discharge. Damage may not be catastrophic and, therefore, not immediately apparent. It usually appears as a degradation of the semiconductor characteristics. Devices that are particularly susceptible are: MOS, CMOS, JFETs, and high impedance operational amplifiers (FET input stages.) The damaged parts may operate within accepted limits over a short period, but their reliability will have been severely impaired. Damage can be significantly reduced by observing the following precautions.

1. Handle static-sensitive components or circuit assemblies at or on a static-free surface. Work station areas should contain a static-free bench cover or work plane such as conductive polyethylene sheeting and a grounding wrist strap. The work plane should be connected to earth ground.

2. All test equipment, accessories, and soldering tools should be connected to earth ground.

3. Minimize handling by keeping the components in their original containers until ready for use. Minimize the removal and installation of semiconductors from their circuit boards.

4. Hold the IC devices by their body rather than the terminals.

5. Use containers made of conductive material or filled with conductive material for storage and transportation. Avoid using ordinary plastic containers. Any static sensitive part or assembly (circuit board) that is to be returned to Tektronix, Inc., should be packaged in its original container or one with anti-static packaging material.

Equipment Required

Table 5-1 lists some test equipment and test fixtures recommended for the adjustment procedure. Test equipment listed in Table 5-1 together with those listed in Table 4-1 in Section 4, Performance Check are required for the adjustment procedure. The characteristics specified are the minimum required for the checks. Substitute equipment must meet or exceed these characteristics.

Table 5-1
EQUIPMENT REQUIRED

Equipment or Test Fixture	Characteristics	Recommendation and Use
Return Loss Bridge	10 MHz to 1 GHz, 50 Ω	Wiltron VSWR Bridge Model 62N50
Attenuator (3 dB miniature)	Frequency, to 5 GHz; connectors 5 mm	Weinchel Model 4M, Tektronix Part No. 015-1053-00
Autotransformer	Capable of varying line voltage from 90 Vac to 130 Vac	General Radio Variac Type W10MT3
Digital Multimeter	10 μV to 350 Vdc	TEKTRONIX DM 501A or DM 502A
Dc Block		Tektronix Part No. 015-0221-00
Adapter (Sealectro male to male)		Tektronix Part 103-0098-00
Adapter (bnc female to Sealectro male)		Tektronix Part No. 103-0180-00
Three Extension Cables (Sealectro female to Sealectro male)		Tektronix Part No. 175-2902-00
Adapter (bnc to Sealectro)		Tektronix Part No. 175-2412-00
Adapter (bnc female to sma male)		Tektronix Part No. 015-1018-00
Cable (20"), Tip Plugs to bnc		Tektronix Part No. 175-1178-00
Coaxial Cable (8")		Tektronix Part No. 012-0208-00
50 Ω Terminator		Tektronix Part No. 011-0049-01
Screwdriver, Tuning		Tektronix Part No. 003-0675-00
Alignment Tool		Tektronix Part No. 003-0968-00
Screwdriver, Flat, 6" with 1/8" Tip		
Screwdriver, Phillips No. 1		
Allen Wrenches (3), 3/32", 5/64", 7/64"		
Service Kit (Extender Boards)[a]		Tektronix Part No. 672-0865-01

ADJUSTMENT PROCEDURE

PREPARATION

CAUTION

Do not place the instrument on its front panel as this may cause damage to the front-panel knobs.

Remove the cabinet as follows:

1. Remove the twelve torque screws holding the rear-panel casting, and pull the casting from the instrument.

2. Remove the eight screws holding on the feet, and the eight screws holding on the handles.

3. Pull the cabinet from the rear of the instrument.

4. Place the instrument on the bench and reconnect the power cord.

Some circuit boards or assemblies must be removed and placed on extenders to gain access to some test points or adjustments. In some cases this will also necessitate removing the airbaffle attached to the left siderail. Turn the power off before removing the assembly.

[a] This kit is part of the Service Kit 006-3286-01, listed in the Maintenance Section.

1. Adjust Low Voltage Power Supply

(R6028 and R6061 on the Power Supply board)

This high-efficiency power supply uses an internal oscillator with a frequency of 66 kHz. The frequency adjustment is normally required only after replacing oscillator components; therefore, Part I is the normal adjustment and check procedure, Part II of this step should only be required after repair of the assembly.

WARNING

Since the Spectrum Analyzer uses a high efficiency power supply, with the primary ground potential different from chassis or earth ground, an isolation transformer, with a 1:1 turns ratio and a 500 VA minimum rating, should be used between the power source and the Spectrum Analyzer power input receptacle.

The transformer must have a three-wire input and output connector with ground through the input and output. Stancor GIS21000 is an example of a suitable transformer. A jumper should also be connected between the primary ground side to chassis ground (emitter of Q2061 and the ground terminal of the input filter FL301.)

If the power supply is separated from the instrument and operated on the bench, hazardous potentials exist within the supply for several seconds after power is disconnected. This is due to the slow discharge of capacitors C6101 and C6111. A relaxation oscillator lights DS5112 (next to C6111) when the potential exceeds 80 V.

Part I
Check and Adjust Low Voltages

a. Connect a voltage-variable transformer in line with the Spectrum Analyzer power input and set the transformer for 117 Vac. Remove the cover over the Z-Axis and Sweep boards.

b. Monitor the +15 V test point on the Z-Axis board (Figure 5-1b) with a voltmeter (DVM).

c. Remove the Power Supply cover screw located below the 10 MHz IF OUTPUT jack on the rear panel (see Figure 5-1a). This will provide access to the +5 V supply adjustment, R6028.

d. Adjust R6028 for +5 V on the voltmeter. R6028 is accessed by inserting a narrow-bit screwdriver through the screw hole that was removed in part c of this step.

e. Vary the input voltage from 90 Vac to 132 Vac. Check that the +15 V supply remains regulated, and input power does not exceed 210 W.

f. Check the other supply voltages at the test points indicated in Figure 5-1b, against tolerances listed in Table 5-2.

Table 5-2
POWER SUPPLY TOLERANCES

Supply	Tolerance
+9 V	+8.92 V to +10.1 V
−5 V	−4.96 V to −5.05 V
−7 V	−7 V to −8.5 V
−15 V	−14.84 V to −15.16 V
+5 V	+4.73 V to +5.23 V
+17 V	+16.81 V to +18.6 V
+100 V	+95 V to +105 V
+300 V	+280 V to +310 V

g. Remove the voltage-variable transformer and reconnect the Spectrum Analyzer directly to the power source.

Part II
Adjusting Power Supply Oscillator Frequency

a. Remove the Power Supply module, as described in the Maintenance section, then remove the Power Supply module cover and disconnect P3045.

b. Plug the power cord into the power input receptacle and connect it to a suitable power source (115 Vac or 230 Vac, depending on the position of the LINE SELECTOR SWITCH).

c. Use a plastic or insulated tuning tool or equivalent, to insert between the two on/off power switches (S300) to close these switches (Figure 5-1a).

d. Connect a test oscilloscope probe, with a deflection sensitivity of 5 V/div and sweep rate of 10 μs/div to TP6053 (Figure 5-1a). Note the amplitude of the output waveform, of the oscillator U6059, is approximately 10 V.

e. Adjust R6061 (Oscillator Freq Adj) for a waveform period of 15 μs (66 kHz).

f. Reconnect P3045, replace the Power Supply module cover, and re-install the module on the Spectrum Analyzer.

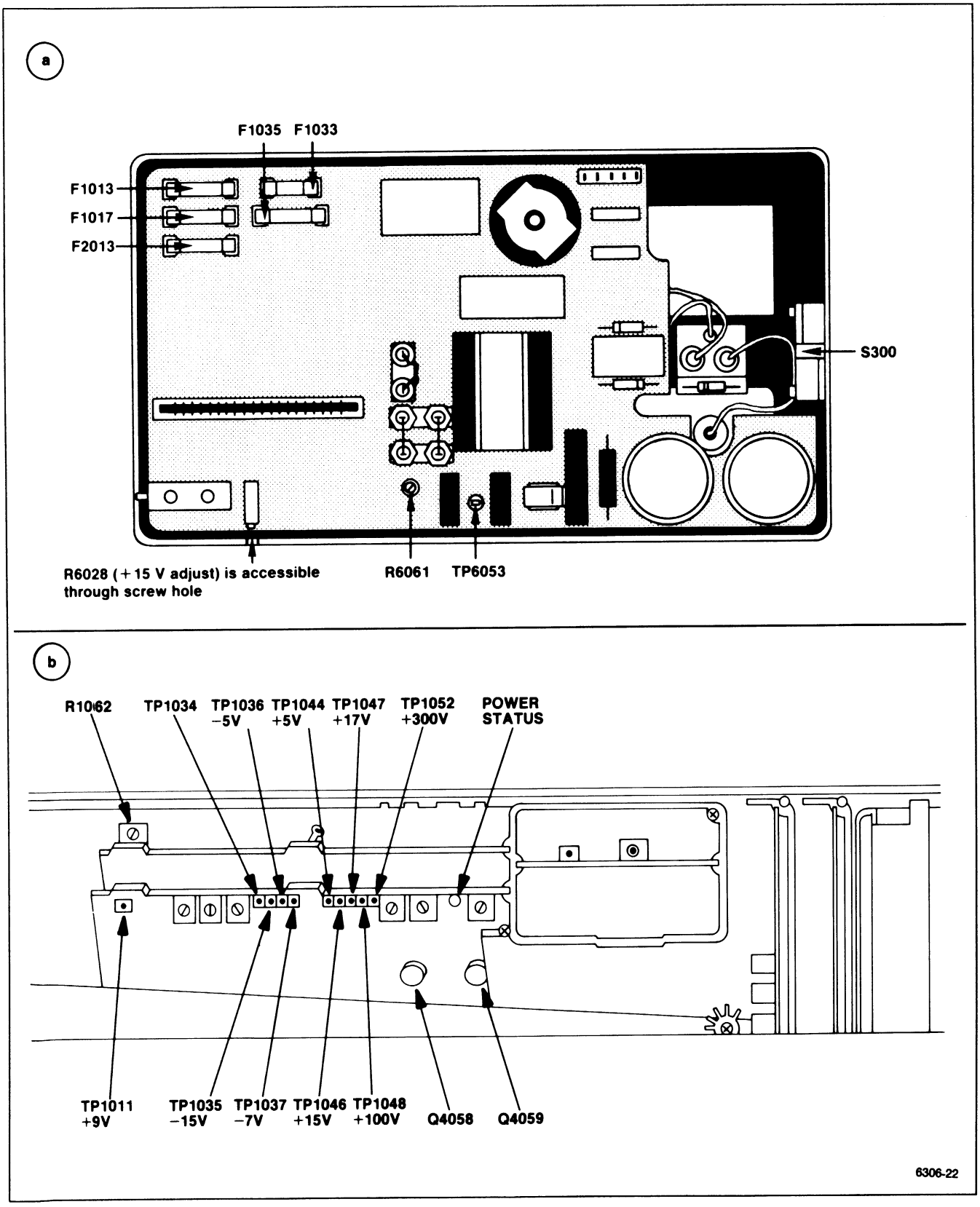


Figure 5-1. Low voltage power supply adjustments.

2. Adjust Z-Axis and High Voltage Circuits

(R1021, R1027, R1030, R1051, and R1058 on the Z-Axis board; R2040 and R3033 on the High Voltage board)

a. Switch POWER off and preset the following Spectrum Analyzer controls:

INTENSITY	Fully Counterclockwise
TIME/DIV	MNL
MANUAL SCAN	Midrange

b. Remove the cover over the Z-Axis and Sweep boards. Set the Intensity Limit R1027, on the Z-Axis board (Figure 5-2) fully counterclockwise and Crt Bias R2040, on the High Voltage board (Figure 5-3) fully clockwise.

c. Switch POWER on and, after the power-up state has stabilized, change the Vertical Display mode to 2 dB/DIV. Deactivate READOUT, VIEW A, and VIEW B.

d. Adjust Crt Bias as follows:

(1) Using a voltmeter in the 20 V range, measure and record the collector voltage of Q4058 or Q4059 on the Z-Axis board (See Figure 5-1b.)

(2) Turn the INTENSITY clockwise until a crt beam dot appears on screen.

(3) Focus the dot by adjusting R3033 on the High Voltage board (Figure 5-3) for the smallest round dot.

(4) Set the INTENSITY for a collector voltage 5.5 V higher than the voltage noted in part d, subpart 1.

(5) Use the non-metallic screwdriver to adjust Crt Bias, R2040, counterclockwise until the crt beam is visible, then clockwise until the beam dot just extinguishes, with the screen shaded. (If no dot appears, with the adjustment fully counterclockwise, this will be the bias setting.)

(6) Turn the INTENSITY clockwise until a dot is visible then defocus the dot with the Focus adjustment, R3033. Adjust Astigmatism R1058 (Figure 5-2) for a round dot then refocus with R3033 for the smallest and sharpest dot.

(7) Turn the INTENSITY counterclockwise until the dot just disappears, and again measure the collector voltage at Q4058 or Q4059. Voltage should equal or exceed that set in part d, subpart 4. If the voltage is less, repeat the procedure for setting Crt bias.

e. Adjust the Crt cathode current as follows:

(1) Switch POWER off, then remove P4036 (Figure 5-3) on the High Voltage board. Turn INTENSITY fully clockwise, MANUAL SCAN fully counterclockwise, and ensure that the TIME/DIV is in the MNL position. Set the Intensity Limit R1027, on the Z-Axis board, (Figure 5-2) fully clockwise.

(2) Connect the voltmeter between TP4028 (Figure 5-3) and the ground lug on the crt shield.

(3) Switch POWER back on. After the instrument initializes, activate 2 dB/DIV and switch Digital Storage off.

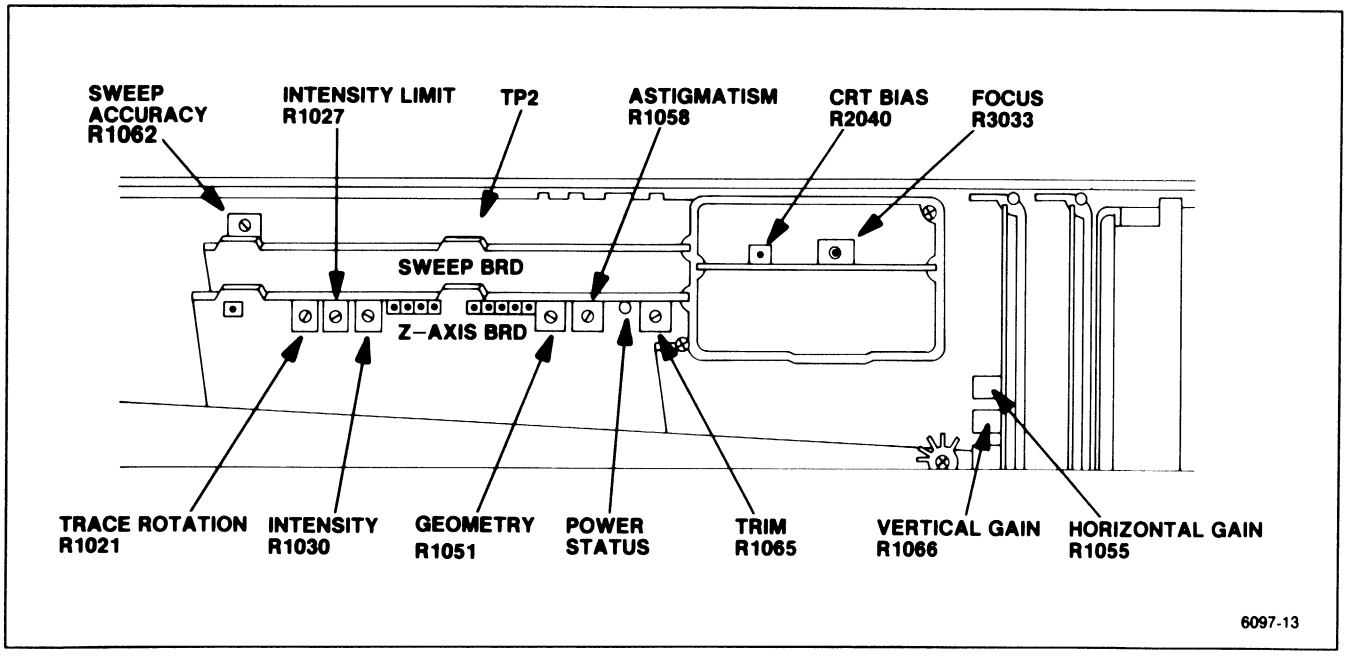


Figure 5-2. Crt display adjustment and test point locations.

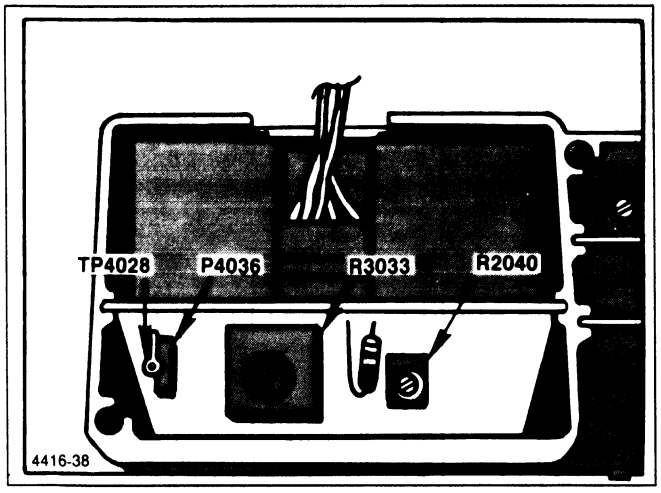


Figure 5-3. Adjustment and test point locations on High Voltage module.

(4) Adjust Intensity Limit R1027 (Figure 5-2) for a voltage reading of 0.9 V at TP4028.

(5) Switch POWER off and re-install the jumper P4036 on the High Voltage board. Turn POWER on and adjust the INTENSITY for normal viewing.

f. Apply the CAL OUT signal to the RF INPUT and set the Spectrum Analyzer controls as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	10 MHz
AUTO RESOLN	On
REF LEVEL	−20 dBm
MIN RF ATTEN	0 dB
VERTICAL DISPLAY	2 dB/DIV
NARROW VIDEO FILTER	On
VIEW A and VIEW B	Off
TIME/DIV	AUTO
TRIGGERING	FREE RUN

g. Activate ZERO SPAN and adjust REFERENCE LEVEL until the trace is approximately mid-screen; then adjust the Trace Rotation R1021 (Figure 5-2) so the trace is aligned with the graticule lines.

h. Activate VIEW A and VIEW B then use the PEAK/AVERAGE cursor, positioned at the top then bottom of the screen, as a reference line to adjust Geometry R1051 (Figure 5-2) for the straightest trace at top and bottom of the screen.

i. Change the REF LEVEL to position the trace within the graticule area with the Vertical Display mode of 2 dB/DIV. Adjust INTENSITY so the trace is just visible.

j. Adjust Intensity R1030 (Figure 5-2) so the brightness of the readout characters is slightly higher than the trace. Readout characters should be just visible after the trace has disappeared. This ratio provides the best setting for photograph purposes. Disconnect CAL OUT signal from the RF INPUT.

3. Adjust Deflection Amplifier Gain and Frequency Response

(C4057, C4061, C5021, C5104, R1055, and R1066 on the Deflection Amplifiers board)

a. Connect the test equipment as shown in Figure 5-4. Set the TIME/DIV to 1 ms. Position the trace on the bottom graticule line.

b. Set the Function generator controls for a 500 Hz sinewave signal, with an amplitude of 0 to +4 V. Connect a jumper between pins 1 and 5 (Ext Video Select and Ground respectively) on the ACCESSORIES connector. Deactivate VIEW A and VIEW B, and set TRIGGERING to INT.

c. Adjust Vert Gain, R1066 (Figure 5-2) for a full screen display.

d. Disconnect the 500 Hz signal from the MARKER/VIDEO input. Remove the jumper between pins 1 and 5 of the ACCESSORIES connector. Reset Triggering to FREE RUN.

e. Set TIME/DIV to MNL. Monitor TP2 on the Sweep board (Figure 5-2) with a voltmeter (Digital Multimeter). Set the MANUAL SCAN control for 0.0 V reading on the voltmeter (TP2). Set the horizontal POSITION control to center the CRT beam (dot).

f. Reset the MANUAL SCAN control for a reading of +5 V at TP2.

g. Adjust Horiz Gain, R1055 (Figure 5-2) to position the crt beam to the right graticule edge (10th graticule line).

h. Reset the MANUAL SCAN control such that crt beam (dot) moves to the left edge of the graticule and check that the voltage at TP2 is now −5.0 V ±0.2 V.

i. Disconnect the voltmeter, set TIME/DIV to AUTO, change the test oscilloscope to Ext Trigger, and apply the signal at TP1038 on the Crt Readout board (Figure 5-5) to the test oscilloscope Ext Trigger input. Set the test oscilloscope Time/Div to 2 μs.

j. Set the Spectrum Analyzer controls for a triggered sweep, then switch the sweep off by activating SINGLE SWEEP, and ensure READ OUT is on.

k. Monitor the collectors of Q1031 and Q1024, on the Deflection Amplifier board, with the test oscilloscope. See Figure 5-6 for the locations of Q1031 and Q1024.

l. Adjust C5021 for the best frequency response (no overshoot or rolloff) as viewed on the test oscilloscope.

m. Monitor the collectors of Q1043 and Q1049, on the Deflection Amplifier board, with test oscilloscope.

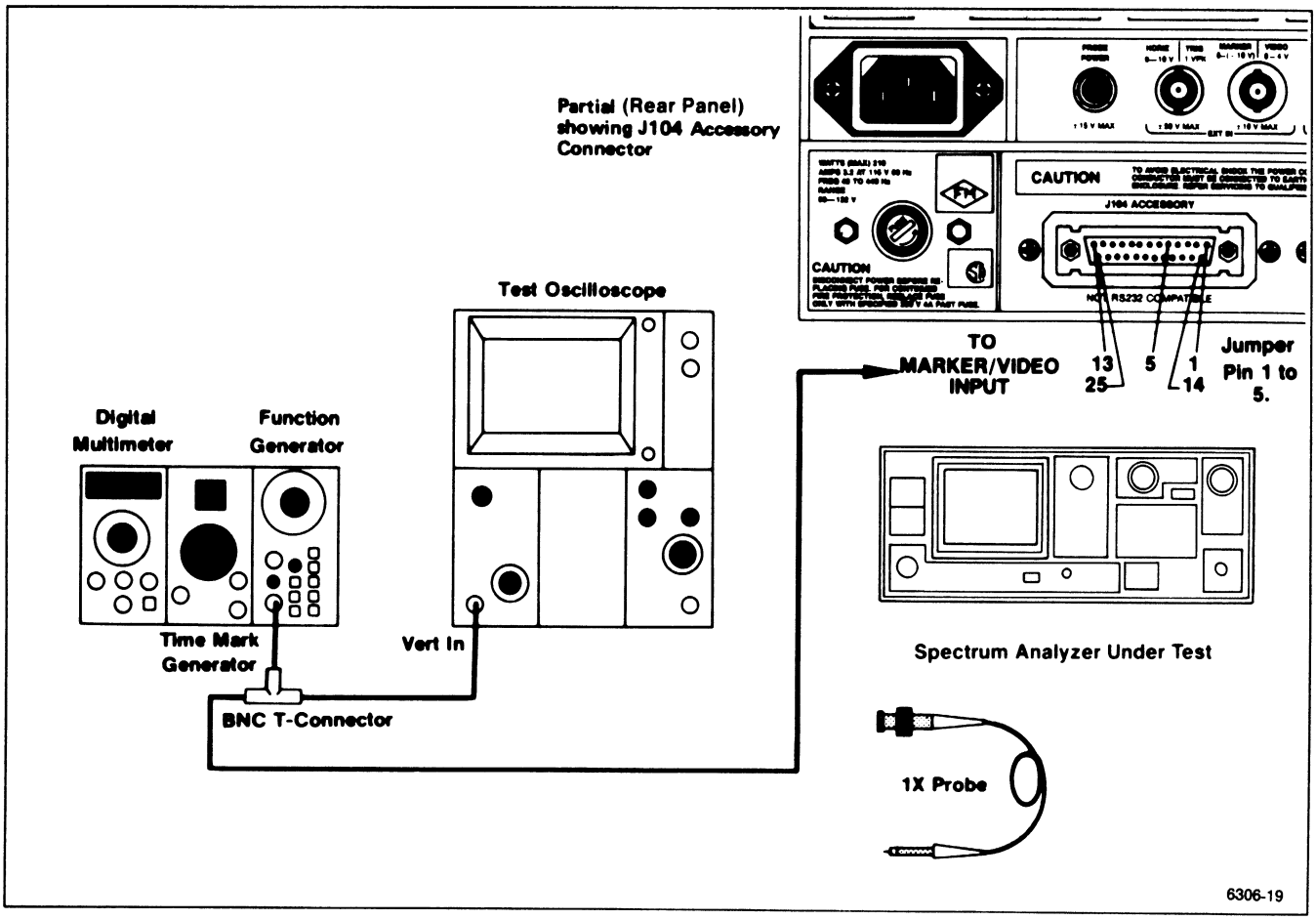


Figure 5-4. Test equipment setup for adjusting the Deflection Amplfier.

n. Adjust C4057 (Figure 5-6) for the best response.

o. Monitor the collectors of Q1072 and Q2078, on the Deflection Amplifier board, with test oscilloscope.

p. Adjust C4061 for the best response.

q. Monitor the collectors of Q1095 and Q2096, on the Deflection Amplifier board, with test oscilloscope.

r. Adjust C5104 for best response.

s. Disconnect the test oscilloscope. Check the appearance of the letter "Z" in GHz of the frequency readout, and if necessary, readjust C5104 and C4061 (vertical output) for the straightest top on the letter "Z".

t. Set the VERTICAL DISPLAY to LIN, TIME/DIV to MNL, the REF LEVEL for 100 μV, and the MANUAL SCAN control fully clockwise.

u. Adjust C5021 and C4057 for best REF LEVEL readout (straightest letters and numerals).

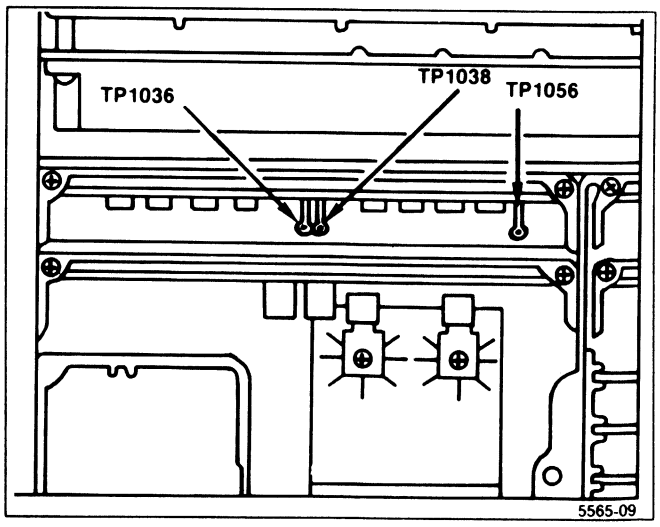


Figure 5-5. Test points on the CRT Readout board.

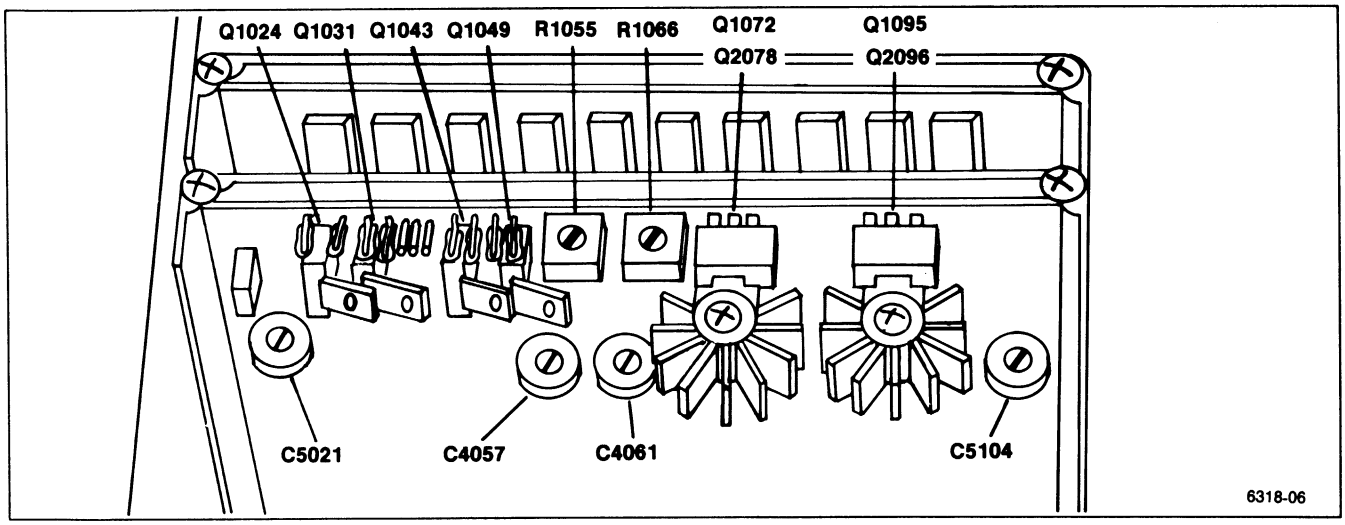


Figure 5-6. Deflection Amplifier test points and adjustments.

4. Adjust Digital Storage Calibration

(R1040, R1050, R1055, and R1060 on the Horizontal Digital Storage board; and R1033, R1034, R1045 and R1046 on the Vertical Storage board)

a. Start the Digital Storage Calibration routine by pressing <SHIFT> 0, and select item 2 (DIGITAL STORAGE CAL.) Follow the instructions that are displayed on the crt, referring to Fig. 5-7.

b. Connect CAL OUT signal to the RF INPUT, and set the Spectrum Analyzer controls as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	200 kHz
RESOLUTION BANDWIDTH	1 MHz
MIN RF ATTEN	0 dB
VERTICAL DISPLAY	2 dB/DIV
VIEW A and VIEW B	Off
PEAK/AVERAGE	Fully Counterclockwise

c. Set REF LEVEL so the signal peak is about one division above the bottom of the graticule.

d. Adjust Input Offset R1046 (Figure 5-7), on the Vertical Digital Storage board, to match the stored display to the non-stored display while repeatedly switching VIEW B on and off.

e. Reset the REF LEVEL to bring the signal peak close to the top of the graticule.

f. Adjust Input Gain R1034 (Figure 5-7), on the Vertical Digital Storage board, to match the stored display to the non-stored display.

g. Because the offset and gain adjustments interact, repeat parts c through f as necessary.

h. Increase FREQ SPAN/DIV to 10 MHz, and tune the signal to within one division of the right edge of the graticule.

i. Adjust Input Gain R1060, on the Horizontal Digital Storage board (Figure 5-7) to match the horizontal position of the stored signal to that of the non-stored signal.

j. Tune the signal to within 1 division of the left edge of the graticule.

k. Adjust Input Offset R1055 on the Horizontal Digital Storage board to match the horizontal position of the stored signal to that of the non-stored signal.

l. Because of interaction, repeat parts i through k as necessary.

5. Adjust Sweep Timing

(R1062 on the Sweeep board)

a. Connect the test equipment as shown in Figure 5-8. Set the following Spectrum Analyzer controls:

FREQ SPAN/DIV	10 MHz or less
TIME/DIV	10 ms
TRIGGERING	EXT

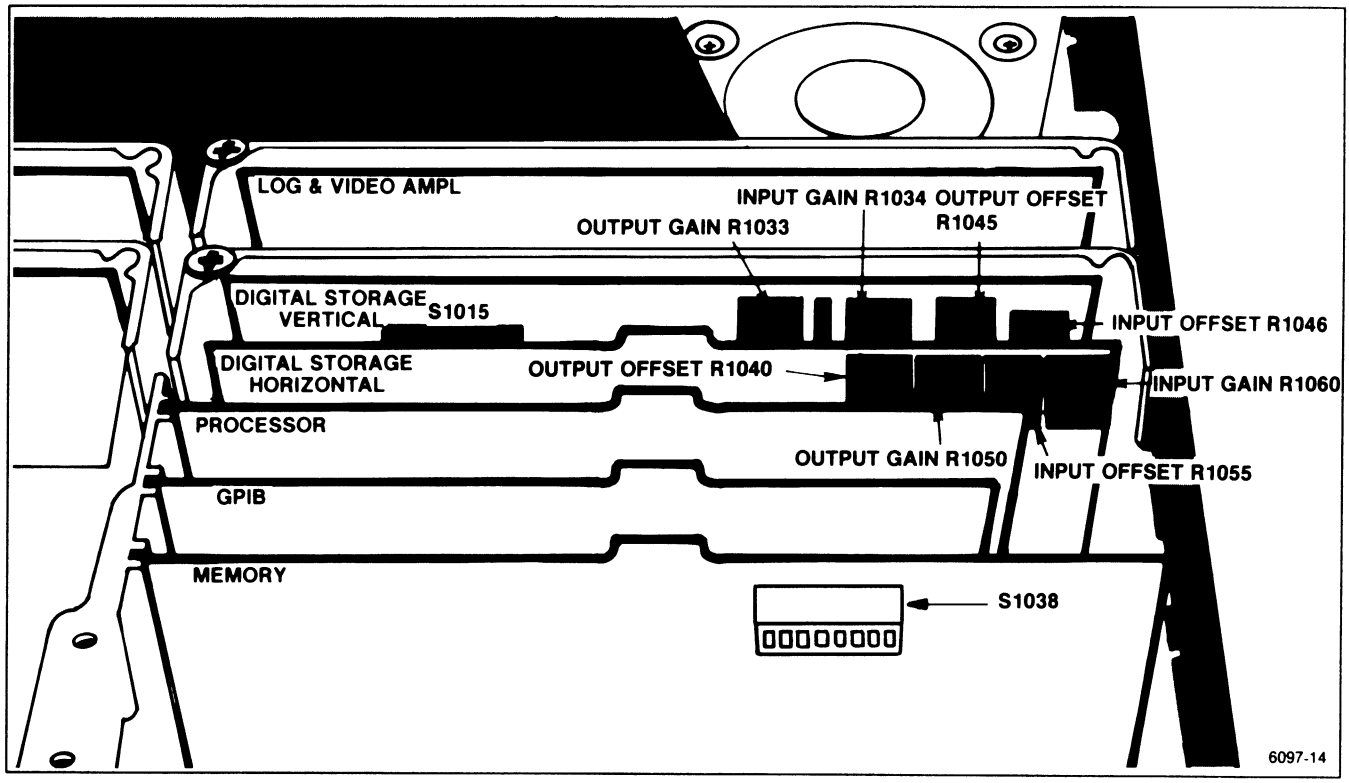


Figure 5-7. Digital storage adjustment locations.

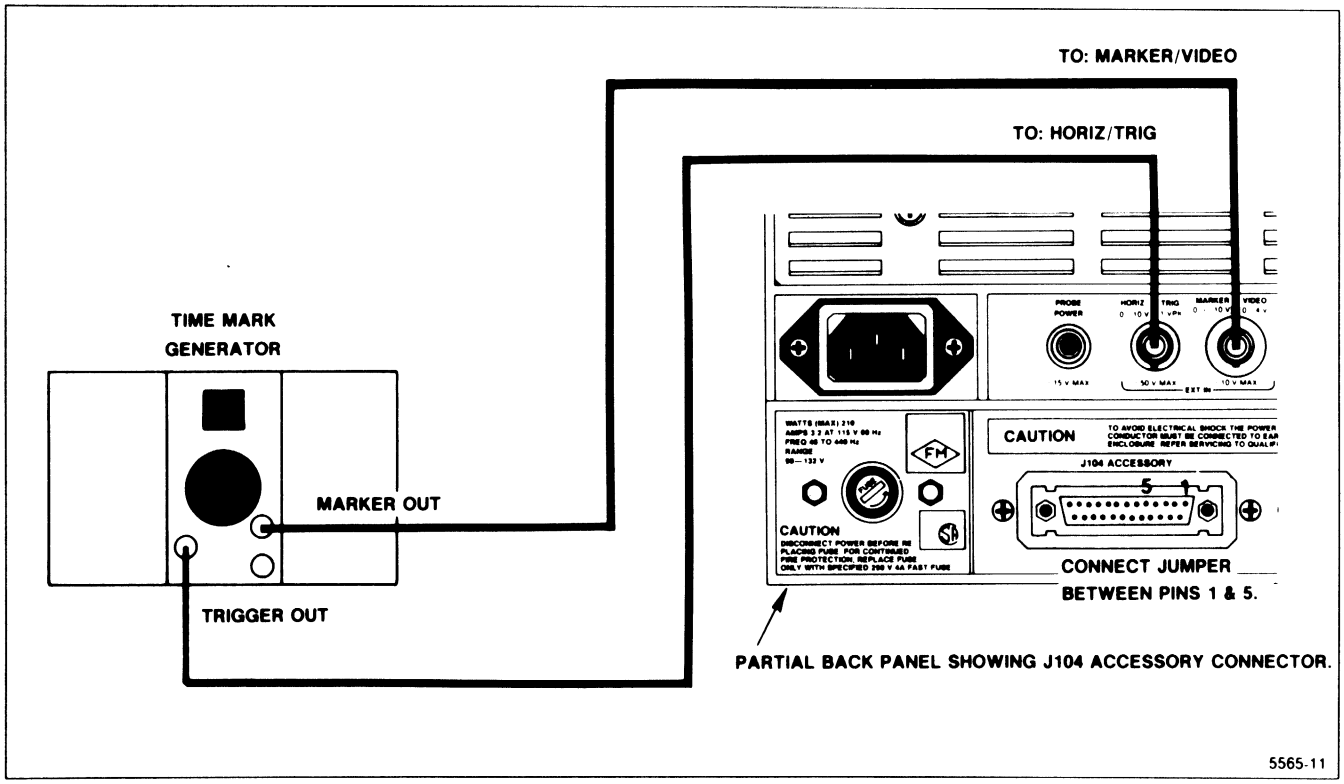


Figure 5-8. Test equipment setup for adjusting sweep timing.

b. Connect a jumper between pins 1 and 5 (Ext Video Select and Ground respectively) on the ACCESSORIES connector.

c. Set the Time Mark Generator controls for 10 ms time marks.

d. Adjust Sweep Timing, R1062 (see Figure 5-9) for 1 marker per division. (Use Horizontal Position adjustment to align markers with graticule lines.)

e. Check the accuracy of the remaining TIME/DIV selections. Error over the center eight divisions must not exceed ±5 %.

f. Reset the TIME/DIV to AUTO and FREQ SPAN/DIV to MAX, activate AUTO RES, and TRIGGERING to FREE RUN.

g. Remove the jumper between pins 1 and 5 of the ACCESSORIES connector. Reposition the trace if moved in part d.

Table 5-3
SWEEP RATE vs SPAN/DIV IN AUTO MODE

FREQ SPAN/DIV	TIME/DIV	RESOLUTION
MAX	20 ms	1 MHz
100 MHz	10 ms	1 MHz
50 MHz	10 ms	1 MHz
20 MHz	10 ms	1 MHz
10 MHz	10 ms	1 MHz
5 MHz	10 ms	100 kHz
2 MHz	10 ms	100 kHz
1 MHz	10 ms	100 kHz
500 kHz	10 ms	100 kHz
200 kHz	50 ms	10 kHz
100 kHz	20 ms	10 kHz
50 kHz	10 ms	10 kHz
20 kHz	10 ms	10 kHz
10 kHz	.1 s	1 kHz
5 kHz	50 ms	1 kHz
2 kHz	20 ms	1 kHz
1 kHz	2 s	100 Hz
500 Hz	1 s	100 Hz
200 Hz	.5 s	100 Hz
100 Hz	.5 s	30 Hz
50 Hz	.5 s	30 Hz
20 Hz	.5 s	30 Hz

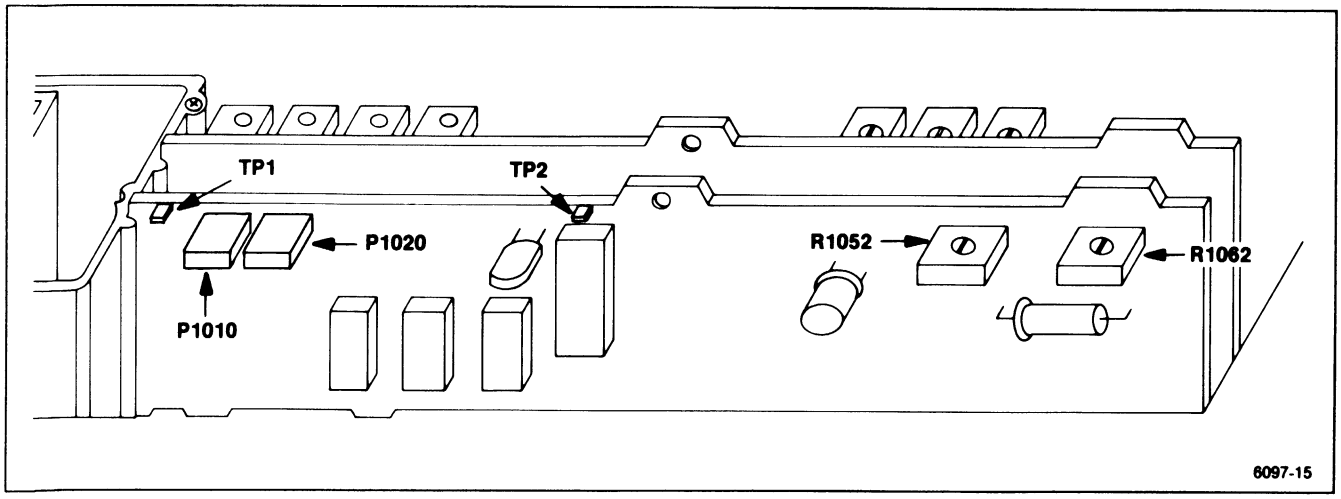


Figure 5-9. Sweep board timing adjustment and test point locations.

6. Adjust Frequency Control System and Dot Marker position

(R1028, R1032, R3040, and R4040 on the CF Control board; R1031, R1032, and R1034 on the 1st LO board; R1063, R1065, R1067, and R1071 on the Span Attenuator board; C1013 and C2011 on the Controlled Oscillator board; and R1052 on the Sweep board)

NOTE

R1028, R1032, R3040, and R4040 on the CF Control board; R1031, R1032, and R1034 on the 1st LO board; and C1013 and C2011 on the Controlled Oscillator board are adjusted in part d.

The Spectrum Analyzer has a procedure in firmware for calibrating the frequency control system. However, it is possible that some adjustments may be misadjusted enough to cause the microcomputer to display an error message. If this occurs, bypass the step then return to the calibration routine.

a. Test equipment required for this step are a Voltmeter, Time Mark Generator, and Frequency Counter. Set the following Spectrum Analyzer controls:

FREQUENCY	0.0 MHz
FREQ SPAN/DIV	5 MHz
TRIGGERING	FREE RUN

b. Connect a shorting strap from TP1035, on the Span Attenuator board, to chassis ground (Figure 5-10). Monitor TP1073 with the voltmeter.

c. Adjust Sweep Offset R1063 (Figure 5-10) for 0.00 V.

d. Remove the shorting strap from TP1035. Press <SHIFT> 0 and select item 1 (FREQUENCY LOOPS CAL), then item 0 (OVERALL SYSTEM) from the menus. Perform the calibration steps as directed ("CONNECT A DVM TO TP1058 ON THE 1ST LO DRIVER BOARD AND GROUND "), etc.

(1) If a "CALIBRATION STEP CANNOT BE COMPLETED" message is displayed, bypass the step, perform the other adjustments then return to the adjustment and try to bring the adjustment in range. If the problem persists, refer to Troubleshooting the Frequency Control System, in the Maintenance section.

e. Adjust 1st LO Sweep as follows:

(1) Apply the CAL OUT signal to the RF INPUT, set the FREQUENCY to 600 MHz, FREQ SPAN/DIV to 100 MHz, and set the REF LEVEL to display the markers.

(2) Adjust Tune Coil Swp R1065, on the Span Attenuator board (Figure 5-10) for one marker per division over the center eight divisions of the graticule. Reset the CENTER FREQUENCY as necessary to align the markers.

(3) Remove the Calibrator signal and apply 0.2 μs time marks from the Time Mark Generator to the RF INPUT.

(4) Set the FREQ SPAN/DIV to 5 MHz, REF LEVEL to +10 dBm, and FREQUENCY to about 10 MHz.

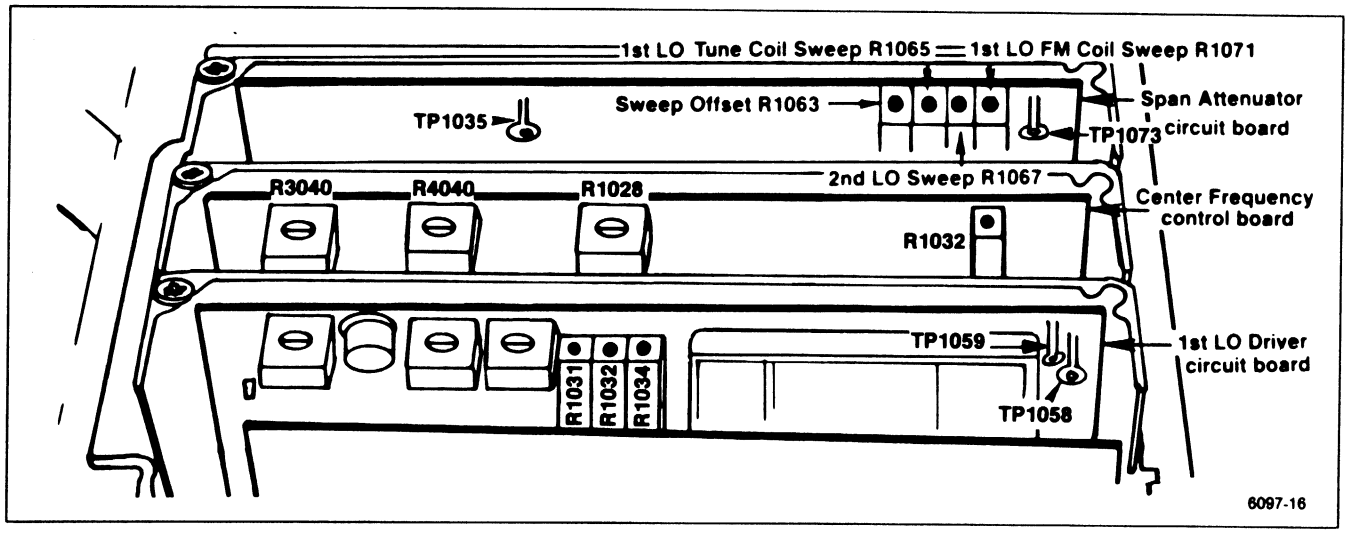


Figure 5-10. Frequency control system test point and adjustment locations.

(5) Adjust the 1st LO FM Coil Swp R1071 (Figure 5-10) for 1 marker/division over the center eight divisions of the display.

(6) Set the FREQ SPAN/DIV to 20 KHz and apply 50 μs markers from the Time Mark Generator.

(7) Adjust the 2nd LO Sweep, R1067, for one marker/division over the center eight divisions.

f. Adjust Dot Marker position as follows:

(1) Disconnect the signal from the RF INPUT.

(2) Press <SHIFT> RESET.

(3) Adjust Dot Position R1052 on the Sweep board to position the dot marker over the start spur.

7. Adjust Log Amplifier

(R4020, R4052, R4071, R4081, and R1085 on the Log Amplifier board)

CAUTION

Use only an insulated screwdriver or tuning tool to make these adjustments.

a. Set the Log Amplifier correction factors to zero by pressing <SHIFT> 0 (DIAGNOSTIC FUNCTIONS) and selecting item 5 (DISABLE/ENABLE USE OF CAL FACTORS), then item 2 (SET RESULTS TO "UNCALED"). Remove Leveler Disable plug P3035 on the Video Processor board (Figure 5-11).

b. Switch POWER off. Remove the Log Amplifier and Detector board assembly from the instrument then remove the shield so adjustments are accessible. Replace the assembly in the instrument and switch POWER back on.

c. Connect the test equipment as shown in Figure 5-12. (P621 must be removed in order to access J621 on the Log Amplifier board. See Figure 5-13.) Set the Spectrum Analyzer controls as follows:

FREQUENCY	2 MHz
FREQ SPAN/DIV	2 MHz
AUTO RESOLN	On
REF LEVEL	−60 dBm
MIN RF ATTEN	0dB
VERTICAL DISPLAY	10 dB/DIV
TIME/DIV	10 ms

d. Center the two front panel LOG and AMPL CAL adjustments. Set the signal generator controls for a 10 MHz/+6 dBm output. Set the step attenuators for 50 dB of attenuation.

e. Position the display at a graticule reference line with the vertical POSITION control, then switch the REF LEVEL from −60 dBm to −110 dBm in decade steps.

f. Adjust the front panel LOG CAL so each 10 dB step equals one division.

g. Reset the REF LEVEL to −20 dBm and the step attenuators for 0 dB attenuation. Reset vertical position to a graticule line if necessary.

h. Increase the attenuation through the step attenuators in 10 dB increments to 50 dB.

i. Adjust the Log Gain, R4020 (Figure 5-13) so each 10 dB increment of attenuation results in one major division of change on the display.

j. Reset vertical position by temporarily removing the signal and setting the vertical POSITION control to position the baseline at the bottom graticule line. Return the step attenuator to 0 dB. Display should be full screen (+6 dBm); if not, readjust the signal generator output for +6 dBm.

k. Adjust Input Ref Level, R4071 (Figure 5-13) for minimum amplitude change between the 10 dB/DIV and 2 dB/DIV displays while alternately switching the VERTICAL DISPLAY between 10 dB/DIV and 2 dB/DIV.

l. Activate 2 dB/DIV and add 10 dB of attenuation. If the 10 dB step (5 division) is short, adjust the gain slightly with R4020 in the same direction; then remove the 10 dB of external attenuation and adjust R4071 for a full screen display. Repeat this check until the 10 dB step is within 0.2 dB of 10 dB. Activate 10 dB/DIV and recheck 10 dB logging.

m. Activate 2 dB/DIV and momentarily remove the input signal to the Log Amplifier. Position the baseline on the bottom graticule line then return the signal to the Log Amplifier.

n. Adjust Output Ref Level, R4081 (Figure 5-13) for a full screen (eight divisions) display.

o. Switch to the 10 dB/DIV mode and set the step attenuators for 40 dB of attenuation. Adjust Log Linearity, R1085 (Figure 5-13) so the display is mid-screen.

p. If a large change in the setting of R1085 was required in part l, repeat the adjustments of R4071 and R4081 because of interaction.

q. Check the accuracy of 10 dB/DIV and 2 dB/DIV display modes by adding attenuation in 10 dB steps for 10 dB/DIV mode and 1 dB steps for the 2 dB/DIV mode and observing that the display steps 1 major division, ±0.25 minor division, for each 10 dB step, and 0.5 division, ±0.5 minor division, for the 2 dB mode. (Readjust the signal generator output to establish a new reference level after each step.) After the accuracy of the individual steps has been verified, reset the signal level for full screen.

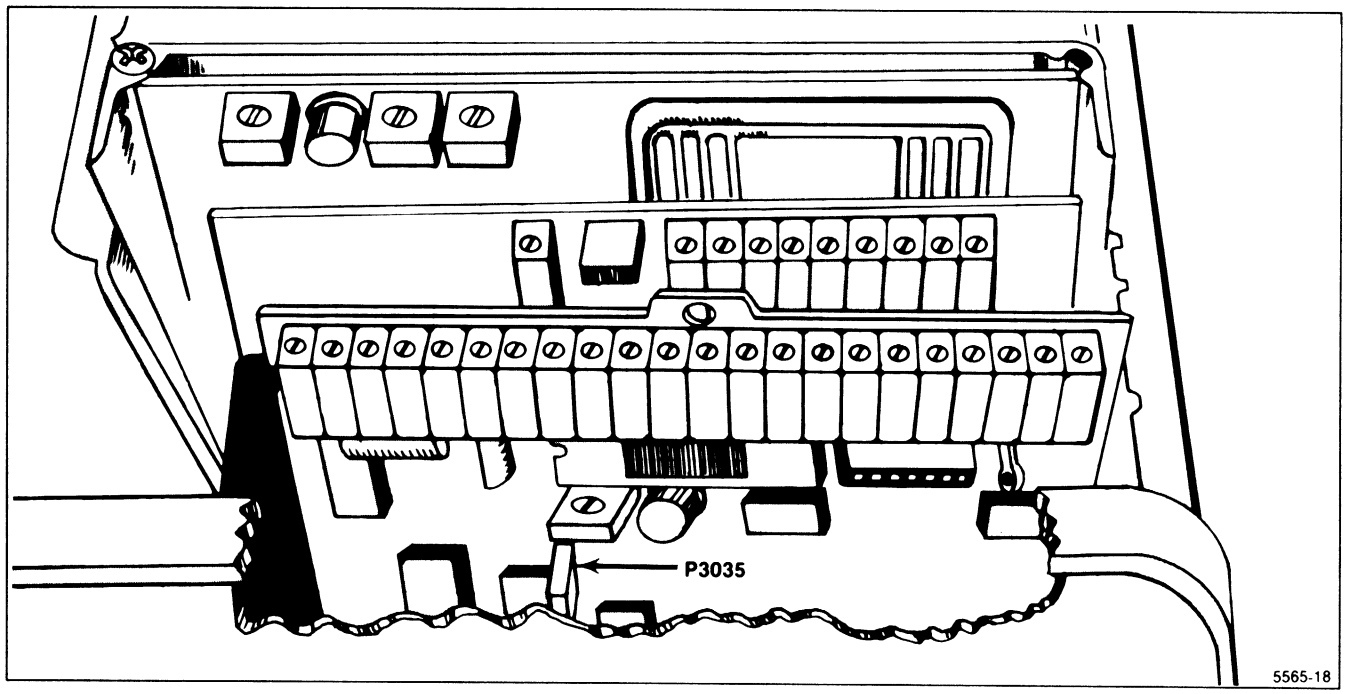


Figure 5-11. P3035 on the Video Processor board.

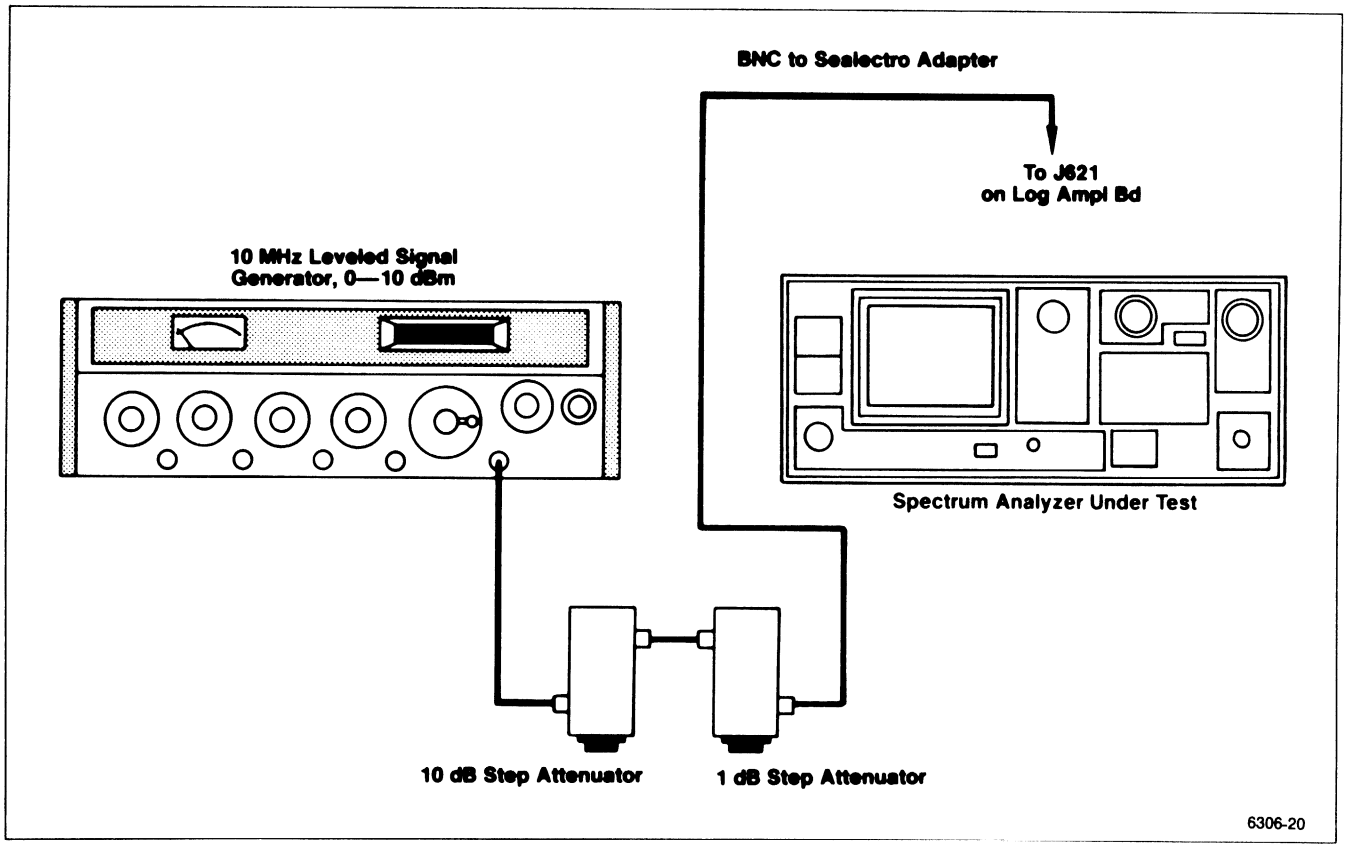


Figure 5-12. Test equipment setup for adjusting the Log Amplifier.

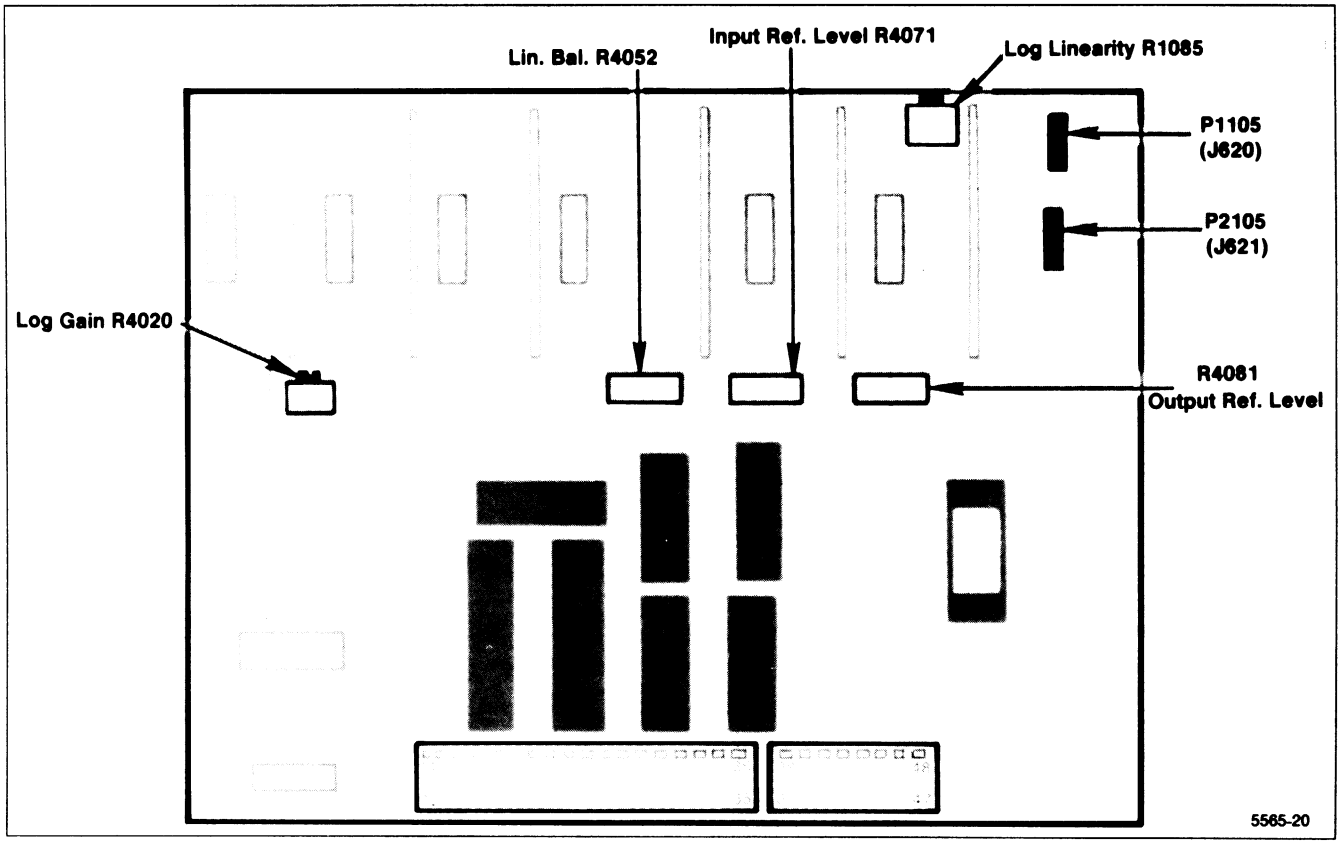


Figure 5-13. Log and Video Amplifier test point and adjustment locations.

r. Add appropriate step attenuation to step the display down screen and measure the worst case error over the dynamic range. Error must not exceed ±1.5 dB over the first 80 dB of range,or ±1.0 dB over the 16 dB range.

s. If the 10 dB log step in the 2 dB/DIV mode is long, adjust gain with R4020 for less gain and rebalance R4071.

t. Set the step attenuators to 10 dB and activate 2 dB/DIV.

u. Set the Ref Level to −15 dBm and adjust the signal generator output for a full screen display in the 2 dB/DIV mode.

v. Press LIN and adjust Lin Mode Balance, R4052 (Figure 5-13) for a full screen display. Amplitude of LIN, 2 dB/DIV, and 10 dB/DIV display should now be the same.

w. Check LIN display linearity by adding 6 dB, 12 dB, and 18 dB of attenuation and note the display step down from full screen to, 4 ±0.4, 6 ±0.4, and 7 ±0.4 divisions.

x. Remove the signal generator signal connection to the Log Amplifier input jack and replace P621. Switch POWER off, remove Log Amplifier board and replace the shield. Replace P3035 on the Video Processor board. Re-install the assembly and switch POWER on.

8. Adjust Resolution Bandwidth and Shape Factor

(C1022, C2026, C5055, C5048, R3041, R1065, R3015, R3029, and R3033 on the VR 2nd Filter Select board) (C1026, C1033, C2037, C3023, C3035, C3050, R2025, and R3035 on the VR 1st Filter Select)

NOTE

The filters in each section are aligned separately, then a signal is applied through both the first and second sections. The final adjustments trim filter shape and bandwidth. Because of interaction, it is easy to offset one filter to compensate for another misadjusted filter; therefore, only adjust each filter in small increments.

The 3 dB down bandwidth of each filter section should be as wide or slightly wider than the 6 dB down point of the combined two filter sections.

Before calibrating the Variable Resolution Bandwidth and Gain, set the correction factors to zero by pressing <SHIFT> 0 and selecting item 5, then item 2.

a. Equipment setup is shown in Figure 5-14.

(1) Remove and install the Variable Resolution module on an extender.

(2) Use a Sealectro male-to-male adapter and coaxial cable to connect the 10 MHz IF output signal, from the 3rd Converter, to the input of the second section (make connection from plug removed from J693 to J683).

(3) Connect the output of the Post VR Amplifier to the input of the Log Amplifier assembly by connecting a cable from J682 on the Variable Resolution Module to J621 on the Log & Video Amplifier assembly (see Figures 5-15 and 5-14).

(4) Apply the CAL OUT signal to the RF INPUT, and set the Spectrum Analyzer controls as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	50 kHz
RESOLUTION BANDWIDTH	10 kHz
REF LEVEL	−20 dBm
MIN RF ATTEN	0 dB
VERTICAL DISPLAY	2 dB/DIV

b. Reset the REF LEVEL for a seven division excursion. Tune the display to center screen and activate SAVE A.

c. Change the RESOLUTION BANDWIDTH to 100 kHz and reset REF LEVEL to bring the signal amplitude to about the same level as the 10 kHz response.

d. Adjust C5055, C5048, and C3041 on the VR 2nd Filter Select board (Figure 5-15) for the best 100 kHz filter response (100 kHz bandwidth, 3 dB down, that is centered about the 10 kHz reference). Refer to Figure 5-16.

e. Reset the RESOLUTION BANDWIDTH to 10 kHz, deactivate and reactivate SAVE A to re-establish the 10 kHz reference.

f. Set the FREQ SPAN/DIV to 500 kHz and the RESOLUTION BANDWIDTH to 1 MHz. Reset the REF LEVEL to set the 1 MHz response amplitude to that of the 10 kHz reference.

g. Adjust C2026 and C1022 (Figure 5-16) for the best 1 MHz response centered about the 10 kHz filter response.

h. Reset the RESOLUTION BANDWIDTH to 100 Hz and FREQ SPAN/DIV to 50 Hz. Set the REF LEVEL such that the response is near the amplitude of the reference.

i. Adjust R4025 (Figure 5-15) for maximum signal amplitude. Deactivate SAVE A.

j. Disconnect the 10 MHz third converter IF signal from J683 and reconnect it to J693 (see Figure 5-17). Reconnect P683 to J683 (Figures 5-14 and 5-15).

k. Set the FREQ SPAN/DIV to 1 kHz, RESOLUTION BANDWIDTH to 1 kHz and reset the REF LEVEL for a 7 division display. Activate SAVE A.

l. Set the FREQ SPAN/DIV to 10 kHz, RESOLUTION BANDWIDTH to 10 kHz and adjust REF LEVEL for a 7 division display.

m. Adjust C2037 (Figure 5-17) for the best 10 kHz response centered about the 1 kHz reference.

n. Deactivate SAVE A and then reactivate to save the 10 kHz display.

o. Now, set the FREQ SPAN/DIV to 50 kHz, RESOLUTION BANDWIDTH to 100 kHz.

p. Adjust C3050, C3035, and C3023 (Figure 5-17) for the best 100 kHz response centered about the 10 kHz filter reference.

q. Set the RESOLUTION BANDWIDTH to 1 MHz, FREQ SPAN/DIV to 500 kHz.

r. Adjust the 1 MHz filter response and centering with C1033 and C1026 in the VR Input board (Figure 5-17). Deactivate SAVE A.

s. Check the waveshape, bandwidth, and centering of all filters. If necessary, make only fine or minor adjustments. Figure 5-18 shows typical response shapes.

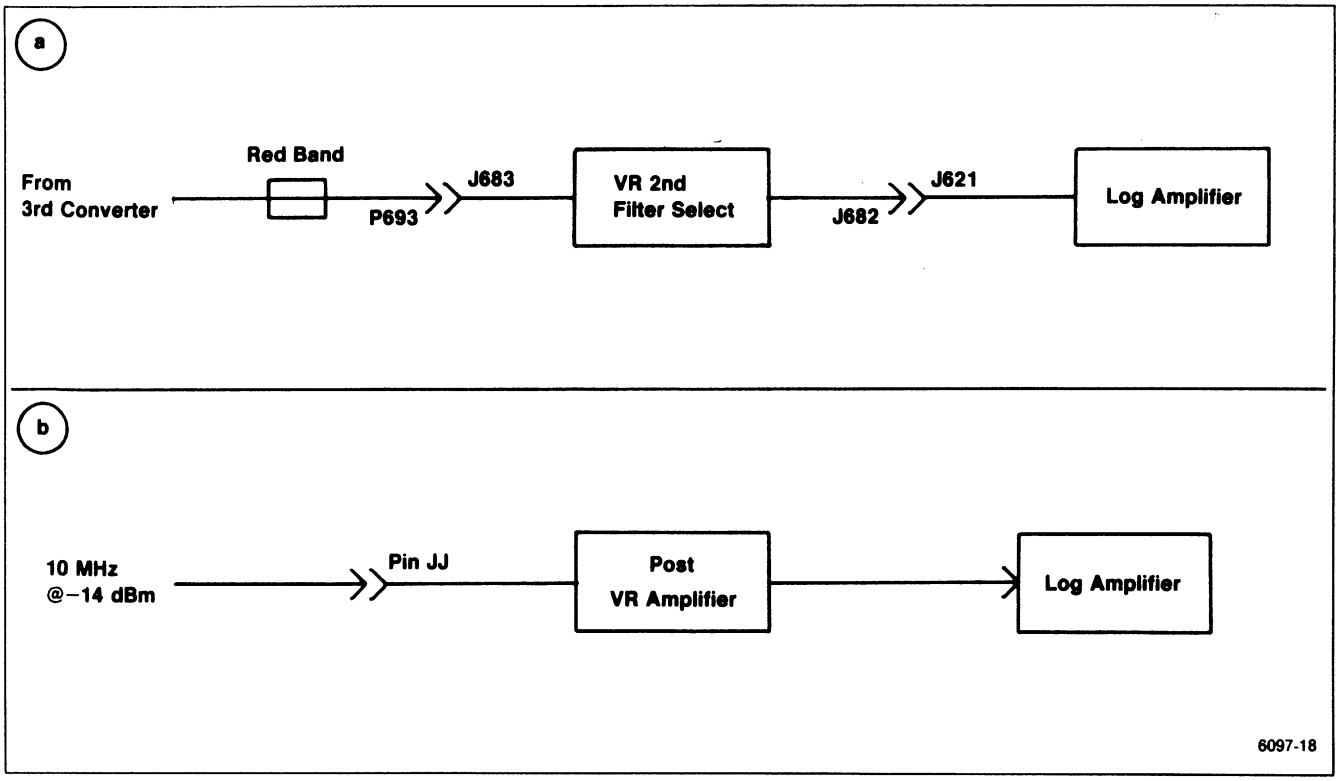


Figure 5-14. Test equipment setup for adjusting the Variable Resolution module.

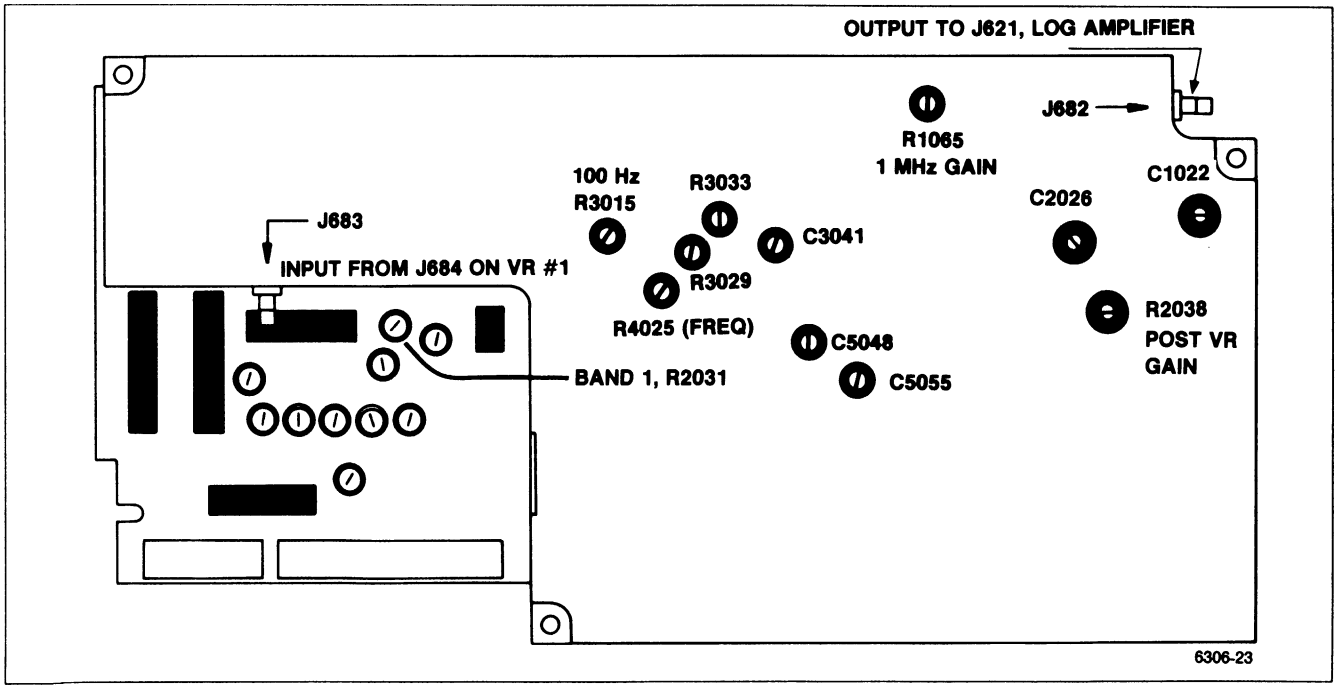


Figure 5-15. Adjustments on the front of the Variable Resolution module.

t. Level the gain of the filters as follows:

(1) Set the FREQ SPAN/DIV to 500 kHz, RESOLUTION BANDWIDTH to 100 kHz, and REF LEVEL to −20 dBm.

(2) Adjust all filters to the 100 kHz level as per the following table. Change FREQ SPAN/DIV as necessary to maintain a suitable display.

Filter	Adjust
1 MHz	R1065
10 kHz	R3033
1 kHz	R3029
100 Hz	R3015
30 Hz	R2025

Locations of the adjustments are shown in Figures 5-16 and 5-17.

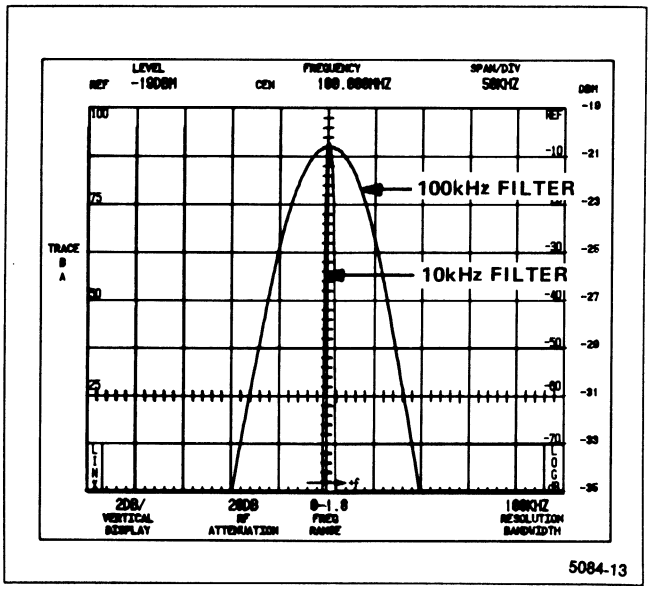


Figure 5-16. 100 kHz filter response over 10 kHz filter reponse.

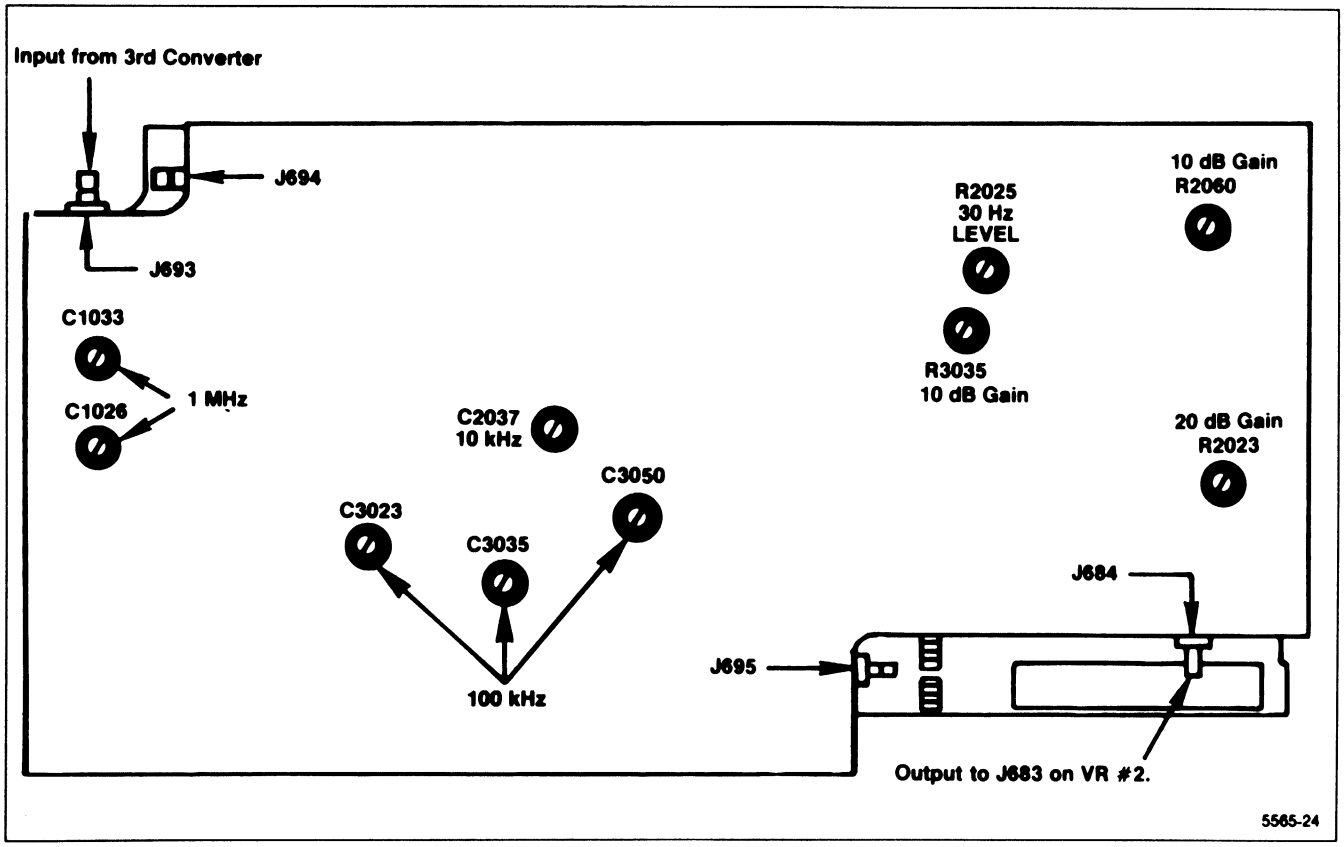


Figure 5-17. Adjustments on the rear of the Variable Resolution module.

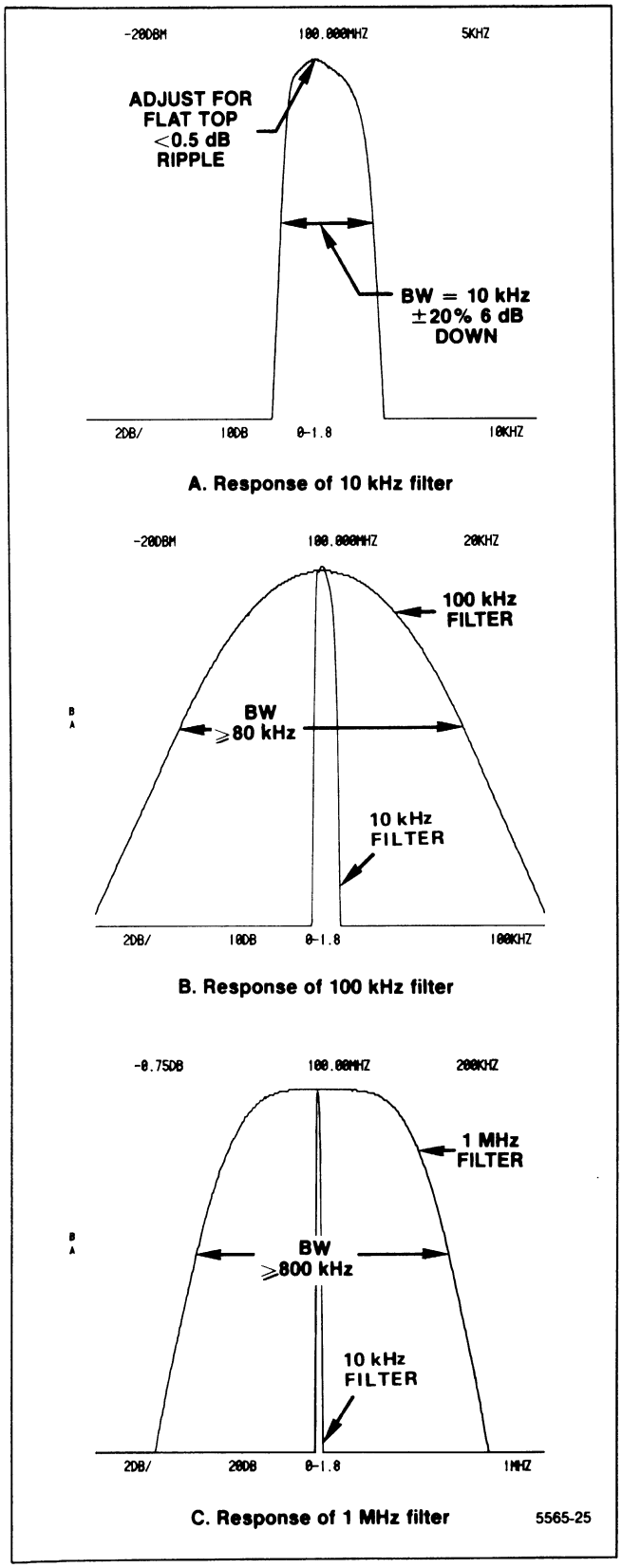


Figure 5-18. 10 kHz, 100 kHz, and 1 MHz filter response.

9. Preset the Variable Resolution Gain and Band Leveling

(R2038 on the Post VR Amplifier board)
(R2031 on the VR #2 Mother board)
(R3035 on the 10 dB Gain Steps board)
(R2023 and R2060 on the 20 dB Gain Steps board)

NOTE

The Log Amplifier must be calibrated before adjusting any Variable Resolution gain settings. Log Amplifier calibration can be verified by applying a +6 dBm, 10 MHz signal to the input (J621), of the Log Amplifier, and checking for full screen display with the REF LEVEL at −20 dBm.

a. Before adjusting the Variable Resolution gain and band leveling, set the correction factors to zero by pressing <SHIFT> 0, and selecting menu item 5, then item 2.

b. Test equipment setup is shown in Figure 5-14. Set the Spectrum Analyzer controls as follows:

FREQ SPAN/DIV	1 MHz
RESOLUTION BANDWIDTH	100 kHz
REF LEVEL	−20 dBm
MIN RF ATTEN	0 dB
VERTICAL DISPLAY	2 dB/DIV

c. The gain of the Post VR Amplifier should be 20 dB for best signal-to-noise ratio through the Variable Resolution stages. If any maintenance has been performed on this stage, perform the following steps.

(1) Remove the cover for the VR 2nd Filter Select board. Disconnect the jumper connector to the input of the Post VR Amplifier (pin JJ).

(2) Apply a 10 MHz, −14 dBm signal, from a 50Ω signal source, to pin JJ of the amplifier.

(3) Adjust Post VR Gain R2038 on the Post VR Amplifier board for a full screen display.

(4) Remove the signal from the input to the Post VR Amplifier and replace the jumper connector to pins JJ at the input to the Post VR Amplifier. Replace the cover for the VR 2nd Filter Select board.

d. Set the front panel AMPL CAL fully counterclockwise and set the Band 1 Gain R2031 on VR Mother board #2 (Figure 5-15) fully counterclockwise.

e. Disconnect P693 (Figure 5-17) and activate MIN NOISE. Apply a 10 MHz, −25 dBm signal, from the signal generator, through a bnc-to-Sealectro adapter to J693. Set the generator frequency to peak the signal amplitude. (Signal amplitude should be between 3.5 and 6.5 divisions. If signal amplitude is not within these limits it indicates a gain problem in the Variable Resolution module.)

f. If the signal amplitude is over 5 divisions, adjust the Post VR Gain R2038 (Figure 5-15) for a 5 division signal amplitude.

g. Reset the front panel AMPL CAL for a 7 division signal.

h. Switch MIN NOISE off, decrease the generator output to −35 dBm, leave the REF LEVEL at −20 dBm, and adjust the 10 dB Gain R3035, on the 10 dB Gain board (Figure 5-17) so the signal amplitude is 7 divisions.

i. Change the generator output to −45 dBm, the REF LEVEL to −40 dBm, and adjust the 20 dB Gain R2023 on the 20 dB Gain Step board (Figure 5-17) for a 7 division signal amplitude.

j. Change the generator output to −65 dBm, the REF LEVEL to −60 dBm, and adjust the 10 dB Gain R2060 on the 20 dB Gain Step board (Figure 5-17) for a 7 division signal amplitude.

k. Set the REF LEVEL to −30 dBm and the generator output to −35 dBm. Check for a 7 division signal amplitude. Repeat this check for −45, −55, and −65 dBm input levels. Note that each maintains the 7 division signal to verify that the gain of the Variable Resolution gain stages are correct. Readjust gain if necessary.

l. Remove the 10 MHz signal to J680 and reconnect P680. The final band level adjustments are described after calibrating the Preselector Tracking and checking flatness. The mean level for each band is set to the level of Band 1.

m. Press <SHIFT> CAL to rerun a calibration routine and re-establish processor correction factors.

10. Adjust Calibrator Output Level

(R1041 on the 100 MHz Osc and 3rd Converter board)

NOTE

The calibrator output level is matched to a known reference. A power meter is used to verify the output level of the reference signal generator. Harmonics of the signal generator must be greater than 40 dB down from the fundamental.

a. Apply a 100 MHz signal from the signal generator to the power meter through a 3 dB attenuator. Set the generator output level for a reading of −20 dBm on the power meter. This sets up a reference signal for adjusting the calibrator output level.

b. Disconnect the power meter from the signal generator, and connect the refence signal (from the generator) to the test spectrum analyzer RF INPUT using the same cable that was used to set the reference signal.

c. Set the test spectrum analyzer controls as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	100 kHz
RESOLUTION BANDWIDTH	1 MHz
REF LEVEL	−18 dBm
MIN RF ATTEN	0 dB
VIEW A and VIEW B	On
PEAK/AVERAGE	Fully Counterclockwise
TIME/DIV	AUTO
TRIGGERING	AUTO

d. Set the test spectrum analyzer Vertical Display factor to the Δ A mode by pressing FINE. Set the REF LEVEL such that the top of the signal is on a graticule line near the top of the crt. Reset the REF LEVEL to 0.00 dB by pressing FINE twice. Store the display by activating SAVE A.

e. Remove the reference signal from the RF INPUT and connect the CAL OUT signal in its place. Tune the CENTER FREQUENCY control to align the CAL OUT signal with the SAVE A display.

f. Adjust Cal Level R1041, in the 3rd converter (Figure 5-19) for no displacement between the CAL OUT signal and the reference (VIEW B and SAVE A displays).

11. Adjust IF Gain

(R1015 on the 110 MHz Amplifier board)

a. Test equipment setup is shown in Figure 5-19. Set the RESOLUTION BANDWIDTH to 100 kHz, REF LEVEL to −20 dBm, and apply a −21.5 dBm, 110 MHz signal, through step attenuators, to the input (J365) of the 110 MHz filter.

b. Set the step attenuators for 0 dB. Adjust the signal generator for maximum amplitude display. (With −21.5 dBm input the signal level should be 7 divisions or more.) Set the generator output for a 7 division signal reference level.

c. Remove the 110 MHz signal from the 110 MHz filter and reconnect P365.

d. Set the step attenuators for 21 dB attenuation and apply the 110 MHz signal to the input (J321) of the 110 MHz IF amplifier (Figure 5-19).

e. Adjust R1015, 110 MHz IF Gain, for a display amplitude that equals the seven division reference set in part b.

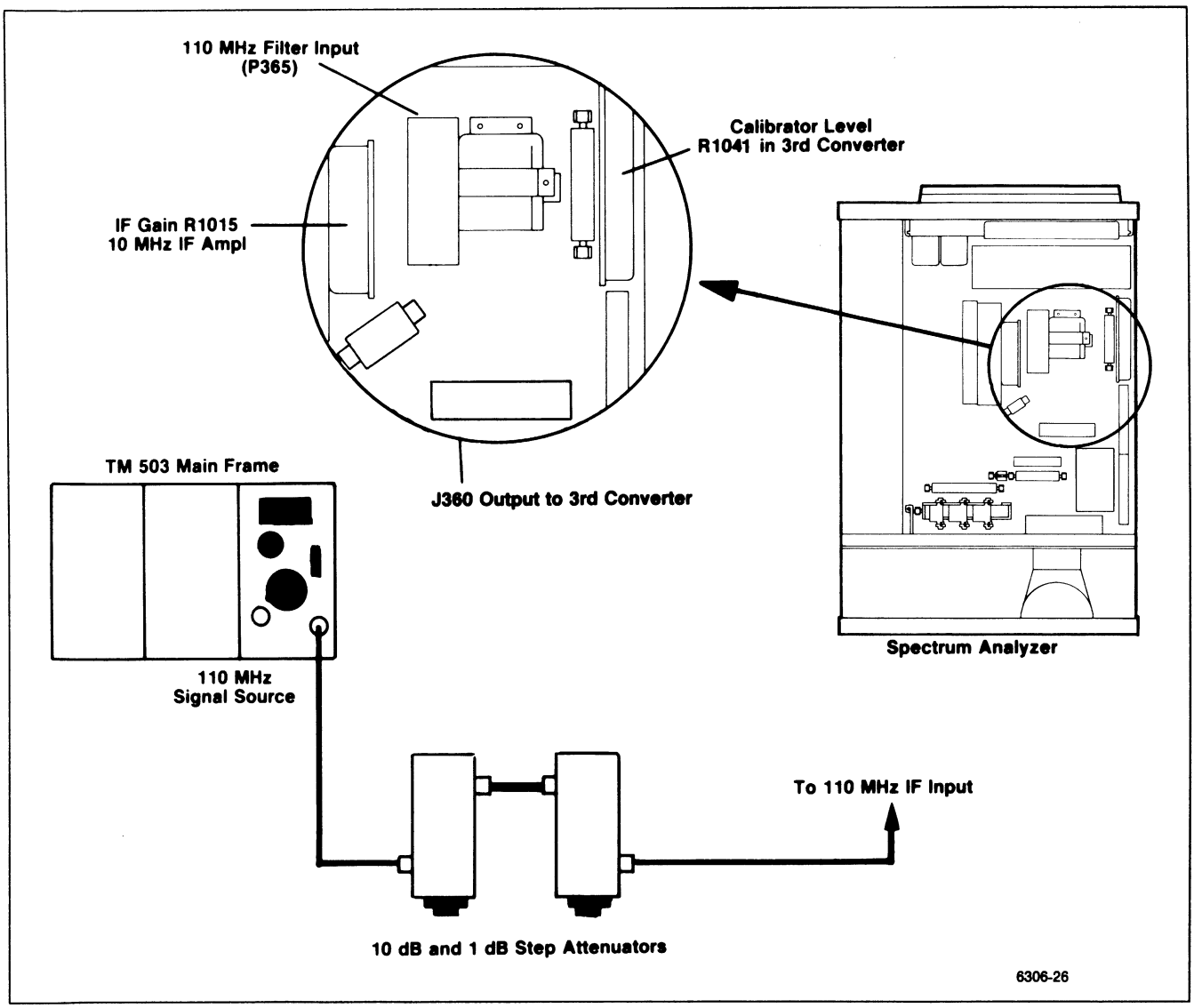


Figure 5-19. IF gain test setup, and adjustment and connector locations.

f. Remove the 110 MHz signal and reconnect P321. Apply the CAL OUT signal to the RF INPUT. Set the Spectrum Analyzer controls as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	100 kHz
RESOLUTION BANDWIDTH	100 kHz
REF LEVEL	−20 dBm

g. Set the front panel AMPL CAL fully counterclockwise and readjust R1015 (110 MHz IF Gain) for 5 divisions of signal. (If this cannot be achieved, it indicates excessive loss through the front end.)

h. Adjust the AMPL CAL for a full screen signal. AMPL CAL adjustment should now have 6 dB down range and 6 dB or more up range.

NOTE

Two variable capacitors, C1054 and C2047 on the 110 MHz IF board, do not require adjustment during calibration. These adjustments require return loss measurement which is a maintenance and repair function.

12. Adjust B-SAVE A Reference Level

(S1015 on the Vertical Digital Storage board)

When B-SAVE A is selected, the expression implemented is [(B-SAVE A) + k , where k is a constant set by the input data for an 8-to-4 line encoder, U1015. Each bit will move the reference level about 0.2 minor division. Normally, the reference level is set at the center graticule line; however, it can be set anywhere within the graticule area by the setting of an 8-bit binary switch, S1015 (Figure 5-7). The MSB (switch #8) shifts the display about five divisions, switch #7 half this amount, etc. The following procedure sets the reference level.

Estimate the amount and direction the reference level is to be shifted, then close or open the switches on S1015 to obtain the desired B-SAVE A reference level.

13. Adjust Band Leveling

(R2031 on the VR #2 Mother board)

NOTE

The mean value of the frequency response is set to a −20 dBm reference at 100 MHz.

a. Perform Frequency Response Check as described in the Performance Check section and note the frequency at the mean level (average level between two extremes).

b. Perform adjustment step 11 (Preset the Variable Resolution Gain and Baseline Leveling) prior to proceeding with this step.

c. Set R2031 on the VR #2 Mother board to midrange.

d. Connect test equipment as shown in Figure 5-20. Set the Spectrum Analyzer controls as follows:

FREQ SPAN/DIV	500 kHz
AUTTO RES	On
REF LEVEL	−20 dBm
MIN RF ATTEN	0 dB
VERTICAL DISPLAY	2 dB/DIV
VIEW A and VIEW B	On

e. Apply a calibrated −20 dBm signal, whose frequency is the same as that noted for the mean level in part a, to the RF INPUT. Set the FREQUENCY to the input signal.

f. Adjust Band 1 Gain R2031 on the VR Mother board #2 (Figure 5-21) for a full screen (−20 dBm) display.

14. Phase Lock Calibration

(C1016, C1018, C1032, and C1034 on the Strobe Driver board; C1013 and C2011 on the Controlled Oscillator board; and R3082 on the Error Amplifier board)

The Phase Lock assembly normally requires calibration only after some part of the assembly has been repaired or replaced. The specification on the noise sidebands should be met before calibrating the assembly.

a. Test equipment setup is shown in Figure 5-22. Remove the Phase Lock module and the two cover plates so all circuit test points and adjustments are accessible. Plug the assembly on extender boards and into the instrument. Use extender cables and adapters to reconnect signal cables to their respective connector (cable with yellow band to J501, and the cable with black band to J502).

If desired, the direct reading counter may be connected to the Vertical Output of the test oscilloscope to get a count of a display at each test point, when appropriate, throughout this procedure. The ground side of the test oscilloscope probe will serve as the common ground return for both instruments.

b. Press <SHIFT> CAL and do the directed calibration routine through adjusting the LOG CAL. Press <SHIFT> to return the instrument to normal operation and set REF LEVEL to −30 dBm. Check that the AUTO RES is active (button lit).

c. Check Offset Mixer — This part of the procedure is only required after repair or replacement of the Mixer board.

(1) Connect the Direct Input of the frequency counter to pin N (Figure 5-23) and set the counter controls for a count. Note the frequency.

(2) Connect the counter to pin K and note the frequency.

(3) Connect the counter to the collector of Q1040 and note the frequency. Frequency should equal the difference between pins N and K (e.g., 25.080 MHz − 25.000 MHz = 80 kHz). Disconnect the counter probe from the collector of Q1040.

(4) Connect a test oscilloscope probe to the collector of Q1040 and check for a signal with a frequency of approximately 80 kHz, 50% duty cycle, and an amplitude of approximately 5 V peak-to-peak.

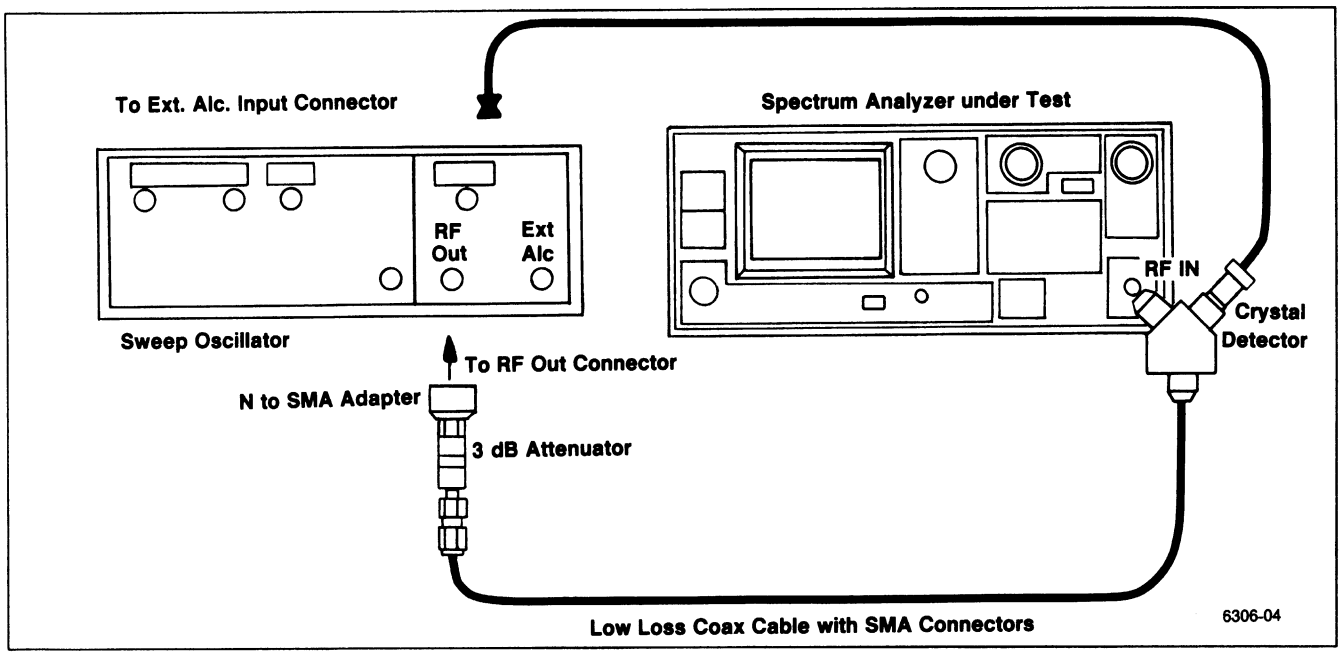


Figure 5-20. Test equipment setup for band leveling adjustment.

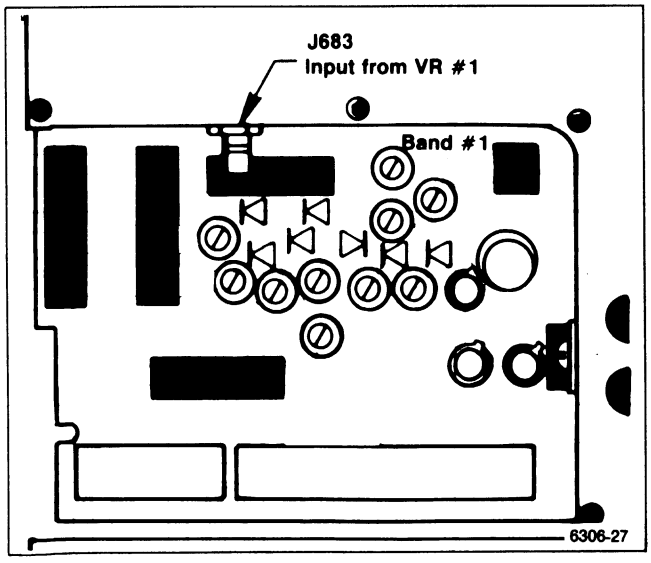


Figure 5-21. Band leveling adjustment and gain diode locations.

d. Check Synthesizer

(1) Set the FREQ SPAN/DIV to 200 kHz. Phase lock should occur.

(2) Change FREQ SPAN/DIV to 500 kHz and connect the counter to J500 on the Synthesizer board. Check for a reading of 50.00 MHz.

(3) Connect the counter to TP2040 (Figure 5-23a) and check for a reading that is near 25.0 MHz.

(4) Connect the test oscilloscope to TP1040 (Figure 5-23a) and check for positive pulses with an amplitude of approximately 4 V peak-to-peak.

(5) Change the FREQ SPAN/DIV to 200 kHz and observe that the signal on TP1040, in part (4) is still there.

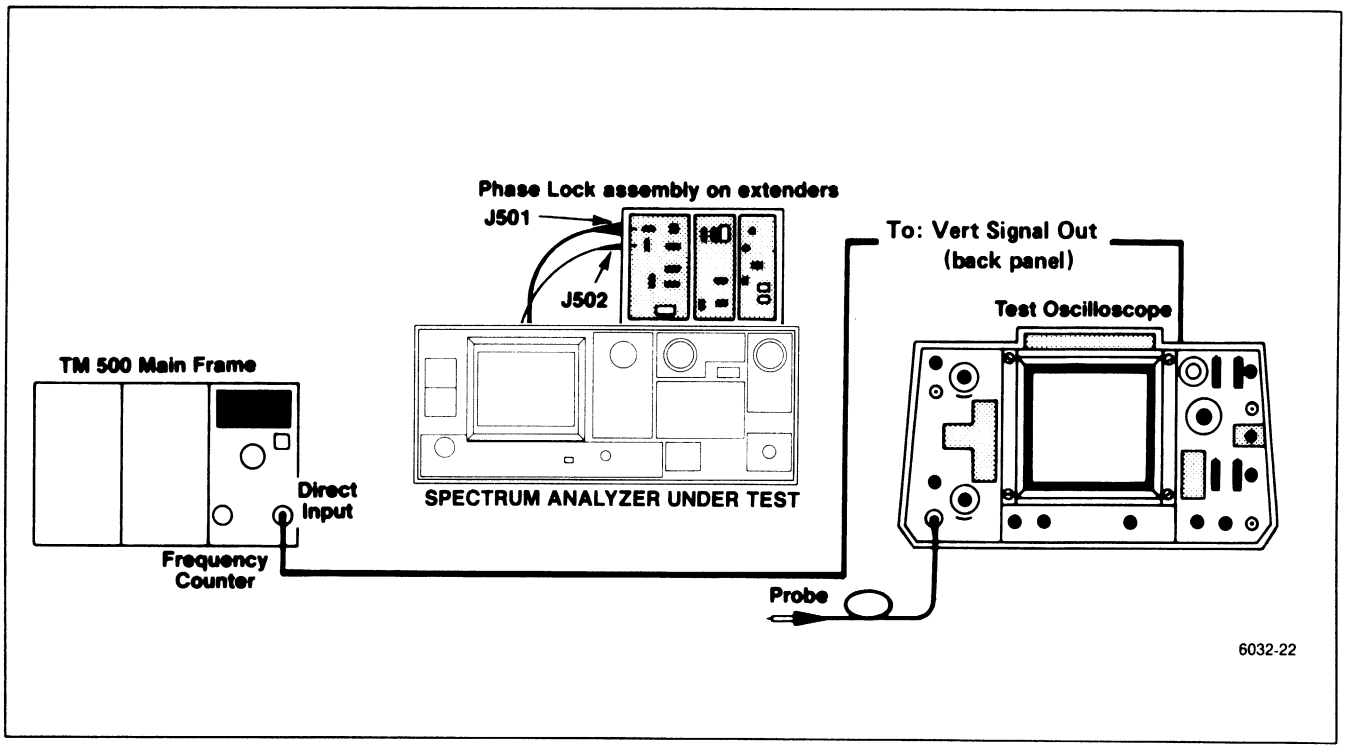


Figure 5-22. Test equipment setup for adjusting the Phase Lock assembly.

e. Controlled Oscillator — This part of the check is only required after repair or replacement of the Controlled Oscillator board.

NOTE

Bandpass filter adjustments C1041 and C1042 are set at the factory because they require a special test fixture. These adjustments do not need further adjustment.

If adustment of C1013 and C2011 is not sufficient to achieve phase-lock, the board should be replaced.

(1) Press <SHIFT> 0 and select item 1 (FREQUENCY LOOPS CAL), then item 5 (PHASE LOCK SYNTHESIZER) from the displayed menu.

(2) Follow the instructions until the message, "VERIFY LAST STEP". Due to the interaction of adjustment capacitors C1013 and C2011, the two steps will have to be repeated until the voltages are correct. Alternately press GHz and MHz on the Data Entry keypad, and adjust until the two voltage readings are correct.

(3) Connect the counter to TP2011 on the Controlled Oscillator board (Figure 5-27a) and alternately press GHz and MHz and check for a count reading of either 25.0943 MHz or 25.0328 MHz.

f. Check Operation of Strobe Driver

The "Phase Lock Synthesizer" test is still used for this test. If aborted, press <SHIFT> 0 to return to the Synthesizer routine. Any step in the routine will work.

(1) Connect the test oscilloscope to TP1012 on the Strobe Driver board (Figure 5-23b) and check for a square wave response with a Time/Div setting of peak-to-peak.

(2) Connect the test oscilloscope to TP1032 and check for a sinusoidal waveform of approximately 5 V p-p.

(3) Connect the counter to TP1032 and check for a count of either 5.018868 or 5.006477 MHz.

(4) Connect the test oscilloscope to J504 and check for 5 V logic levels.

(5) Press <SHIFT> to abort the test.

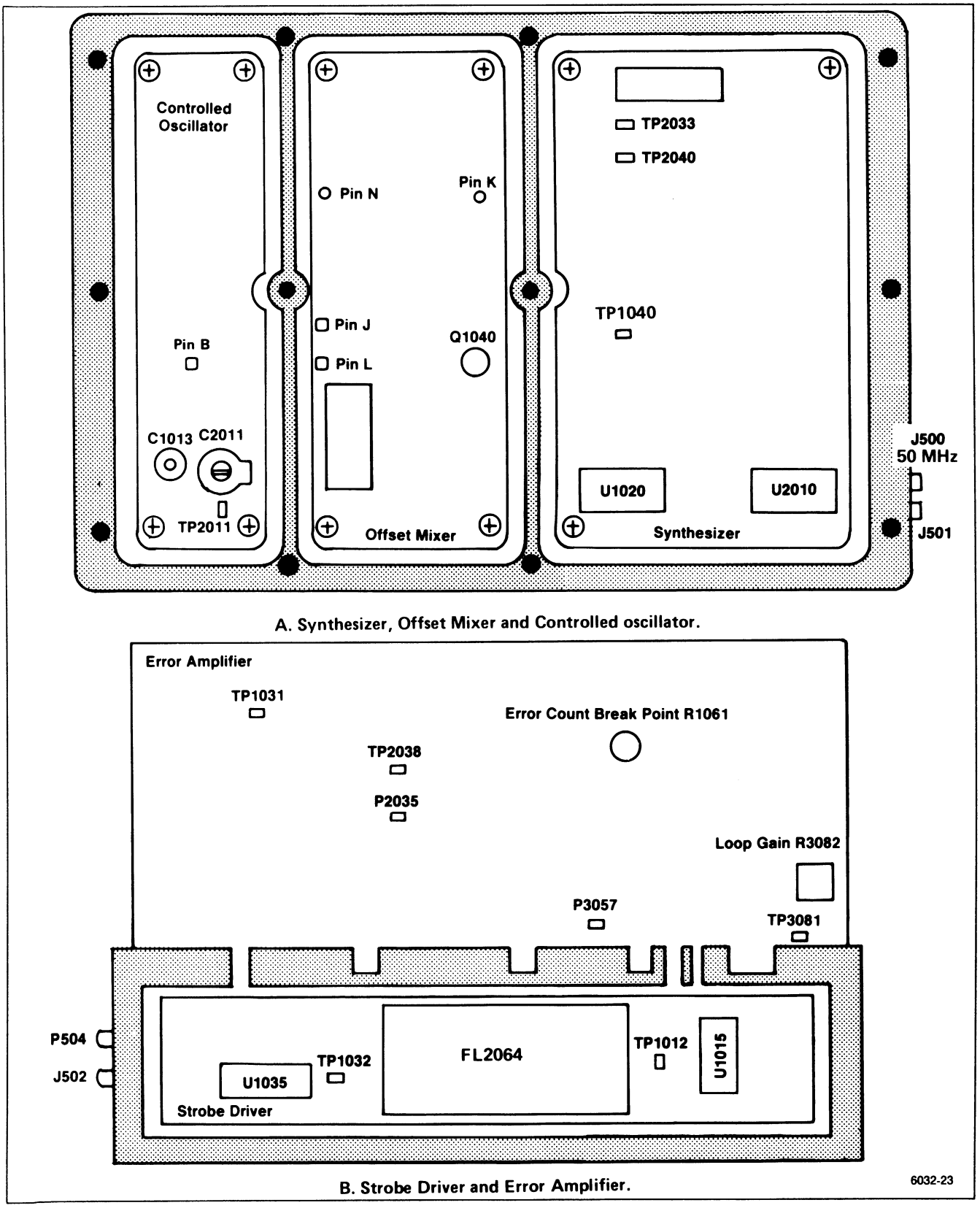


Figure 5-23. Phase Lock assembly adjustment and test point locations.

g. Error Amplifier — This procedure sets loop gain which is required when either the Phase Lock assembly, 1st LO, Phase Detector, or Error Amplifier is replaced.

(1) Set FREQ SPAN/DIV to 200 kHz then press <SHIFT> 0. The DIAGNOSTIC FUNCTIONS menu will now be displayed. Select menu item 3 (DIAGNOSTIC AIDS) and select 1st LO PHASE LOCK (sub-menu item 0). Phase lock should be disabled.

(2) Connect the test oscilloscope to TP2038 (Figure 5-23b) and set the test oscilloscope Time/Div to 20 ms. Check for a waveform with an amplitude that is approximately 6 V peak-to-peak.

(3) Press 10 dB/DIV to enable phase lock and note that the message indicates LOCK ENABLED. Connect the test oscilloscope to TP 3081 (Figure 5-23b) and vary R3082 from stop to stop and note that the beat note signal varies in amplitude. Press <SHIFT> to return to normal operation.

(4) Set the TIME/DIV to AUTO and FREQUENCY SPAN/DIV to 50 kHz.

(5) Remove P3057 (Figure 5-23b). This turns on the strobe to the Phase Gate. Set Loop Gain R3082 fully counterclockwise.

(6) Monitor TP3081 with the test oscilloscope. Sweep the test oscilloscope externally with the signal at TP2038 (U2048-6) shown Figure 5-23b. Set the test oscilloscope Time/Div to X-Y and Volts/Div to 0.5 V. Note the beat notes. Beat notes are produced by the difference between strobes from the phase lock (one every 5 MHz) and the particular frequency the 1st LO is tuned to.

(7) Tune the CENTER/MARKER FREQUENCY until the intensified marker on the oscilloscope is at the beatnote minimum.

(8) Reduce the FREQ SPAN/DIV to 20 MHz, and activate VIEW A.

(9) Check that the beat note is >0.5 V peak-to-peak. If the beat note does not meet this requirement, the Phase Gate may be defective. Adjust R3082 for a minimum but no less than 0.5 V signal.

(10) Replace P3057, disconnect the test oscilloscope trigger and probe connections. Ensure that P3057 is installed correctly; its absence will produce spurious responses on the display.

(11) Reduce FREQ SPAN/DIV to 200 kHz and ensure that phase lock occurs, by the absence of error message and a sweep. Replace the covers on the assembly and reinstall the module in the instrument. Perform the phase lock noise check as described in the Performance Check section.

(12) Set R1061 to midrange.

h. Check Strobe Driver — Excessive noise on the display and intermittent lock are indications that the strobe pulse from the Strobe Driver is noisy or low in amplitude. This can be caused by a mismatch in input or output impedance to the band-pass filter FL2064. The following procedure is required if the filter or any component that affects the input or output impedance match is replaced.

(1) With the instrument in phase lock mode (FREQ SPAN/DIV 200 kHz or less), monitor TP1032 with a test oscilloscope. Note the amplitude of the 5 MHz strobe signal. Amplitude of the sinusodial strobe signal is normally 5 V to 6 V peak-to-peak.

(2) If the strobe signal amplitude is low and noisy, change the value of select capacitors C1016, C1018, C1032 and C1034 to obtain the maximum strobe pulse amplitude at TP1032. These capacitors range from 3.3 pF to 27 pF.

(3) If the signal amplitude is still low, check the frequency at TP1012 with a frequency counter. Frequency must lie betwee 5.0067 MHz and 5.0188 MHz. The frequency is a function of the Controlled Oscillator assembly and counter U1022.

OPTION INSTRUMENTS ONLY

15. Adjust Option 07 VR Band Leveling
(R3024 on the VR Mother board #2)

a. Set the front-panel controls as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	200 kHz
REF LEVEL	−20 dBm
MIN RF ATTEN	0 dB
AUTO RESOLN	On
TIME/DIV	AUTO
VERTICAL DISPLAY	10 dB/DIV
VIEW A/VIEW B	On

b. Place the VR module on an extender, and connect the CAL OUT signal to the 50Ω RF INPUT via a 50Ω cable.

c. It may be necessary to set the FREQUENCY control to keep the 100 MHz signal at center screen.

d. Reset the RESOLUTION BANDWIDTH to 300 kHz, and the VERTICAL DISPLAY to 2 dB/DIV.

e. Set the front-panel AMPL CAL for a 7-division excursion of the 100 MHz signal.

f. Remove the 50Ω cable from the instrument and reconnect the CAL OUT signal to the 75Ω RF INPUT via a 75Ω cable. Push the 75Ω RF INPUT button.

g. Reset the REFERENCE LEVEL to +20 dBmV

h. Adjust R3024 on the VR Mother board #2 for a 7-division excursion of the 100 MHz signal.

i. Disconnect the 75Ω cable, disable the 75Ω input, and re-install the VR module in the spectrum analyzer.

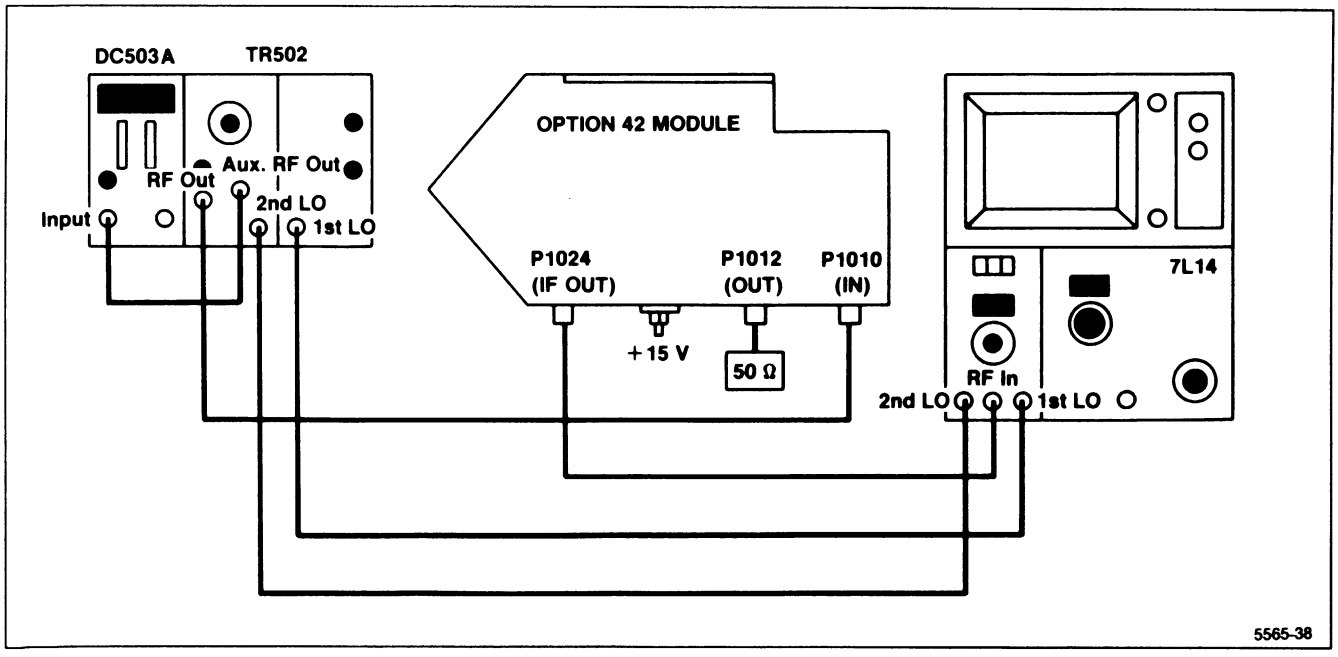


Figure 5-24. Option 42 adjustment test equipment setup.

16. Adjust Option 42 Module

(C1016, C1020 and C1024 in the Option 42 Module)

This adjustment need only be done after the circuit board in the module has been replaced.

a. Connect the test equipment as shown in Figure 5-24.

b. Set the front-panel controls of the test instrument as follows:

TR502	
Output Level –dBm	25
Var dB	0

7L14	
Center Frequency	0110
Freq Span/Div	2 MHz
Resolution	3 MHz
Vertical Display	2 dB
Reference Level	
Display A and B	Off

DC503A	
Ch A	
Term	50Ω
Slope	+
Atten	
Coupl	dc
Frequency A	
Autotrig	

c. Set the 7L14 Time/Div to Manual, and adjust the crt beam (dot) to center screen.

d. The DC503A readout should indicate approximately 110.000 MHz. Set Level as necessary, and set the 7L14 Center Frequency for an indication of 110.0 MHz.

e. Set the 7L14 Time/Div to calibrated display.

f. Adjust C1016, C1020 and C1024 for maximum amplitude, symmetry and bandpass (3 dB and 6 dB points).

(1) Adjust the bandwidth symmetry ±0.5 divisions (±1 MHz) at the 3 dB and 6 dB points.

(2) Check that bandwidth at the 3 dB point is 7.5 MHz, ±1.5 MHz.

(3) Check that 3 dB and 6 dB points are equidistant from center screen within 0.5 division.

(4) Check that any ripple present on the waveform is ⩽0.2 div (0.4 dB).

NOTE

A slight change in display may be observed when the cover is reinstalled on the module.

g. Check the Coupled Forward Gain (IF OUT port P1024).

(1) Set the 7L14 Spectrum Analyzer Reference Level to 0 dBm.

(2) Check that the display on the 7L14 is between 4 and 7 divisions in amplitude (–5 dBm, ±3 dBm).

h. Check the Input Compression.

(1) Increase the TR502 Output Level and REFERENCE LEVEL setting in 1 dB increments until the amplitude displayed by the 7L14 decreases by 0.5 division (1 dB compression).

(2) Check that the signal displayed on the 7L14 indicates ⩾0 dBm.

i. Check Forward Gain

(1) Return the TR502 Output Level to –25 and remove the connection to the module IF OUT.

(2) Connect a 50Ω termination to the IF OUT connector, P1024.

(3) Connect the OUT (P1012) connector to the 7L14 RF Input with a 50Ω cable.

(4) Adjust the 7L14 Reference Level until the displayed signal is near full screen (8 divisions).

(5) Check that the signal displayed on the 7L14 indicates –20 dBm to –23 dBm (–21.5 dBm ±1.5 dBm).

MAINTENANCE

INTRODUCTION

This section describes procedures for reducing and preventing instrument malfunction, troubleshooting methods, corrective maintenance, and procedures for recalibrating those assemblies that normally do not require routine calibration.

Do not place the instrument on its front panel as this may cause damage to the front-panel knobs.

Remove the cabinet as follows:

1. Remove the twelve torque screws holding the rear-panel casting, and pull the casting from the instrument.

2. Remove the eight screws holding on the feet, and the eight screws holding on the handles.

3. Pull the cabinet from the rear of the instrument.

4. Place the instrument on the bench and reconnect the power cord.

Table 6-1
RELATIVE SUSCEPTIBILITY TO STATIC DISCHARGE DAMAGE

Semiconductor Classes	Relative Susceptibility Levels[a]
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs. (Most Sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High-frequency bipolar transistors	5
JFET devices	6
Linear microcircuits	7
Low-power Schottky TTL	8
TTL (Least Sensitive)	9

Voltage Equivalent for Levels:

1 — 100 to 500 V	**4 — 500 V**	**7 — 400 to 1000 V (est)**
2 — 200 to 500 V	**5 — 400 to 600 V**	**8 — 900 V**
3 — 250 V	**6 — 600 to 800 V**	**9 — 1200 V**

[a] Voltage discharged from a 100 pF capacitor through a resistance of 100Ω.

Static-Sensitive Components

This instrument contains electrical components that can be damaged by static discharge. See Table 6-1 for the relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV can occur in unprotected environments.

CAUTION

Static discharge can damage any semiconductor component in this instrument.

Observe the following precautions to avoid damage:

1. Minimize handling of static-sensitive components.

2. Transport and store static-sensitive components or assemblies in their original containers, on metalized or conductive foam. Label packages that contains static-sensitive assemblies or components.

3. Discharge body static voltage by wearing a grounded wrist strap while handling these components. Static-sensitive assemblies or components should be handled and serviced only at static free work stations by qualified service personnel.

4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.

5. Keep the component leads shorted together whenever possible.

6. Pick up components by the body, never by the leads.

7. Do not slide the components over any surface.

8. Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.

9. Use a soldering iron that is connected to earth ground.

10. Use only special anti-static suction type or wick type desoldering tools.

PREVENTIVE MAINTENANCE

Preventive maintenance consists of cleaning, visual inspection, performance check, and if needed a recalibration. The preventive maintenance schedule that is established for the instrument should be based on the environment in which the instrument is operated and the amount of use. Under average conditions (laboratory situation) a preventive maintenance check should be performed every 2000 hours of instrument operation.

Elapsed Time Meter

A 5000 hour elapsed time indicator, graduated in 500 hour increments, is installed on the Z-Axis/RF Interface circuit board. This provides a convenient way to check operating time. The meter on new instruments may indicate from 200 to 300 hours elapsed time because most instruments go through a factory burn-in time to improve reliability. This is similar to using aged components to improve reliability and operating stability.

Cleaning

Clean the instrument often enough to prevent dust or dirt from accumulating in or on it. Accumulation of dirt and grease acts as a thermal insulating blanket and prevents efficient heat dissipation. It also provides high resistance electrical leakage paths between conductors or components in a humid environment.

Exterior. Clean the dust from the outside of the instrument by wiping or brushing the surface with a soft cloth or small brush. The brush will remove dust from around the front-panel selector buttons. Hardened dirt may be removed with a cloth dampened in water that contains a mild detergent. Abrasive cleaners should not be used.

Interior: Clean the interior by loosening accumulated dust with a dry soft brush, then remove the loosened dirt with low pressure air to blow the dust clear. (High velocity air can damage some components.) Hardened dirt or grease may be removed with a cotton tipped applicator dampened with a solution of mild detergent in water. Do not leave detergent on critical memory components. Abrasive cleaners should not be used. If the circuit board assemblies need cleaning, remove the circuit board by referring to the instructions under Corrective Maintenance in this section.

After cleaning, allow the interior to thoroughly dry before applying power to the instrument.

CAUTION

Do not allow water to get inside any enclosed assembly or components such as the hybrid assemblies, RF Attenuator assembly, potentiometers, etc. Instructions for removing these assemblies are provided in the Corrective Maintenance part of this section. Do not clean any plastic materials with organic cleaning solvents such as benzene, toluene, xylene, acetone or similar compounds because they may damage the plastic.

Lubrication

Components in this instrument do not require lubrication.

Fixtures and Tools for Maintenance

Table 6-2 lists kits and fixtures that are available to aid in servicing the spectrum analyzer.

Visual Inspection

After cleaning, carefully check the instrument for such defects as defective connections, damaged parts, and improperly seated transistors and integrated circuits. The remedy for most visible defects is obvious. If heat-damaged parts are discovered, try to determine the cause of overheating before the damaged part is replaced; otherwise, the damage may be repeated.

Transistor and Integrated Circuit Checks

All transistors and integrated circuits are soldered on the boards to prevent pin contact problems. Periodic checks of the transistors and integrated circuits is not recommended. The best measure of performance is the actual operation of the component in the circuit. In most cases any degradation in performance will be detected by the microcomputer when it runs its power up routine. Performance of these components is also checked during the performance check or recalibration; any sub-standard transistors or integrated circuits will usually be detected at that time.

When handling a MOS FET, keep the shorting strap in place until the transistor is soldered in the circuit board.

Table 6-2
SERVICE KITS AND TOOLS

Nomenclature	Tektronix Part No.
Service Kit consisting of:	006-3286-01
1 Front panel extender	067-0973-00
1 Power module extender	067-0971-00
1 Accessories Interface extender	067-0972-00
1 Ribbon cable	175-2901-00
3 Coaxial cables, Sealectro male-to-Sealectro female	175-2902-00
1 VR module handle	367-0285-00
1 Circuit board extender assembly kit consisting of:	672-0865-01
1 Left extender board	670-5562-00
2 Right extender boards	670-5563-00
1 Right GPIB extender board	670-8493-00
1 Frame extrusion for circuit board extender	426-1527-00
6 Screws, panhead with flat and lockwashers	211-0116-00
Screwdriver, flat, with 1/4 to 3/8-inch bit	
Screwdriver, Posidrive® 440-2	
Wrench, 5/16-inch open-end	
Hex drive wrenches, 3/32, 5/64,7/64-inch	
Torque Wrench Kit	003-1324-00

Performance Checks and Recalibration

The instrument performance should be checked after each 2000 hours of operation or every 12 months if the instrument is used intermittently to ensure maximum performance and assist in locating defects that may not be apparent during regular operation. Instructions for conducting a performance check are provided by the Performance Check section of the service instructions.

Saving Stored Data in Battery-Backup Memory

If the battery on the Memory board is removed while the board is not powered up, data stored in battery-backed up memory will be lost. A program for storing data on tape is provided at the end of this section.

TROUBLESHOOTING

The spectrum analyzyer contains firmware that will troubleshoot the frequency control system and the power supply. Troubleshooting procedure for this system and the power supply is provided in the Diagnostics part of this section. Also included with this part is a description of the trace modes and their actions. After the defective assembly or component has been located, refer to the Replacing Assemblies and Sub-assemblies part of this section for removal and replacement instructions.

Troubleshooting Aids

Diagrams — Functional block and circuit diagrams, on foldout pages in the Diagrams section, contain significant waveforms, voltages, and logic data information. Conditions for getting the data are provided on the diagram or adjacent to it. Refer to the Replaceable Electrical Parts list section for a description of all assemblies and components. Diagrams are arranged in signal flow sequence and by sections, such as RF section, IF section, frequency control section, etc., with an accompanying functional block diagram.

Schematic diagrams list the Tektronix Part No. (670-xxxx-) for the assembly or board along with the assembly number (e.g. A50) and name. The last two digits or suffix of the part number are not indicated on the diagram, however, they are listed in the Electrical Parts section. These two digits reflect changes or modifications to the assembly or board. When a change is made to the assembly the suffix rolls one digit. The diagram indicates these changes with a grey tint drawing of the original circuit or if a component changes value the symbol is enclosed with a grey tint box. When a major modification is made to an assembly or board and it is no longer compatible with earlier instruments a new part number is assigned and a separate schematic with associated illustrations are added, all diagrams indicate the new part number and the instrument serial number break. If the assembly is compatible with earlier instruments and the change is significant enough to require a separate schematic, this will also be identified.

NOTE

Corrections to the manual and instrument modifications are documented by adding correction pages behind a tabbed page, labeled Change Information, at the rear of the manual. Check this Change Information section for changes to the manual or the instrument.

Circuit Board Illustrations and Component Locator Charts — Electrical components, connectors, and test points are identified on circuit board illustrations that are located on the inside fold of the corresponding circuit diagram or the back of the preceding diagram. A grid on the circuit board illustration and the circuit schematic, plus a look-up table, provide the means to quickly locate components on either the diagram or the circuit board.

In most cases, circuit numbers are assigned according to the physical location of the component on the board or assembly. The first digit designates the row of a grid, the second the column, with the last two reserved as an expander. Three digit numbers designate chassis mounted components.

Diagnostics — The spectrum analyzer contains firmware that will assist in locating trouble in the frequency control system and the power supply. This diagnostic information is part of this section.

General Troubleshooting Techniques

Before using test equipment, to measure across static-sensitive components or assemblies, be certain that voltages or current supplied by the test equipment does not exceed the limits of the components to be tested.

Try to isolate the problem to a component through signal analysis. Determine that circuit voltages will not damage the replacement.

Semiconductor Checks — Semiconductor failures account for the majority of electronic equipment failures. Most semiconductors are soldered to the boards to reduce pin contact problems. The following guidelines should be observed if you substitute any of these components.

1. Turn the power off before removing an assembly or board.

2. Use a de-soldering tool and 25 W or less soldering iron to remove the components.

3. Use only good components for substitution. Be sure the new component is inserted into the board properly before soldering. Refer to the manufacturer's data sheet for integrated circuit and transistor lead configuration.

NOTE

If a substitute is not available, check the transistor or MOS FET with a dynamic tester such as the TEKTRONIX Type 576 Curve Tracer. Static type testers, such as an ohmmeter, can be used to check the resistance ratio across some semiconductor junctions if no other method is available, however, DO NOT MEASURE RESISTANCE ACROSS A MOS FET to avoid damage from static charges. Use the high resistance ranges (R × 1k or higher) so the external test current is limited to less than 6 mA. If uncertain, measure the external test current with an ammeter. Resistance ratios across base-to-emitter or base-to-collector junctions usually run 100:1 or higher. The ratio is measured by connecting the meter leads across the terminals, note the reading, then reverse the leads and note the second reading.

Diode Checks — Most diodes can be checked in the circuit by taking measurements across the diode and comparing these with voltages listed on the diagram. Forward-to-back resistance ratios can usually be taken by referring to the schematic and pulling appropriate transistors and pin connectors to remove low resistance loops around the diode.

CAUTION

Do not use an ohmmeter scale with a high external current to check diode junctions. Do not check the forward-to-back resistance ratios of mixer diodes.

Diagnostic Firmware

The firmware in the spectrum analyzer provides diagnostic routines that can be used with the Diagnostic part of this section to troubleshoot the Frequency Control system and diagnose Power Supply problems. This part follows General Troubleshooting information. Refer to this part to help isolate problems within this loop. The following are also some general suggestions that may help isolate a problem when troubleshooting.

Troubleshooting Steps

1. Ensure that the problem exists in the spectrum analyzer by checking the operation of associated test equipment.

2. Try to isolate the problem to a circuit or at least board level by evaluating operational symptoms; for example, absence of the frequency dot could be caused by a malfunction in the video summing stage, the marker generator, or switching circuits.

3. Three levels of block diagrams are provided to aid in understanding the theory of operation. The most detailed level is adjacent to the schematic and usually provides signal and voltage levels at critical points within the circuits. Signal levels are usually the levels required to produce full screen deflection.

4. Instructions on how to remove or replace those assemblies which are not obvious, are provided in this section. Refer to this part before removing any assembly for testing or repairing.

5. Visually inspect the area or assembly for such defects as broken or loose connections, improperly seated components, overheated or burned components, chafed insulation, etc. Repair or replace all obvious defects. In the case of overheated components, try to determine the cause of the overheated condition and correct before applying power.

6. Use successive electrical checks to try to locate the problem. An oscilloscope is a valuable test item for evaluating circuit performance. If applicable, check the calibration adjustments; however, before changing an adjustment note its position so it can be returned to its original setting. This will facilitate recalibration after the trouble has been located and repaired.

7. Determine the extent of the repair needed; if complex, we recommend contacting your local Tektronix Field Office or representative. If minor, such as a component replacement, see the Replaceable Parts list for replacement information. Removal and replacement procedure of the assemblies and sub-assemblies are described under Corrective Maintenance.

CAUTION

When measuring voltages and waveforms, use extreme care with the placement of test probes. Because some circuit boards have a high component density, access to points in some circuits is limited. A test probe could accidentally short a circuit and generate transient voltages that can destroy many static-sensitive components.

DIAGNOSTICS

This part consists of explanations and procedures for troubleshooting the frequency control system and the power supply using diagnostic firmware in the spectrum analyzer.

TROUBLESHOOTING USING THE ERROR MESSAGE DISPLAY

Introduction

This part contains procedures for troubleshooting the frequency control system and the power supply. When the microprocessor detects a failure or error in the Frequency Control loops or a failure in the Power Supply voltages it will cause the spectrum analyzer to display an error message near center screen for a few seconds; this is followed by an error status message near the top of the screen which remains as long as the error or problem exists.

These error messages pertain to problems that exist under current instrument operational modes or front panel settings; for example, an error that pertains to the hardware in the phase lock loop will exist only when the instrument is in the phase lock mode (narrower span/div settings).

The following troubleshooting procedures are keyed to the brief error messages. Some problems may produce more than one error message in which case the spectrum analyzer will display only the predominant error. A listing of all error messages will be displayed if you press <SHIFT> . (decimal point). Combinations of error messages may help determine and expedite the process of finding the problem.

Some of the procedures use firmware diagnostics aid routines which can only be accessed by pressing <SHIFT> 0 and selecting menu item #3 (DIAGNOSTIC AIDS).

Combination of Error Messages

The following is a list of error message combinations and suggestions as to their cause. If the problem is not resolved with the following suggestions, or if the combination of error messages displayed is not covered, proceed to the listing of each error message and how to troubleshoot the problem.

POWER SUPPLY OUT OF REGULATION
(in combination with any other message/s)

A missing or inaccurate supply voltage is probably causing the other errors. Proceed to the POWER SUPPLY OUT OF REGULATION procedure.

TUNING FAILURE — 1ST LO
and
TUNING FAILURE — 2ND LO

The CF Control board is probably the cause, particularly if signals do not tune or do not tune smoothly. The problem is probably the voltage reference or in the digital control section.

Procedure Format

The format for these procedures is such that the problem is diagnosed in a descending order. The aim, to isolate a problem down to one part of the system, usually an assembly (such as a module or board) or a functional section of the assembly. After the problem has been isolated to the assembly or circuit level, refer to the diagrams and circuit description, as suggested under General Troubleshooting Techniques, for further isolation.

The procedures are structured as follows:

Error Message

Troubleshooting Procedure

1. _____

   a. _____

   b. _____

      (1) _____

      (2) _____

2. _____

Steps at the same level are either sequential or alternative steps, based on measurement or observation. Proceed to the lower-level steps only if the conditions of the higher-level steps are met. If the conditions are not met, proceed to the next step at the same level. An "(E)" at the end of a step, signifies this is as far as this procedure can take you to locate the problem.

Several of the troubleshooting procedures require that frequencies be counted and compared to either an expected value, or the number counted by the spectrum analyzer's internal counter. The frequencies can differ by up to (1×10^{-5} + counter accuracy) in the standard instruments, and up to (1×10^{-7} + counter accuracy) in Option 05 instruments.

Some failures, in the frequency control system, may appear only at specific oscillator frequencies. If this occurs, in a higher frequency range, the fundamental frequency of the appropriate oscillator should be determined so it can be set to the same frequency in the lower bands. This can be done by:

(1) Press <SHIFT> 0 and #0, then select either the 1st LO readout (menu item #1) or the 2nd LO readout (menu item #2).

(2) After noting the frequency of the oscillator, press <SHIFT> 0 and #0, and select center frequency readout to return to the normal center frequency readout mode.

Since the instrument's power is usually switched on and off during troubleshooting, the power-down settings, that are automatically stored in register 0 of battery-backed-up memory, should be recalled so the instrument settings and operating mode duplicate those that existed when the error message was generated.

The following describes each error message and the procedures recommended to locate the problem.

POWER SUPPLY OUT OF REGULATION

Any out-of-tolerance voltage will cause this error message to be displayed. A power supply status circuit within the power supply will change the status LED on the Z-Axis board to red when any supply except −17 V changes by more than 25%. An error message will be also be displayed. An apparent power supply failure can be produced when either the supply fails or a circuit demands excessive current and blows a protective fuse or produces a current limit condition. The following procedure should determine those voltages that are out of range and whether the failure is in the supply or in a circuit outside the supply. Use a DVM to measure voltages.

Troubleshooting procedure

WARNING

The spectrum analyzer uses a high efficiency power supply, with the primary ground potential different from chassis or earth ground. An isolation transformer, with a turns ratio of 1:1 And a 500 VA minimum rating, should be used between the power source and the spectrum analyzer power input receptacle. The transformer must have three-wire input and output connectors with a through ground between input and output. Stancor GIS1000 is an example of a suitable transformer. A jumper should also be connected between the primary ground side to chassis ground (emitter of Q2061 and the ground terminal of the input filter FL301).

If the power supply is separated from the instrument and operated on the bench, hazardous potentials exist within the supply for several seconds after power is disconnected. This is due to the slow discharge of capacitors C6101 and C6111. DS5112 (next to C6111) lights when the potential exceeds 80 V.

1. Verify that the power supply status LED, on the Z-Axis board, is red. If the LED is green, there is probably a failure in the microprocessor interface. (E)

2. Measure the power supply voltages at the test points on the Z−Axis board. To access the test points, remove the hold down cover over the Sweep and Z−Axis boards.

WARNING

Hazardous voltages (300 V and 100 V) are present on the Z-axis board.

The ranges for each supply are listed in Table 6-3. These are tolerance limits which are much tighter than the limits used by the power supply sensing circuit. A supply that exceeds these limits may not trigger the error message or cause the instrument to malfunction. The +15 V supply is adjustable and affects the other supplies. Refer to the Adjustment Procedure section of the manual for adjustment information if a supply is just out of tolerance.

a. If all supplies are within limits and the power supply status LED is red, the problem is probably in the power supply status circuit on the Z−Axis board. R1065 may be misadjusted; adjust R1065 to see if the LED changes to green. If it changes, set R1065 at the center of the "green" range. (E)

b. If the +17 V or −17 V supply and any other supply or supplies are inaccurate, or, if both the +9 V and +5 V supplies are inaccurate, the trouble is likely in the Power Supply. (E)

c. If the voltage is high (in absolute value), the trouble is probably in the Power Supply. (E)

d. If the voltage from a fused supply is inaccurate, the trouble is probably in the Power Supply. (E)

e. If the voltage from a fused supply is absent, it indicates the fuse could be blown. To access the fuses, remove the cover at the top left hand corner of the Power Supply module (as viewed from the front of the instrument). A blown fuse generally indicates that one of the circuits that this supply furnishes is defective; however, a fuse may open without an overcurrent condition. Replace the fuse and try again. If the fuse blows, the trouble is definitely in one of the circuits the supply furnishes.

If the fuse is not blown and the voltage is still absent, it indicates the trouble is the Power Supply. (E)

Table 6-3
POWER SUPPLY RANGES

Supply	Range	Test Point	Circuit Protection
+300 V	280 V to 310 V	TP1052	Fuse (F1033)
+100 V	95 V to 105 V	TP1048	Fuse (F1035)
+17 V	16.8 V to 18.6 V	TP1047	Fuse (F2013)
15 V	14.85 V to 15.15 V	TP1046	Current limit
+9 V	8.5 V to 10.5 V	TP1011	Fuse (F1017)
+5 V	4.8 V to 5.2 V	TP1044	Current limit
−5 V	−4.8 V to −5.2 V	TP1036	Current limit
−7 V	−7 V to −8.5 V	TP1037	Fuse (F1013)
−15 V	−14.85 V to −15.15 V	TP1035	Current limit
−17 V[a]			Fuse (F3038)
Gnd		TP1034	Ground Reference

f. If the voltage from a current limited supply is absent or low, the problem could be the supply, or circuits the supply furnishes may be drawing excessive current. Turn the POWER off, then disconnect the suspect assemblies or modules from the supply and re-measure the voltage; or, remove the Power Supply from the instrument and measure the unloaded voltages on the Power Supply connector.

(1) If the supply voltage is correct with assembly or module removed, or when the voltage with the power supply removed is normal, the circuits this supply furnishes are causing the problem. (E)

(2) If the voltage for the unloaded supply voltage is still inaccurate, the power supply is defective. (E)

TUNING FAILURE — 1ST LO

The 1st LO is set by a combination hardware/software loop. There are two distinct hardware blocks to the loop: the block that measures the oscillator frequency and the block that sets the oscillator to frequency. The microprocessor system closes the loop by determining how far the oscillator must be moved to bring it to the desired frequency. Setting is an iterative process wherein the microprocessor indirectly counts the 1st LO, moves it as needed, and counts again. The 1st LO Tuning Failure error message is displayed when the 1st LO has not been set correctly after a number of iterations which varies with instrument settings.

The 1st LO Control Diagnostic Aid displays data on the crt screen which can be used to determine which part of the loop has failed. A typical display follows Table 6-4.

The first two lines list the voltage to be expected at the output of the 1st LO section of the Center Frequency Control and the voltage across the sense resistor of the 1st LO Driver. The nominal values are based on the Desired 1st LO Freq and the nominal tuning sensitivity of the oscillator.

Table 6-4
POWER SUPPLY
EDGE CONNECTOR VOLTAGES

Supply	Pin on Edge Connector
+300 V	W
+100 V	20
+17 V	U
+15 V	C, D, 3
+9 V	T, 16
+5 V	R, S, 14, 15
−5 V	H
−7 V	17
−15 V	E, F, 6

[a] The −17 V supply is not monitored by the power supply status circuit nor does it have a test point on the Z-axis board. If this supply fails, the cooling fan will not run. The fan will also not run if the ambient temperature is low. The −17 V supply will probably affect other supplies as well.

1ST LO CONTROL DIAGNOSTIC AID		
	NOMINAL	DAC SET
TUNE VOLTS	−6.79 V	−6.80 V
SENSE VOLTS	3.43 V	3.43 V
	DESIRED	COUNTED
1ST LO FREQ	2.720 504 GHZ	2.719 735 GHZ
MIXER FREQ	45.896 MHZ	46.665 MHZ
1ST LO SETTING ACCURACY		4.981 MHZ
AUXILIARY SYNTHESIZER		212.800 MHZ
PRESS "SHIFT" TO EXIT		

The DAC Set values are based on the setting of the 1st LO tuning DACs. The DAC Set values can differ from the Nominal values because the system cannot be exactly calibrated, the tuning sensitivity of the oscillator is possibly not its nominal value, and the DACs will be moved in an attempt to set the oscillator.

The Desired 1st LO Freq is the frequency to which the processor is trying to move the oscillator. The Counted 1st LO Freq is the frequency the microcomputer has calculated from, the internally counted harmonic mixer output frequency, the Auxiliary Synthesizer frequency, and the assumed harmonic number of the Auxiliary Synthesizer. Because of this last assumption, if the 1st LO is not near the Desired Frequency, the Counted Frequency will not be the actual oscillator frequency, even though the counter is functioning.

The Desired Mixer Freq is the difference between the the Desired 1st LO Freq and the nearest harmonic of the Auxiliary Synthesizer. (The Auxiliary Synthesizer harmonic will always be higher in frequency than the desired 1st LO frequency.)

The 1st LO Setting Accuracy is the maximum permitted difference between the actual and desired LO frequencies. The setting process will end when the difference becomes less than, or equal to, this value. The tolerance depends on frequency span and band.

The Auxiliary Synthesizer Freq is the frequency that is programmed into the +N synthesizer.

This troubleshooting procedure should localize a problem to the oscillator, the oscillator setting block, or the oscillator counting block. If the failure is not in the oscillator, it is further localized within one of the hardware blocks.

Troubleshooting Procedure

1. Press <SHIFT> 0 and #3 to display the Diagnostic Aids menu, then select #1 to display the 1st LO Control Diagnostic Aid information.

2. If the Counted 1st LO Freq is within the 1st LO Setting Accuracy of the Desired Freq readout, press <SHIFT> to return to normal operation. Now determine if the error occurs, for the same center frequency, at frequency spans/division above 5 MHz only, or at spans less than 5 MHz/div.

   a. If the frequency control error occurs only at frequency spans of 5 MHz/div or more, the capacitor switching relay, on the 1st LO assembly, is probably shorted. (E)

   b. If the error occurs with a frequency span/div of 5 MHz or less, the 1st LO is probably defective. (E)

3. Measure the voltage across the sense resistor (R1040) on the 1st LO Driver board. If this voltage is within 50 mV of the DAC Set value, measure the frequency on the 1ST LO Output connector. This measured frequency should be within 50 MHz of the frequency calculated by multiplying 800 MHz/V by the voltage that was measured across the sense resistor R1040.

a. If the calculated and measured frequencies are within 50 MHz of each other and the measured frequency agrees with the internally counted 1st LO Freq readout or differs from it by a multiple of the Auxiliary Synthesizer Freq, return to normal operation (by pressing <SHIFT>). Now attempt to calibrate the CF Control board and the 1st LO Driver board by pressing <SHIFT> 0 and select #1 from the menu for the FREQUENCY LOOPS CAL, and #1 again for the CF Control board, or #2 for the 1st LO Driver board. Exit from the CF Control board calibration routine by pressing <SHIFT> when the step for R4040 is displayed. If you are able to complete the calibration routine, check to see if the error message is still present. If it is, or if the calibration routines cannot be completed, continue troubleshooting with step 3c. (E)

b. If the calculated and measured frequencies are within 50 MHz, but do not meet the above condition in step 3a, measure the Auxiliary Synthesizer output frequency at P1060 on the Auxiliary Synthesizer board.

(1) If the Auxiliary Synthesizer output frequency is correct, measure the input frequency from the Harmonic Mixer with a spectrum analyzer, at the cable connection to P261 on the Auxiliary Synthesizer board. (A counter would probably give an erroneous reading because of the harmonic mixing process). The frequency measured with the spectrum analyzer should equal the sum of the Desired Mixer Freq and the measured 1st LO frequency, less the Desired 1st LO Freq, if the calculated frequency is between 10 MHz and 90 MHz. If the calculated frequency is outside the 10 MHz to 90 MHz range, the 1st LO frequency is far from the desired value. Repeat the previous steps in this procedure.

(a) If the Harmonic Mixer output frequency is correct, measure the frequency at edge connector 15, on the Auxiliary Synthesizer board, with a counter. This should be 1/100th of the Harmonic Mixer output frequency.

(b) A correct frequency measurement indicates the Counter board is defective. (E)

(c) An incorrect frequency measurement indicates the Auxiliary Synthesizer is defective. (E)

(d) The Harmonic Mixer is probably defective if no signal is present at the output or the signal frequency is incorrect. (E)

(2) If the output frequency, at P1060 is incorrect, measure the tune voltage for the 200—220 MHz VCO, between TP1066 and TP1074 on the Auxiliary Synthesizer board. The range of the tuning voltage is normally +5 V to +12 V.

(a) If the tune voltage is within the center of its normal range and the output frequency at P1060 is stable (varies no more than 1—2 Hz), the programmable divider in the phase-locked loop is probably defective. (E)

(b) If the tune voltage is in the center portion of its normal range and the output frequency at P1061 is unstable, the loop amplifier is probably defective. (E)

(c) If the tune voltage and oscillator frequency are at the end or outside their range, in the same direction (high or low), C1070 in the VCO may be misadjusted. If adjustment of the capacitor does not correct the problem it is not in the VCO but somewhere else in the loop. (E)

(d) If the tuning voltage and the Auxiliary Synthesizer frequency are in opposite directions from the center of their respective ranges (8.5V and 210 MHz), the VCO is probably defective. (E)

(e) If the calculated and measured frequencies differ by more than 50 MHz, remove the jumper plug P3043 on the 1st LO Driver board and measure the oscillator current.

CAUTION

The oscillator coil has significant inductance. Interrupting the oscillator current will generate high voltage. Remove/replace P3043 or connect/disconnect a current meter after the power is off. (Typical voltages at P3043 can range as high as 35 V.)

The coil current should be: 40 mA/V, where the voltage is the sense-resistor voltage as previously measured across R1040. The measured current should be within 1% of this value.

(3) If the measured and calculated currents are within 1%, return to normal operation (by pressing <SHIFT>) and determine if the frequency control error occurs with frequency span/div of 5 MHz or less, or above 5 MHz/div, with the same center frequency.

(a) If the frequency control error occurs only with frequency spans of 5 MHz/div or less, one of the noise filter capacitors on the 1st LO Assembly is probably defective. (E)

(b) If the error occurs with frequency spans greater than 5 MHz/div, the 1st LO is probably defective. (E)

(4) If the measured and calculated currents are not equal, the problem is likely in the final stage of the LO Driver. (E)

4. Measure the 1st LO tuning voltage at edge connector 47, of the Center Frequency Control board. This voltage should be within 200 mV of the listed DAC Set value.

a. If the voltage is within this limit, failure of the 1st LO Driver board is indicated. (E)

b. If the voltage is not within the limit, failure of the Center Frequency Control board is indicated. (E)

TUNING FAILURE — 2ND LO

The 2nd LO is set by a combination hardware/software loop. There are two distinct hardware blocks in the loop; the block which measures the oscillator frequency and the block which sets the oscillator to frequency. The microprocessor closes the loop by determining how far the oscillator must be moved to bring it to the desired frequency. Setting is an iterative process wherein the microprocessor counts the oscillator frequency, moves it as needed, and counts again. The error message is displayed if the 2nd LO is not set to the desired frequency after a number of iterations, depending on instrument settings.

The 2nd LO Control Diagnostic Aid displays data which can be used to determine which part of the loop has failed. A typical display is shown below. Press <SHIFT> 0 and select #3 from the menu for the DIAGNOSTIC AIDS, then select #2 for the 2nd LO Control.

2ND LO CONTROL DIAGNOSTIC AID

	NOMINAL	DAC SET
TUNE VOLTS	0.01 V	0.19 V
	DESIRED	**COUNTED**
2ND LO FREQ	2.182 000 GHZ	2.182 140 GHZ
OFFSET FREQ	18.000 000 MHZ	17.860 MHZ
OFFSET SETTING ACCURACY		540.672 KHZ

PRESS "SHIFT" TO EXIT

The Tune Volts is the voltage that would be expected at the output of the 2nd LO section of the Center Frequency Control. The Nominal voltage is the value needed for the Desired frequency of the oscillator in a perfectly calibrated system. The DAC Set voltage should be produced by the present setting of the 2nd LO tuning DACs. The DAC Set voltage may differ from the Nominal value because the system may not fully calibrated and the DACs will be moved to try to set the oscillator.

The Desired 2nd LO Freq is the frequency to which the microcomputer is trying to move the oscillator. The Counted 2nd LO Freq is that frequency the microcomputer has calculated from the Counted Offset Freq.

The Offset Freq is the frequency of the low-frequency offset VCO in the 2nd LO Assembly. In the 2182 MHz LO, this frequency is the difference between 2200 MHz and the LO frequency. Again, the Desired Freq is the frequency the microcomputer is trying to set the offset, and the Counted Freq is the value read by the internal counter.

The Offset Setting Accuracy is the maximum permitted difference between the actual and desired offset frequencies. The setting process ends when the difference becomes less than or equal to this value. The tolerance depends on frequency span and band.

The following procedure should localize the failure to the 2nd LO assembly, the hardware setting block, or the hardware counting block.

Troubleshooting Procedure

1. Display the diagnostic information for the 2nd LO control loop as outlined above.

2. If the Counted Offset Freq and the Desired Offset Freq are within the Offset Setting Accuracy, the 2nd LO probably has failed.

3. If the Counted Offset Freq is within 100 kHz of the Desired Offset Freq, make sure that P1048 is properly seated on J1048. If the fine tune ground lead is not making good contact, the tuning voltage can shift sufficiently to cause setting failures. (E)

4. If the Counted Offset Freq readout is within 100 kHz of the Desired Offset Freq, the oscillator may be out of calibration. Return to normal operation by pressing <SHIFT>. Try to calibrate the 2nd LO by pressing <SHIFT> 0 and selecting #1 from the menu for the FREQUENCY LOOPS CAL, then selecting #4 (2nd LO). Now, follow the instructions of the displayed messages. If you are able to complete the calibration routine, check to see if the error condition still exists. If the error is still there or you where unable to complete the calibration routine, proceed to the next step. (E)

5. Measure the 2nd LO Tune Volts at TP1044 on the Center Frequency Control board.

a. If the 2nd LO tuning voltage is within 200 mV of the DAC Set value, measure the 2nd LO frequency at the front-panel 2ND LO Output connector.

(1) If the measured frequency does not agree with the internally Counted readout, the Counter board is probably at fault. (E)

(2) If the frequency agrees with the Counted value, measure the mixed down frequency at the cable going to P513 on the Counter board. This frequency should equal the sum of the Desired Offset Freq and the Desired 2nd LO Freq, less the measured 2nd LO frequency.

(a) If this frequency is present, measure the 2182 MHz oscillator tuning voltage on the feedthrough capacitor C2203 between the 16—20 MHz Phase Lock circuit and the 2182 MHz Microstrip Oscillator in the 2182 MHz Phase Locked 2nd LO Assembly. The normal range of this voltage is 0 V to −12.5 V. With the phase locked loop unlocked, this voltage will probably be slightly outside one end of the range.

(i) If the absolute value (magnitude) of the tuning voltage and the oscillator frequency are off in the same direction from the centers of their respective ranges (−6 V and 2182 MHz), the Microstrip Oscillator has probably failed. (E

(ii) If the absolute value (magnitude) of the tuning voltage and the oscillator frequency are off in the opposite direction from the center or their respective ranges (−6 V and 2182 MHz), some other part of the lock loop, besides the Microstrip Oscillator, has probably failed. (E)

(b) If the mixed-down frequency is absent, either the 2200 MHz Reference, the 2182 MHz Microstrip Oscillator or the 2200 MHz Reference Mixer probably has failed. (E)

b. If the tuning voltage is not within 200 mV of the DAC Set value, the Center Frequency Control board probably has failed. (E)

PHASE LOCK FAILURE — 1ST LO

The following procedure assumes that the oscillator is at the correct frequency, so the problem must be in the phase lock system.

The following crt display of the 1st LO Phase lock Diagnostic Aid displays data for troubleshooting the 1st LO phase lock loop.

```
1ST LO PHASE LOCK DIAGNOSTIC AID
1st LO FREQ          2.072 000 000 GHZ
STROBE FREQ          5.016 949 MHZ
LOCK DISABLED          PRESS
                       10 dB/DIV
                       TO
                       ENABLE

PRESS "SHIFT" TO EXIT
```

While the troubleshooting information is displayed, the 1st LO is repetitively being stepped ±750 KHz. If LOCK DISABLED is displayed, the lock loop is open between the output of the phase gate and the input to the FM coil. If lock is enabled, the loop is closed, and the fourth line of the display changes to LOCK ENABLED PRESS "10 dB/DIV" TO DISABLE.

The 1st LO Freq readout is the frequency the oscillator should be at when locked. The frequency that is measured at the front-panel 1ST LO Out connector will not check exactly with this value because the oscillator is unlocked and stepping in frequency.

The Strobe Freq is the frequency at P502 and P504 of the Phase Lock module.

This procedure should help localize the failure to the Phase Gate or to a section of the phase lock circuitry.

Troubleshooting procedure

Before troubleshooting data on the phase lock loop is displayed, the Freq Span/Div must be in those spans that enable the phase lock mode (200 kHz or less for band 1).

1. Press <SHIFT> 0 and select #3 from the menu to bring up the DIAGNOSTIC AIDS menu, then select #0 to display the 1st LO PHASE LOCK diagnostic aid information.

2. With an oscilloscope, examine the signal at P242 on the Phase Gate. Beat notes (bursts of signal at up to 500 kHz) at a 10 Hz rate should be present as the oscillator is stepped. Beat note amplitude should be about 6 V peak-peak. The amplitude of the positive and negative peaks should not differ by more than 20%.

a. If beat notes are present, press 10 dB/DIV to enable the lock. Check the Error Amplifier output at TP2037, on the Error Amplifier board in the Phase Lock module. Output signal amplitude should be approximately 6 V peak-peak and its frequency should be 10 Hz. The up and down out-of-range signals, on edge connectors 8 and 10 of the Error Amplifier board, should be toggling between 0 V and +5 V.

(1) If there is a signal at TP2037 but one or both of the out-of-range lines is not toggling, the out-of-range comparator on the Error Amplifier board, or the sensing circuit on the Phase Lock Control board, has probably failed. This could cause problems in maintaining lock but not in acquiring lock. If the instrument does not acquire lock, note the out-of-range problem and continue troubleshooting with step 3).

(2) If there is no signal at TP2037, the Error Amplifier has probably failed. (E)

(3) If there is a signal at TP2037, the switching circuit that connects the output of the Error Amplifier to the FM coil of the 1st LO has probably failed. (E)

b. If beat notes are present, but their amplitude is less than 3.8 V (peak-peak), or the amplitude difference of the positive and negative excursions is more than 20%, the Phase Gate is probably defective. (E)

c. If there are no beat notes, measure the strobe frequency, at P504 on the Phase Lock module.

(1) If the strobe frequency is the same as the readout on the diagnostic aid display, it is possible, but not probable, that the 1st LO system is miscalibrated and that the 1st LO is near the wrong harmonic of the Auxiliary Synthesizer. Press <SHIFT> to return to normal operation and look at the calibrator line that is closest in frequency to the frequency (in Band 1) at which the error occurs. If the frequency indicated for the calibrator line is correct (a multiple of 100 MHz), the Phase Gate has probably failed.

If the frequency indicated is incorrect, attempt to calibrate the 1st LO system by pressing <SHIFT> 0 and selecting #1 (FREQUENCY LOOPS CAL), and then #0 (OVERALL SYSTEM) from the menu. Exit from the calibration routine when the display for R4040, on the CF Control board appears by pressing <SHIFT>. If the calibration can not be completed, or it does not result in the correct frequency indication for the calibrator line, troubleshoot the 1st LO system using the procedure under TUNING FAILURE —1st LO error message step 3b. (E)

(2) If there is no strobe signal, check for a signal on feedthrough M, on the Strobe Driver board in the Phase Lock module.

(a) If there is a signal, the Strobe Driver has probably failed. (E)

(b) If there is no signal, the Controlled Oscillator has probably failed. (E)

(3) If the frequency of the strobe signal is erroneous, but is stable (within 1—2 Hz), in the normal strobe range of 5.006477 MHz to 5.018868 MHz, the programmable divider in the Synthesizer has probably failed. (E)

(4) If the listed Strobe Freq is below 5.007100 MHz and the actual strobe frequency is slightly above the desired frequency; or above 5.018240 MHz and the actual strobe frequency is slightly below the desired frequency, attempt to calibrate the Phase Lock Synthesizer. Press <SHIFT> 0 and select #1, then #5. If you are able to complete the calibration, check to see if the error message is still present. If it is still displayed, or the calibration routine could not be completed, proceed to the next step as if the strobe frequency was not within the above range. (E)

(5) If the listed Strobe Freq is outside the range in the preceding step, measure the tune voltage for the VCO, at feedthrough H on the Controlled Oscillator board in the Phase Lock module. The normal range is from 5.9 V to 11.3 V. With the loop unlocked, the voltage will probably be near or beyond one end of the range.

(a) If the voltage is around the center of the range, the loop filter and amplifier, on the Error Amplifier board, are probably at fault. (E)

(b) If the tuning voltage and the strobe frequency are displaced from the center of their range (8.6 V and 5.013 MHz) in the same direction, the VCO is good and something else within the loop has failed. (E)

(c) If the tuning voltage and the strobe frequency are displaced in opposite directions from the center of their range, the VCO has probably failed. (E)

TRACE MODES

Trace Mode provides information on how the frequency control system is working. It is accessed by pressing <SHIFT> 0, menu item #7, then selecting 1st LO (menu item #1), 2nd LO (menu item #2), MARKER (menu item #3), or DISPLAY RESULTS (menu item #4).

Trace Mode 1, starts tracing the 1st LO control actions. Trace Mode #2, starts tracing the 2nd LO control actions. Trace Mode #3, starts tracing signal counts. Trace Mode #4 starts tracing marker correction cycles.

Information from these four trace modes is stored in RAM and can be displayed by selecting DISPLAY RESULTS (menu item 5) from the TRACE MODE menu. This mode displays up to 16 lines of data gathered by the trace modes.

For modes #1 and #2, the first field of the display indicates which mode was active at the time the information was gathered. The second field of the display indicates which attempt at tuning or correcting the oscillator the data is for. The next field contains the tuning DAC settings before a tune or correction took place. The first three digits are the upper DAC settings, the next three digits the lower DAC settings. The next field contains the DAC settings after the tuning or correction was attempted. Again, the first three digits are the upper DAC, and the next three digits the lower DAC settings. The next field indicates the time delay between setting the DACs to the new values and reading the resulting frequency, in units of millisecond. The final field contains the frequency of the oscillator in question, after the tune or correction attempt. Actually, the displayed frequency is the beat note frequency from the auxiliary mixer for the 1st LO (in KHz), and the 16—20 MHz oscillator frequency for the 2nd LO.

For mode 4, the resulting trace display consists of seven columns. The first column is always 4, indicating that the marker is being traced. The second column gives the iteration number of the correction cycle which the displayed line describes. The third column consists of two letters and a number. The first letter is P if the data applies to the primary marker and S if the data applies to the secondary marker. The second letter is C if the oscillators are being counted at the marker position to determine the marker frequency, or S if the marker position is being synthesized to maintain a constant marker frequency. The number in this column is 1 if the 1st LO is being counted at the marker and 2 if the second LO is being counted. The fourth column is the hexadecimal setting of the marker DAC. The fifth column is the decimal digital storage location of the marker. The sixth column is the oscillator settling time in ms before the count. The last column is the harmonic mixer output frequency in KHz for a 1st LO count, or the 16—20 MHz VCO frequency for a 2nd LO count at the marker position.

The sequence <SHIFT> 0, #7, #0, terminates trace actions and erases the RAM of all data.

Alternate Frequency Display

The Alternate Frequency Display mode selects an alternate frequency display instead of the normal Center Frequency display. These alternate frequencies are selected by pressing <SHIFT> 0, selecting menu item #0, and selecting #0, #1, or #2 as indicated by the menu.

The normal Center Frequency is displayed when #0 is selected.

The frequency of the 1st LO is displayed when #1 is selected. This display is updated each time the 1st LO frequency is counted.

The frequency of the 2nd LO is displayed when #2 is selected. This display is updated each time the frequency of the 2nd LO is counted.

Auxiliary Synthesizer Control

The Auxiliary Synthesizer Control can be turned on continuously, or turned on only during correction for the 1st LO tunes. This mode is toggled (turned on continuously or during 1st LO corrections) by pressing <SHIFT> 0, and selecting menu item #4. A message will come on screen indicating which mode the Auxiliary Synthesizer is in.

Correction Disable/Enable

Correction of the 1st and 2nd LO frequencies can be disabled or enabled by pressing <SHIFT> 7 or <SHIFT> 0, and selecting menu item #6. When corrections are disabled, the oscillator frequencies are counted but no further action is taken. This mode can be used to monitor the drift of the oscillators by activating the respective trace mode. When corrections are disabled, the 1st LO cannot be phase locked!

CORRECTIVE MAINTENANCE

Corrective maintenance consists of component replacement and instrument repair. Special techniques and procedures that may be required to remove and replace assemblies and/or components in this instrument are described here.

Handling Static Sensitive Components

Most semiconductor types, both separately and in assemblies, are susceptible to damage to static charge, see Table 6-1 for voltage levels. We recommend static sensitive procedures be implemented for all operations involving semiconductor handling.

Obtaining Replacement Parts

All electrical and mechanical parts are available through your local Tektronix Field Office or representative. The Replaceable Parts list section contains information on how to order these replacement parts.

NOTE

Some components that are heat sinked to the circuit board extrusion or module wall, are soldered to the board after the board is mounted in place. This is necessary to avoid cracking the case when the mounting screw is tightened. These components are identified by a note on the schematic drawing. Their part number appears with chassis mounted components in the Replaceable Electrical Parts list.

Parts orientation and lead dress should be duplicated because some components are oriented to reduce interaction between circuits or control circuit characteristics.

Where applicable, an improved part will be substituted when a replacement is ordered. If the change is complex, your local Field Office or representative will contact you concerning the change. After repair, the circuits may need recalibration.

Parts Repair and Return Program

Assemblies containing hybrid circuits or substrates in a semi-sealed module, and complex assemblies such as the 1st LO can be returned to Tektronix for repair under the repair and return program.

Tektronix repair centers provide replacement or repair service on major assemblies as well as the unit. Return the instrument or assembly to your local Field Office for this service, or contact your local Field Office for repair and exchange rates.

Firmware Version and Error Message Readout

This feature provides readout of the firmware version when the power on/off is cycled. During the initial power-up cycle, the instrument firmware and front panel firmware versions are displayed on the crt for approximately two seconds. The Replaceable Electrical Parts list section, under Memory board (A54) and GPIB board (A56), list the ROM devices and their Tektronix part numbers for each firmware version.

Whenever an error occurs in an operational routine, an error message on screen describes the nature of the error. Status messages or prompts (see Diagnositics part of this section), are also displayed when running a diagnostic test or calibration procedure.

Selected Components

A few components that are selected to meet certain parameters such as temperature compensation, or to center the range of some adjustable component. The selected components are identified as selectable on the circuit diagram and in the Replaceable Electrical Parts list. The Replaceable Parts list description for the component gives either a nominal value. The procedure for selection is explained in the adjustment part of recalibration procedure. Table 6-5 lists these components, their nominal values, and the criteria for selection.

Replacing EPROM or ROM Devices

Firmware for the microcomputer is contained in ROM packs on the Memory and GPIB boards. Refer to the Replaceable Electrical Parts list (Vol. 2) under these assemblies (A54 Memory and A56 GPIB) for the versions and integrated circuit part numbers. All integrated circuits are soldered into sockets on the board to reduce problems that occur due to poor contact because of corrosion or loose pins. Refer to replacing Transistor and Integrated Circuit for procedure.

Table 6-5
SELECTED COMPONENTS

Component Number	Nominal Value	Selection Criteria
A22A1R1070	6.04kΩ	Sets Reference Mixer output at 18 MHz
A22A1R2049	6.04kΩ	Adjusts linearity of the 2nd LO sweep
A22A1R2070	6.04kΩ	Adjusts 2nd LO tune range
A22A1R2072	3.83kΩ	Sets 2nd LO sweep
A46A1R1011 A46A1R1012	10KΩ	Matched for temperature coefficient to 5PPM/°C
A46A1R1013 A46A1R1014	10KΩ	Matched for temperature coefficient to 5PPM/°C
A46A1R1015 A46A1R1016 A46A1R1020	10.5kΩ 5kΩ 10kΩ	Matched for temperature coefficient to 5PPM/°C
A46A1R1048 A46A1R1049	10KΩ	Matched for temperature coefficient to 5PPM/°C
A46A1R1050 A46A1R1051	10KΩ	Matched for temperature coefficient to 5PPM/°C
A46A1R1052 A46A1R1053 A46A1R1055	5kΩ 10.5kΩ 10kΩ	Matched for temperature coefficient to 5PPM/°C
A50A5C1038	47 pF	Move C1041 frequency adjustment range
A50A5C1048	47 pF	Move C1042 frequency adjustment range
A50A2C1016 A50A2C1018 A50A2C1032 A50A2C1024	3.3 pF—27 pF	FL1024 input/output impedance match

Surface-Mounted Components

Surface-mounted components have been used in this instrument. These components are mounted on pads on the circuit board, rather than through holes in the board. (In some rare instances, components may be mounted on pads around through holes.) Lead configuration of these components is shown in Figure 6-1.

The positive end of electrolytic capacitors is identified with a band. Other capacitors and resistors have no visible identification. However, like their axial-leaded counterparts, their values can be measured with a meter.

Surface-mounted semiconductor devices are sensitive to static electricity discharges, and should be treated as outlined in the beginning of this section.

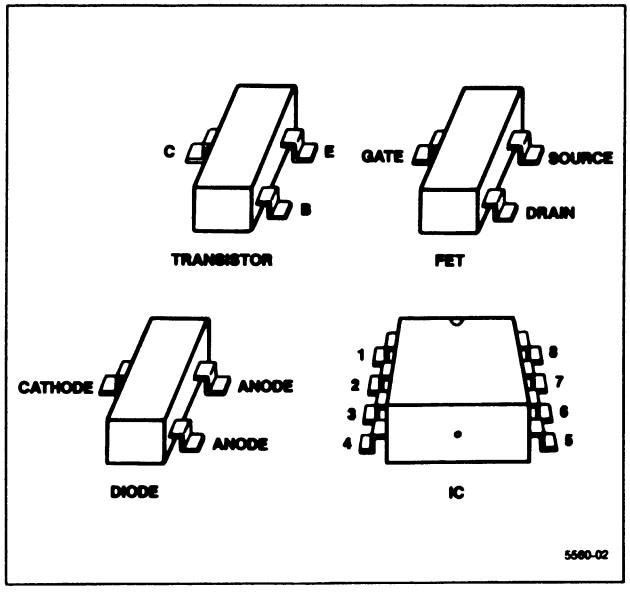


Figure 6-1. Surface-mounted components lead configuration.

Table 6-6
SERVICING TOOLS FOR BOARDS WITH SURFACE MOUNTED COMPONENTS

Description	Model Type	Tektronix Part No.
Hot Air Repair Terminal	Nu-Concepts Systems HART200A	N/A
Tempilaq	Nu-Concepts Systems	N/A
Tempilaq Thinner	Nu-Concepts Systems TLTH	N/A
Flux Dispenser	Nu-Concepts Systems FD2	N/A
Soldering Iron	Hexacon Model SMD10	003-1401-00
Soldering Iron SMD Tips		
Semi-Chisel, 1/16"	Hexacon Model Z780X	003-1402-00
Conical, 1/32"	Hexacon Model Z783X	003-1403-00
Sharp Conical"	Hexacon Model Z784X	003-1404-00
Bevel, 1/32"	Hexacon Model Z786X	003-1405-00
Chisel, 1/16"	Hexacon Model Z787X	003-1406-00
Bevel, 1/16"	Hexacon Model Z788X	003-1407-00
0.062" Slot"	Hexacon Model S303	003-1408-00
0.195" Slot	Hexacon Model S308	003-1409-00
0.195" Slot	Hexacon Model S314	003-1410-00
0.195" Slot	Hexacon Model S316	003-1411-00
0.195" Slot	Hexacon Modified S302	003-1412-00
Stainless Steel, Non-Magnetic Tweezers		
Straight Tip		Tektronix Part No. 003-0464-00
Curved Tip		Tektronix Part No. 003-0465-00
Silver Solder		Tektronix Part No.251-0514-00

Replacing Surface-Mounted Components

A Hot Air Machine, such as Hart Model 200A manufactured by Nu-Concept Computer Systems Incorporated of Colmar, Pennsylvania, is recommended for unsoldering and soldering surface-mounted components.

Table 6-6 lists tools that are suitable for servicing circuit boards with surface-mounted components.

Do not apply too much heat, as the pad/s on which the device is soldered may be lifted from the circuit board.

1. Unsolder the component.

2. Clean the board with isopropyl alcohol.

3. Solder in the replacement. Surface-mounted components are pretinned, and should be soldered onto the board with solderpaste rather than solder.

CAUTION

If you use a soldering iron, use one with a small tip. After applying the solderpaste, touch the corner of the pad with the iron to fasten the component. Avoid touching the component with the hot soldering iron. Thermal shock causes hairline cracks that are not visible to the eye.

Transistor and Integrated Circuit Configurations

Lead identification for transistors and integrated circuits, is readily available from manufacture's data books. Integrated circuit pin-outs for Vcc and ground are shown with a box on the schematic diagram. Refer to Soldering Technique in Corrective Maintenance part for unsoldering and soldering instructions.

Diode Color Code

The cathode of each glass encased diode is indicated by a stripe, a series of stripes, or a dot. Some diodes have a diode symbol printed on one side. Figure 6-2 illustrates diode types and polarity markings that are used in this instrument.

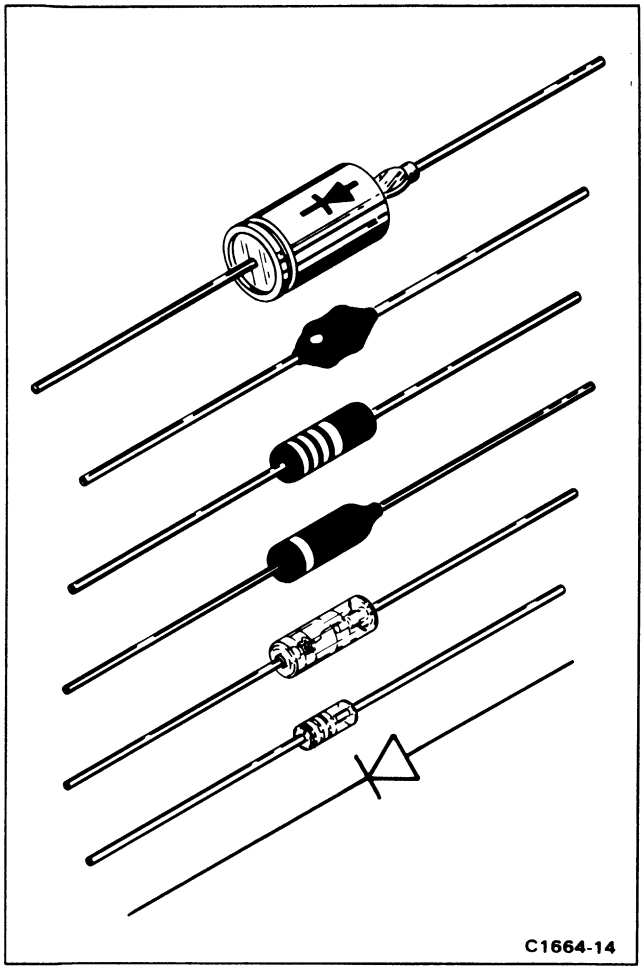


Figure 6-2. Diode polarity markings.

Multiple Terminal (Harmonica) Connectors

Some intercircuit connections are made through pin connectors that are mounted in a harmonica type holder. The terminals in the holder, are identified by numbers that appear on the holder and the circuit diagrams. Connectors are identified on the schematic and board with either the prefix letter P or J followed by a circuit number. Connector orientation to the circuit board is keyed by a triangle on the holder and the circuit board (see Figure 6-3). In some cases, the triangle or arrow is screened on the chassis adjacent to the connector. Some connectors contain more than one section.

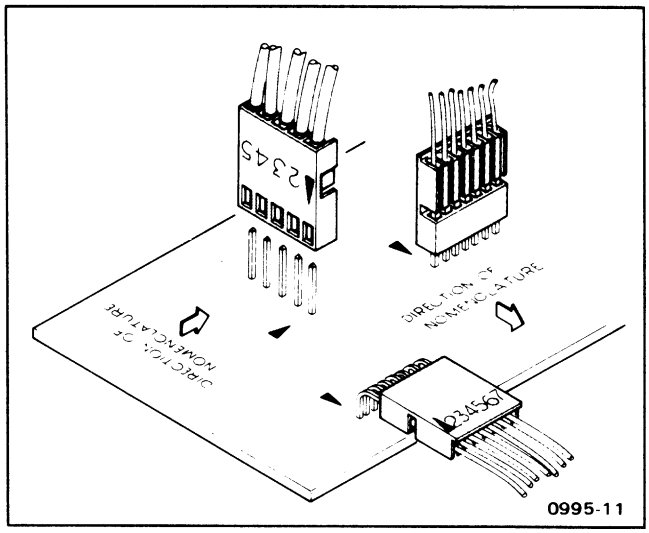


Figure 6-3. Multipin (harmonica) connectors.

Resistor Values

Many types of resistors (such as composition, metal film, taped, thick film resistor network package, plate, etc.) are used. The value is either color coded in accordance with the EIA color code, or printed on the body of the component.

Capacitor Marking

The capacitance value of ceramic disc, plate, and slug, or small electrolytic capacitors, is marked in microfarads on the side of the component body. The ceramic tubular capacitors and feed-through capacitors are color coded in picofarads.

Soldering Techniques

CAUTION

Disconnect the instrument from its power source before replacing or soldering components.

Some of the circuit boards in this instrument are multilayer; therefore, extreme caution must be used when a soldered component is removed or replaced. Excess heat from the soldering iron and bent component leads may pull the plating out of the hole. We suggest clipping the old component free.

To remove the component leads, use a 15 W or less pencil type iron. Straighten the leads on the back side of the board; then when the solder melts, gently pull the soldered lead through the hole. A desoldering tool should be used to remove the old solder. Use a desoldering tool that has a low build-up of static charge, such as Silverstat Soldapullt desoldering tool, when unsoldering integrated circuits or transistors.

Replacing the Square Pin for the Multi-pin Connectors

It is important not to damage or disturb the ferrule when removing the old stub of a broken pin. The ferrule is pressed into the circuit board and provides a base for soldering the pin connector.

If the broken stub is long enough, grasp it with a pair of needle nose pliers, apply heat, with a small soldering iron, to the pin base of the ferrule and pull the old pin out. (The pin is pressed into the ferrule so a firm pull is required to pull it out.)

If the broken stub is too short to grasp with pliers, use a small dowel (0.028 inch in diameter) clamped in a vise to push the pin out of the ferrule after the solder has melted.

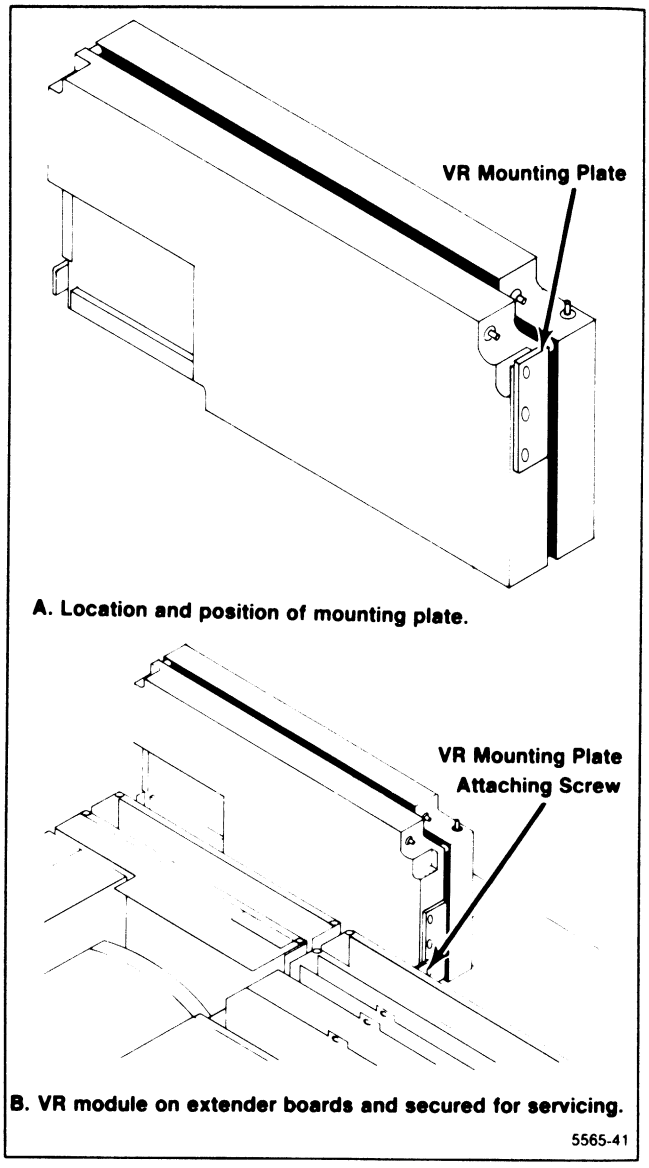
The old ferrule can be cleaned by reheating socket and placing a sharp object such as a toothpick or small dowel into the hole. A 0.031 inch drill mounted in a pin vise may also be used to ream the solder out of the old ferrule.

Use a pair of diagonal cutters to remove the ferrule from the new pin; then insert the pin into the old ferrule and solder the pin to both sides of the ferrule.

If it is necessary to bend the new pin, grasp the base of the pin with needle-nose pliers and bend against the pressure of the pliers to avoid breaking the board around the ferrule.

Servicing the VR Module

The VR module requires mechanical support when it is installed on board extenders. Mechanical support is provided by moving the mounting plate at the upper side of the module (Figure 6-4A) to the bottom side. This allows installation of a mounting screw through a support bracket into the mounting plate screw hole as shown in Figure 6-4B. For better support, we recommend using a second bracket on the other end. Remove the bracket, turn it over and install it so the threaded studs are below the module.



A. Location and position of mounting plate.

B. VR module on extender boards and secured for servicing.

Figure 6-4. Servicing the VR assembly.

REPLACING ASSEMBLIES AND SUBASSEMBLIES

Most assemblies or sub-assemblies in this instrument are easily removed and replaced. The following describes procedures for replacing those assemblies that require special attention. Top and bottom views are shown in Figures 6-5 and 6-6, respectively. These illustrations show the location and identify most assemblies by their name and assembly number.

Some circuit boards and assemblies must be placed on extenders to access test points or adjustments. Before removing these boards and assemblies, the air baffle attached to the left siderail must also be removed.

Turn the power off before removing an assembly.

Instructions for removing the cabinet can be found under Preparation in Section 5, Adjustment Procedure.

Removing or Replacing Semi-rigid Coaxial Cables

Performance of the instrument is easily degraded if these connectors are loose, dirty, or damaged. The following procedure will help ensure that the connection is good enough to maintain proper performance.

1. Use a 5/16 inch open-end wrench to loosen or tighten the connectors. It is good practice to use a second wrench to hold the rigid (receptacle) portion of the connector to prevent bending or twisting the cable.

2. Ensure that the plug and receptacle are clean and free of any foreign matter.

3. Insert the plug connector fully into the receptacle before screwing the nut on. Tighten the connection to 8 in-lbs to ensure that the connection is tight. Do not overtighten (15 to 20 in-lbs) because this can damage the connector.

Replacing the Dual Diode Assembly in the 1st Mixer

The diode subassembly that houses the Schottky mixer diodes permits easy field replacement of the diodes. The subassembly is secured in place with four 0-80 screws. An 8-32 threaded hole is provided to facilitate insertion and removal of the subassembly. There are three contact points located on the substrate side of the subassembly. Use care to ensure proper fit when mounting and orienting these contacts in the mixer assembly. Insertion and removal of the subassembly more than twice is not recommended due to the gold-ribbon attaching technique used in fabrication.

A tuning screw is adjusted to null a start spur on Band 1. This tuning screw is mounted through the top of the diode asssembly, adjacent to the 8-32 hole. If adjustment of this screw is warranted, care should be taken to not force the tuning screw after it bottoms out on the surface of the quartz-suspended substrate.

The diode assembly is packaged in a static-free package. Keep the diode subassembly in this package until ready to install. The following should be used when replacing this assembly.

CAUTION

The diodes are beam-lead devices, mounted on a quartz-suspended substrate. These diodes are extremely sensitive to static electricity discharge. Refer to the caution note on static discharge at the beginning of this section. Do not expose the diode assembly to RF fields.

1. Loosen and disconnect the three coaxial cable connections at the 1st Converter assembly.

2. Remove the two mounting screws, and remove the assembly from the instrument.

3. Remove the four 0-80 screws that hold the diode subassembly in the 1st Converter, and insert a 8-32 screws into the threaded hole provided in the center of the diode assembly.

4. Lift the diode assembly out of the mixer assembly by means of the 8-32 screw, then remove the screw.

5. Open the diode package. Use a pair of tweezers to grasp the diode assembly by its side, and place it on a static-free surface. Grasp the side of the assembly with the fingers. Avoid contact with the diodes. Insert the 8-32 screw.

6. Orient the diode assembly so the three contact tips are aligned with their respective contacts in the mixer; then, using the index fingers of both hands so equal pressure is applied, press the subassembly into place.

7. Insert the four mounting screws, then replace and tighten the three coaxial connectors to 8 in-lbs. Remount the 1st Converter assembly by installing the two mounting screws that hold the assembly to the RF deck.

8. The Spectrum Analyzer may not meet the flatness specification after the Dual Diode assembly is replaced. Refer to MAINTENANCE ADJUSTMENTS in this section for a procedure for adjusting converter bias and flatness.

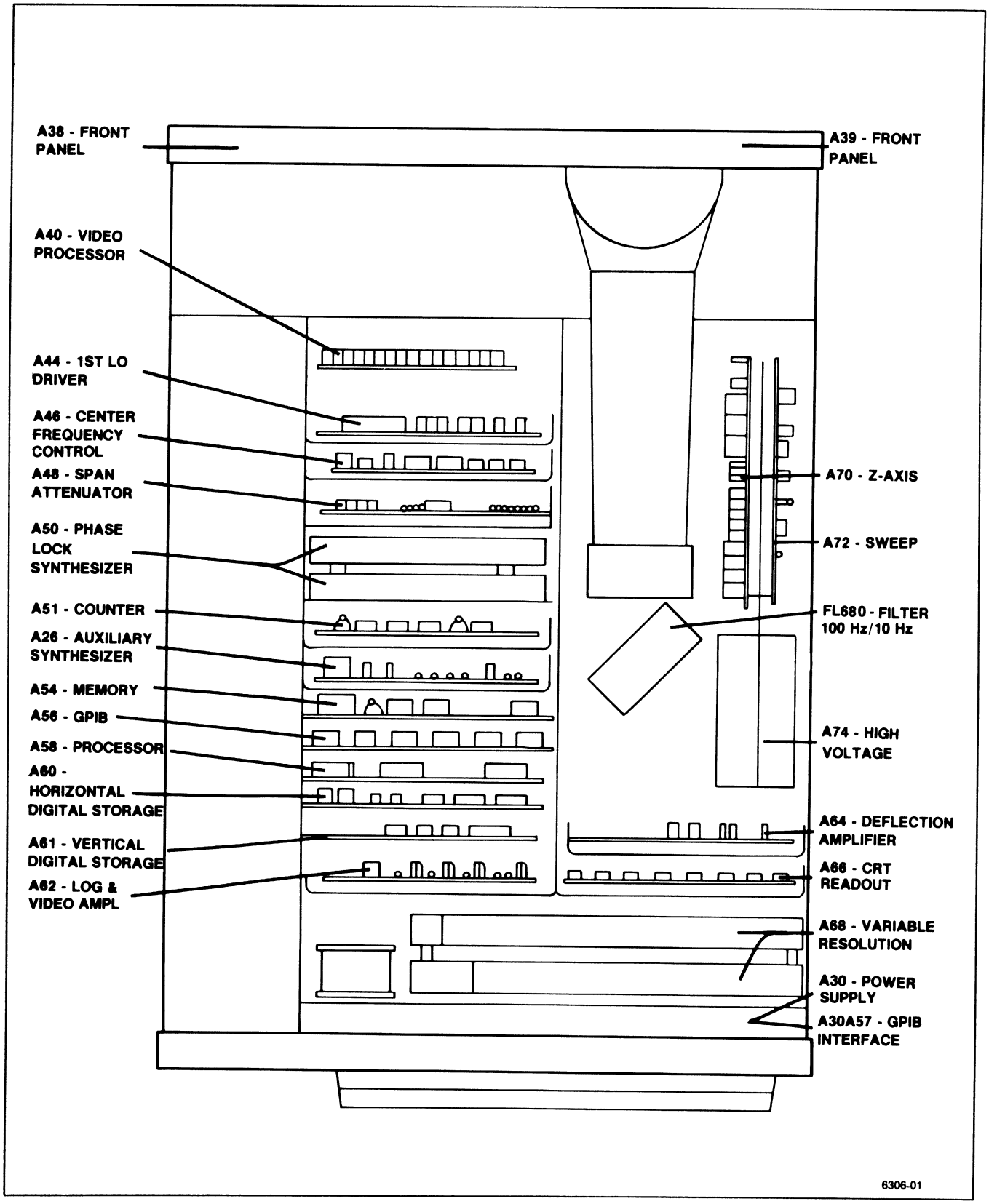


Figure 6-5. Top deck assemblies.

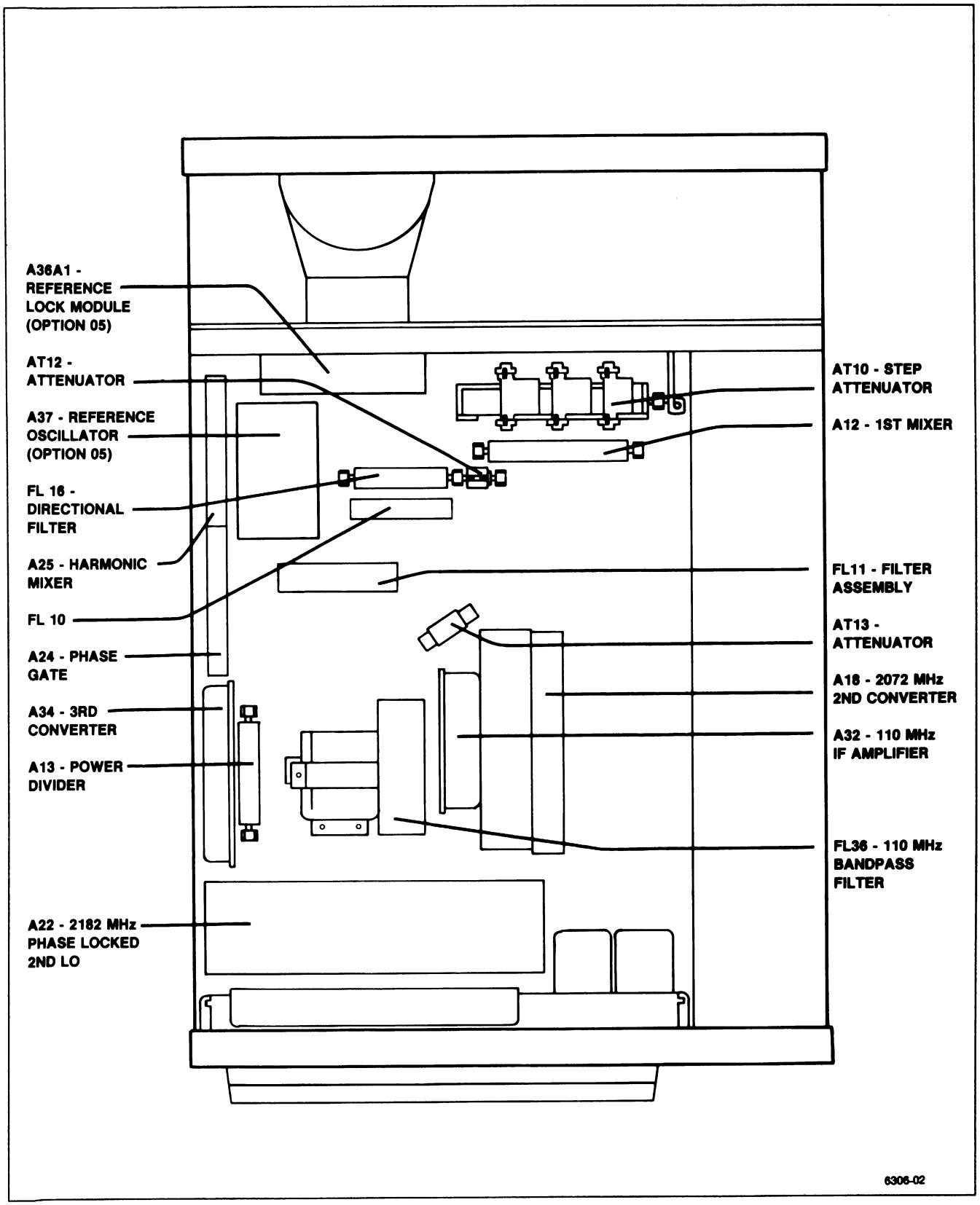


Figure 6-6. RF deck assemblies.

Replacing the Crt

1. Remove the snap-in printed bezel and crt light filter.

2. Use an 8/64 inch Allen wrench to remove the four bezel screws, unplug and remove the inner bezel.

3. Unsolder the ground wire from the front panel casting and unplug the crt cables at their respective board connections (High Voltage module, Deflection Amplifier board, and Z-Axis board).

4. Slide the crt, with its shield, out through the front panel.

5. Remove the crt shield as follows:

a. Remove the tube base cap and unplug the socket.

b. Remove the two side screws that hold the upper shield in place, then remove the shield.

c. Loosen the screws that clamp the plastic bracket around the crt, then remove the bracket.

6. Install the plastic bracket so the back on the clamp is 5.07 inches from the back of the crt socket guide.

7. Replace the crt shield plus the socket and base shield by reversing the removal procedure. The finished crt assembly length, with cap installed, must equal 11.05 inches. If it is longer, the assembly may short circuit the Deflection Amplifier circuit board when it is installed.

8. Place the spectrum analyzer on its rear panel then loosen the four crt blue plastic mounting blocks on the front casting so they can be readily positioned when the crt is installed.

9. Install the crt with shield assembly through the front panel; seat the wedges on the side of the crt, into the blue plastic mounting blocks.

10. Position the cast bezel and implosion shield in place to ensure that there is clearance between the crt face and the bezel. (The bezel must bottom on the front casting.)

CAUTION

It is very important that the four mounting blocks are loose enough so the bezel retaining screws can be tightened without the bezel touching the crt face. If not the crt or the bezel may crack when the screws are tightened.

11. Remove the bezel and tighten the mounting block screws evenly in a cross pattern to approximately 8 in-lbs. Make sure the crt stays centered in the blue plastic mounting blocks as the screws are tightened.

12. Replace the bezel and implosion shield, reconnect cables to their respective board connectors, and resolder the ground lead to its terminal.

13. Replace crt light filter and snap-in printed bezel.

Repairing the Crt Trace Rotation Coil

The trace rotation coil is part of the crt assembly. If the coil is damaged beyond repair, the crt with the coil must be replaced.

If the "finish" (red) lead is broken, remove the tape and unwind one or two turns so it can be respliced and soldered to the lead wire. Rewind and retape.

If the "start" (black) lead is broken and the lead is too short to re-splice, attempt to fish out the broken end so one or two turns can be unwound, re-splice and solder to the lead; then rewind and retape.

Front Panel Assembly Removal

It is not necessary to remove the front panel assembly to replace any of the push buttons. (Refer to Replacing Front Panel Pushbuttons, following this procedure.) The crt is removed with the front-panel assembly.

1. Place the front of the instrument just off the edge of a table, then unscrew and remove the mounting nuts and washers from the RF INPUT, and the two 1st and 2nd LO OUTPUT connectors. Remove the knobs.

2. Unplug the CAL OUT coaxial cable from the 3rd Converter, and unplug the crt from the Z-Axis/RF Interface, High Voltage module, and the Deflection Amplifier.

3. Unplug the front-panel board from the Mother board, and remove the cables connecting the two front-panel boards.

4. Pull off the snap-in crt bezel, and loosen the allen screws holding the crt. Remove the front-panel overlay. Remove the eight screws holding the front- panel assembly to the frame.

Replace the front-panel assembly by reversing the removal procedure.

Front-Panel Board Removal

NOTE

A replacement Front Panel board comes with switches and controls for different versions of the spectrum analyzer. Before replacing an existing board, remove the switches and controls on the new board that are not used on the particular version of the instrument.

It is not necessary to remove the front-panel assembly to remove the front-panel board.

1. Remove the front-panel knobs. Remove the cables connecting the two front- panel boards, and the cable connecting the front panel to the Mother board.

2. To remove front panel #1, remove the 8 screws holding it to the subpanel. To prevent losing the grounding rings or bushings between the front-panel controls, gently pull the board from the subpanel.

3. To remove front-panel #2, remove 3 screws holding it to the subpanel.

Replacing Front Panel Pushbutton Switches

1. Remove the front panel board, using the previous procedure.

2. Pull off the switch keycap, and push the switch through the board from the back.

3. When installing a new switch, support the led from the back when appropriate.

Main Power Supply Module Removal

CAUTION

To avoid damage to the Mother board connector J5041 and Interface connector J1034, during removal or installation of the Power Supply module, use the following procedure.

1. Disconnect the power cord, set the spectrum analyzer on its face or front panel and remove the instrument cover. 2. On the circuit board side of the instrument, unplug the coaxial cable connector P620 from the Log and Video Amplifier assembly. On the RF deck side disconnect the plug for the cable to the Reference Lock assembly, at the lower right corner of the Power Supply module.

3. Remove the cable clamp for the GPIB interconnect cable and unplug P560 to the GPIB Interface board.

4. Remove the three screws that hold the power module to the RF deck flange (bottom right side), then remove the four screws that hold the power supply module to the side rails.

5. With the instrument RF deck on the near side, pull the left side of the power module from its side-rail (no more than 1.5 inch). Now grasp both sides of the module and lift to separate the module from the Mother board.

WARNING

Because C6111 and C6101 discharge very slowly, hazardous potentials exist within the power supply for several minutes after the power switch is turned off. A relaxation oscillator, formed by C5113, R5111, and DS5112, indicate the presence of voltages in the circuit until the potential across the filter capacitors is below 80 V.

6. Loosen and remove the two screws that hold the mounting bracket for P361. Lift the cover off the module and unplug P3045 to the Fan Drive board. The power supply should now be accessible.

7. Reinstall P361 mounting bracket then plug P3045 onto the power supply board and replace the cover.

8. Set the instrument with the RF deck on the near side then hold the power supply module over the instrument so the right side is touching the side-rail and the left side is about 1.5 inch above its side-rail.

9. Align connectors P5041 and P1034 with their respective Mother board and Interface board connectors, then press the module into place between the side rails.

10. Replace the four module holding screws and the three flange screws.

11. Reconnect the coaxial cables and GPIB cable, if appropriate, then install the cable clamp.

12. Replace the instrument cover.

High Voltage Power Supply

A screw must be removed before the High Voltage Power Supply circuit board can be unplugged and removed. The screw goes through the side-rail into a nylon standoff bushing at the bottom corner of the board.

Removing and Replacing the 1st LO

1. Unplug and remove the multipin connectors to the assembly. Cut the tie-down that holds the black encased RF coil to the semi-rigid cable.

2. Using a 5/16 inch open-end wrench, loosen and disconnect the semi-rigid coaxial cable.

3. Loosen and remove the four mounting screws that hole the assembly to the RF deck. Remove the 1st LO assembly.

4. To replace the assembly, reverse the removal procedure. Use a tie-down to re-tie the RF coil to the semi-rigid cable to prevent vibration from breaking the coil leads.

Replacing the 1st LO Interface Board

The 1st LO assembly includes an interface circuit board that can be replaced. To replace the board refer to Figure 6-7 and the following procedure. Use a desoldering tool to remove the solder as the leads are unsoldered.

1. Unsolder and lift one end of C1014 (820 uF capacitor) at the top of the board.

2. Unsolder and lift one end of VR1010.

3. Unsolder and lift the + lead of C1016.

4. Unsolder the eight leads to the oscillator and lift the board off the assembly.

Fan Assembly Removal

1. Remove power supply as described in this section.

2. Remove six screws that hold the power supply cover in place. Take the coaxial cable out of the plastic retainer clip and lift the power supply cover with fan up, so harmonica connector P3045 can be disconnected and the cover removed.

3. Remove the nuts and lockwashers that hold the fan brackets from the back side of the power supply housing. The fan will fall free from the brackets.

4. The resilient mounts at the corners of the fan frame should be replaced if a new fan is to be installed or fan vibration is generating spurs on the display.

5. Insert four resilient mounts into the corners of the fan, flush with the fan frame.

6. Install one of the fan brackets to the power supply housing by attaching its lock washers and nuts to the back of the housing.

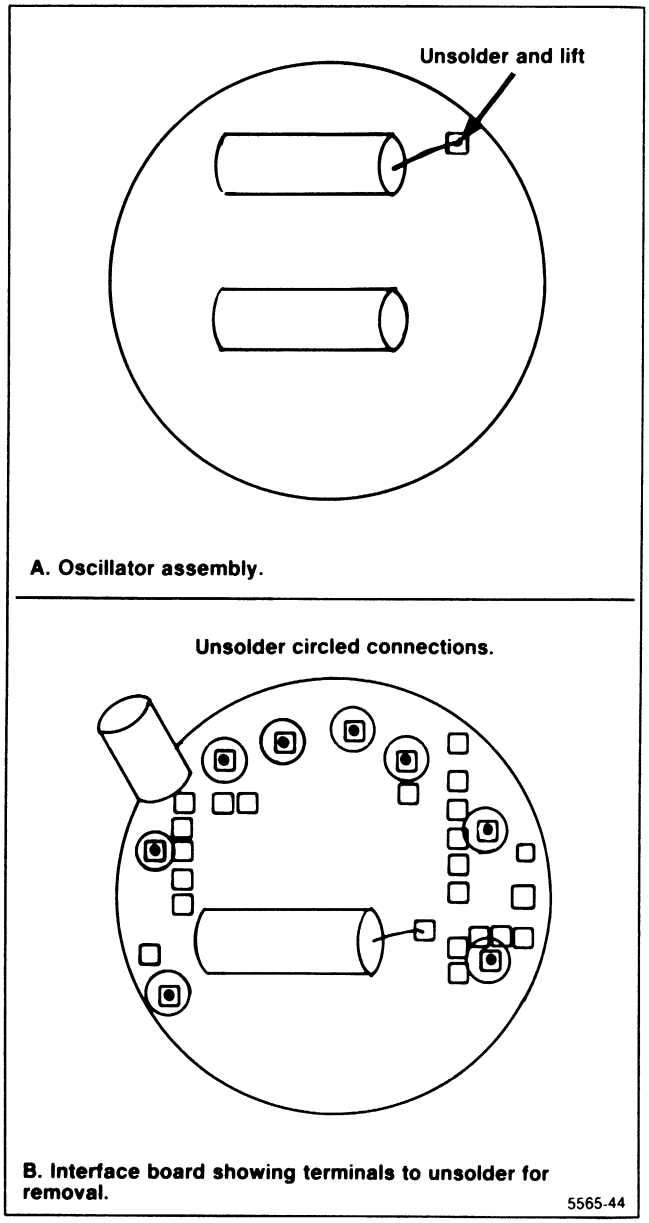


Figure 6-7. Removing the 1st LO Interface board.

NOTE

Fan brackets should be installed as in Figure 6-8.

7. Insert the posts of the brackets into the holes provided in the resilient mount and install the remaining bracket, with lockwashers and nuts, to the back side of the power supply housing.

8. Reconnect the fan to the Fan Drive board then replace the cover, with the fan, onto the power supply module.

9. After installing the six screws that hold the cover in place, ensure that the fan assembly moves freely. Replace the coaxial cable in the plastic retaining clip.

10. Reinstall the Power Supply assembly as directed under Power Supply Replacement. Apply power and check for normal fan operation.

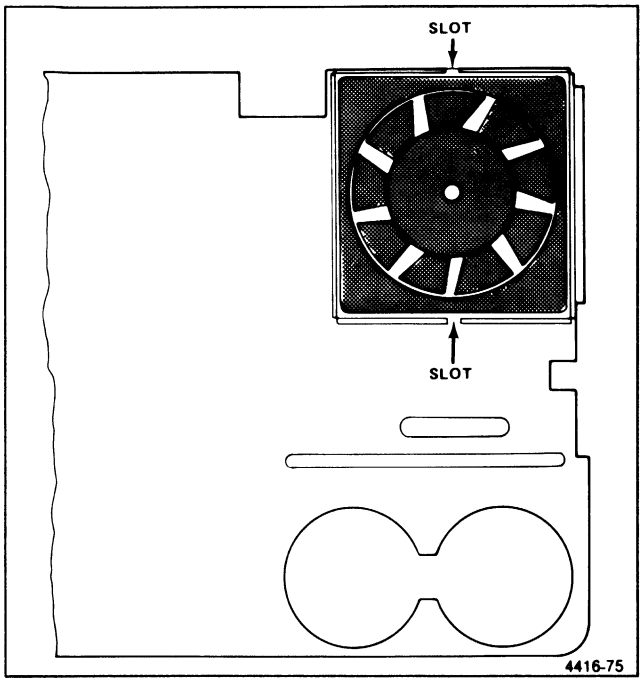


Figure 6-8. Fan assembly mounting.

MAINTENANCE ADJUSTMENTS

The following procedures are not part of the regular calibration. They are only performed when certain assemblies are replaced or after major repair.

0 Hz Response Adjustment

This adjustment is required only after replacement of the 1st Mixer assembly A12 or the Mixer Diode assembly A12A1.

a. Set the Spectrum Analyzer controls as follows:

FREQUENCY	0
FREQ SPAN/DIV	200 kHz
REFERENCE LEVEL	−20 dBm
RESOLUTION BANDWIDTH	100 kHz
VIEW A and VIEW B	On
VERTICAL DISPLAY	10 dB/DIV
MIN RF ATTEN	0 dB
MIN NOISE	On
TRIGGERING	FREE RUN
TIME/DIV	AUTO

b. Terminate the RF IN connector with a 50Ω terminator.

c. Reset the CENTER/MARKER FREQUENCY control to center the 0 Hz reponse.

d. An adjustment screw for the 0 Hz response is accessed by inserting a small screwdriver into the access hole on the Dual Diode assembly in the 1st Mixer. See Figure 6-9.

CAUTION

Use extreme caution when adjusting the tuning screw clockwise. Do not force the adjustment screw after it bottoms out to avoid cracking the diode substrate.

e. Adjust the tuning screw on the 1st Mixer assembly for minimum amplitude of the 0 Hz response.

f. Remove the protective cover from the adjustment for the Variable Load assembly.

g. Adjust the Variable Load adjustment for a peak amplitude of −30 dBm of the 0 Hz response.

h. Replace the protective cover over the adjustment for the Variable Load assembly.

Auxiliary Synthesizer VCO Adjustment

a. Monitor TP1066 on the Auxiliary Synthesizer board with a voltmeter. See Figure 6-10 for the location of TP1066.

b. Disable frequency corrections by pressing <SHIFT> 7.

c. Enable the Auxiliary Synthesizer by pressing <SHIFT> 0 and selecting menu item #4.

d. Adjust C1070 on the Auxiliary Synthesizer board for +5 V at TP1066.

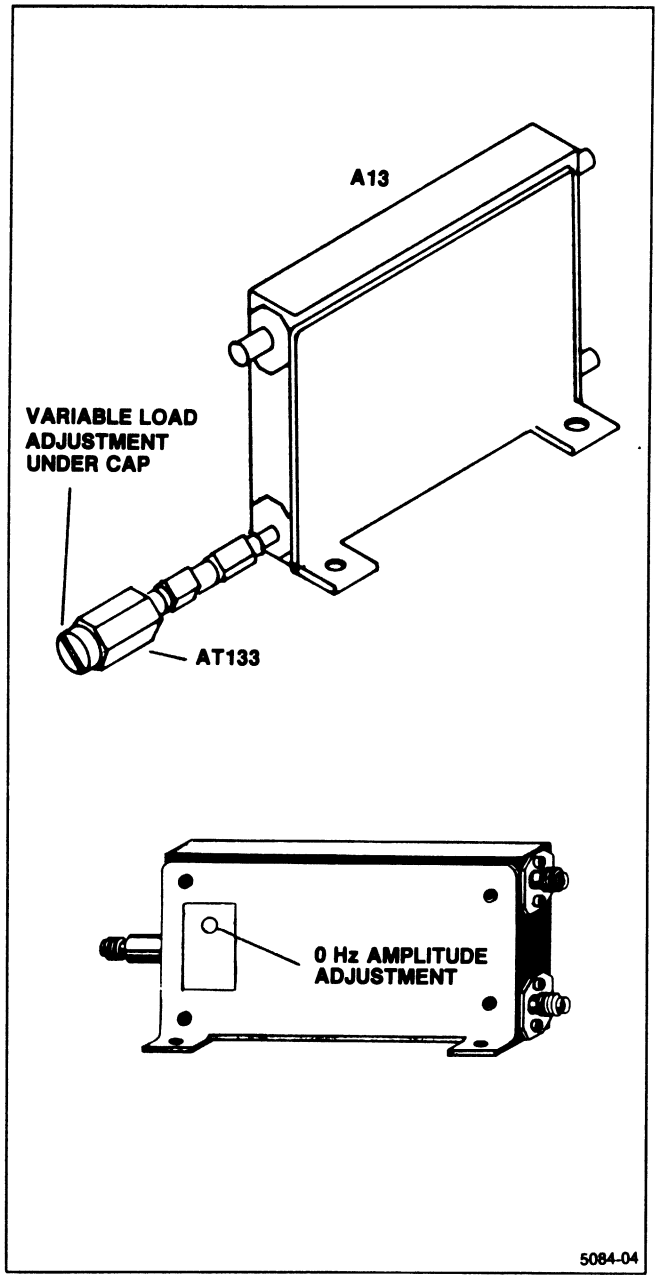


Figure 6-9. Adjustment locations for 0 Hz response.

110 MHz IF Assembly Return Loss Calibration — (Table 6-7 lists test equipment required to adjusts this assembly.)

1. Test equipment setup is shown in Figure 6-11. The IF assembly must be removed to gain access to the adjustments.

2. Apply 110 MHz at 2 V peak-to-peak (+10 dBm) through 35 dB of attenuation to the RF Input of the VSWR bridge. Connect the RF Out of the VSWR bridge to the RF Input of the spectrum analyzer. (Do not connect the 110 MHz IF to the VSWR bridge.)

3. Set the test spectrum analyzer Center Frequency to 110 MHz, Frequency Span/Div to 5 MHz, Resolution Bandwidth to 3 MHz, Vertical Display to 10 dB/Div, and Ref Level to −20 dBm.

4. Set the step attenuator for a full-screen display (−20 dBm).

5. Connect the 110 MHz IF input to the VSWR bridge and connect a 50Ω termination to the output of the IF amplifier. Now plug the power cable P3045 into the + and −15 V source and ground the case of the assembly.

6. Adjust C2047 and C1054 (Figure 6-12) simultaneously for minimum signal amplitude on the spectrum analyzer display. Minimum amplitude must be at least −55 dBm.

7. Disconnect test equipment setup and replace the 110 MHz IF assembly.

2072 MHz 2nd Converter

The 2nd Converter assembly consists of a four cavity 2072 MHz band-pass filter, mixer, and a 110 MHz low-pass filter. The assembly is precalibrated prior to installation, and requires no calibration after it is installed. We recommend replacing the assembly if it should malfunction. The following procedures describe adjustments that can be made if the biasing should malfunction or the seal on any of the filter tuning slugs is broken. The mixer diodes are not to be replaced in the field. Return the assembly to Tektronix, Inc., for repair.

CAUTION

Do not open the assembly. Adjust the tuning slug only after checking the filter characteristics.

Four Cavity Filter—The characteristics of the filter are checked with a network analyzer. Frequency of the filter is 2072 MHz, bandpass, 15 MHz down, is 1 dB, return loss is 20 dB or greater, and insertion loss is 1 dB. If the seal is broken on any tuning slug, adjust for maximum return loss.

Mixer—To gain access to the Bias adjustments, remove the assembly from its mounting; then remove the mounting plate on the bottom of the assembly. Reconnect the Mixer to the input/output lines, using the same cables (cable length of semi rigid cables is critical).

Apply the CAL OUT signal to the RF INPUT and tune a marker to center screen. Simultaneously adjust both bias potentiometers, R1021 and R1022, (see Figure 6-13) for maximum signal amplitude.

Table 6-7
EQUIPMENT REQUIRED FOR RETURN LOSS ADJUSTMENT

Test Equipment	Characteristics	Recommended Type
Spectrum Analyzer	Frequency range ⩾110 MHz	TEKTRONIX 49X-Series or 275X-Series or 7L14
Signal Generator	+10 dBm at 110 MHz	TEKTRONIX SG 503 for the TM 500-Series
VSWR Bridge		Wiltron 62BF50
10 dB & 1 dB Step Attenuators	50Ω, 0 dB to 40 dB	Hewlett Packard 355C & 355D
Termination	50Ω	Tektronix Part No. 011-0049-01
Adapter	Bnc-to-Sealectro	Tektronix Part No. 175-0419-00

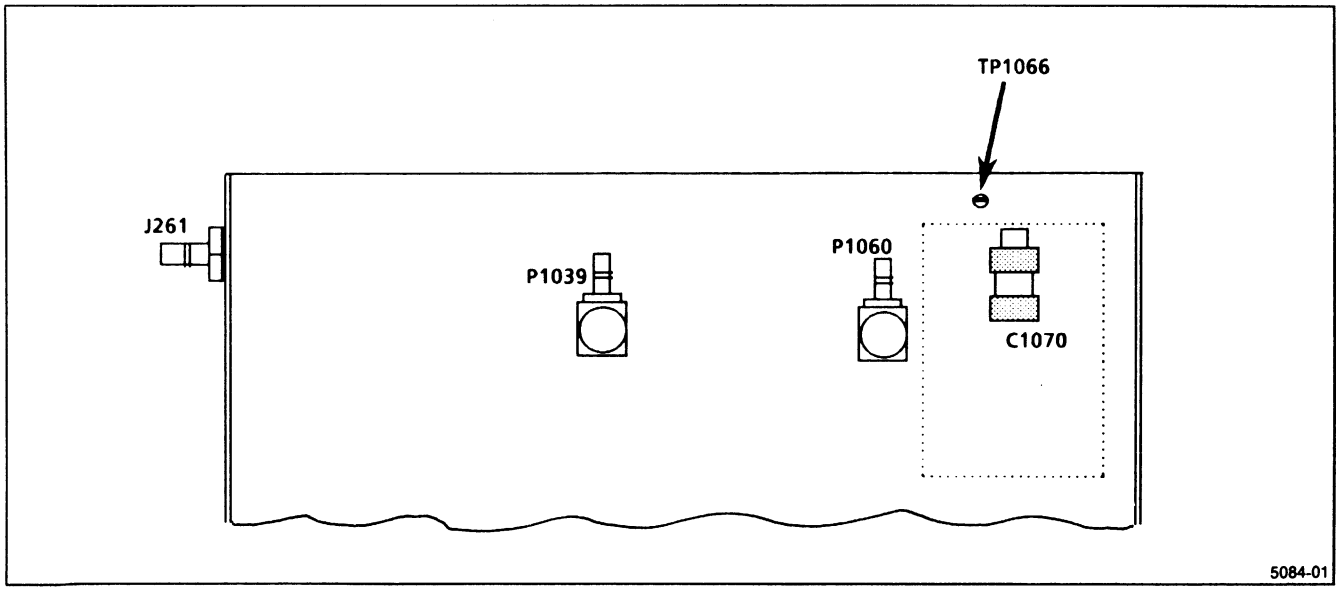


Figure 6-10. Auxiliary Synthesizer test point and adjustment locations.

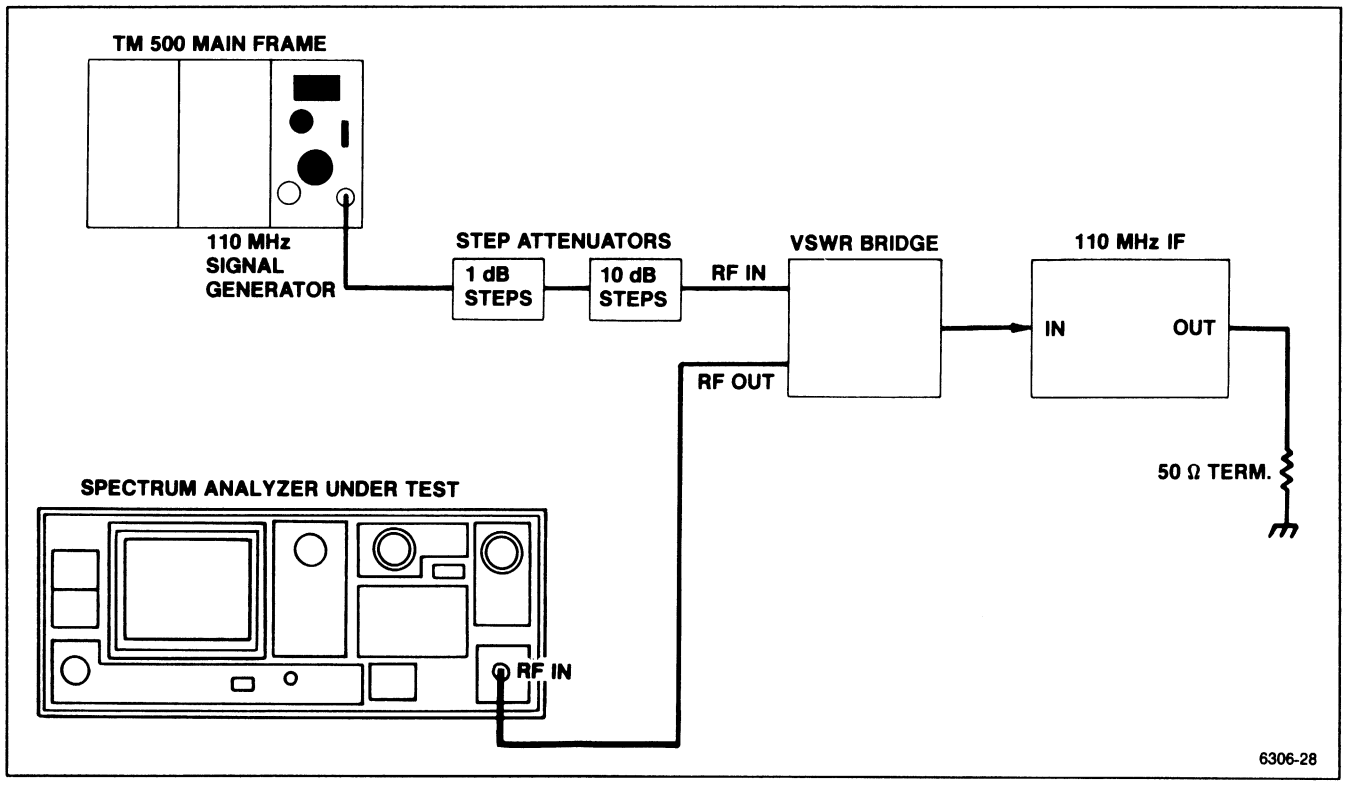


Figure 6-11. 110 MHz IF return loss adjustment setup.

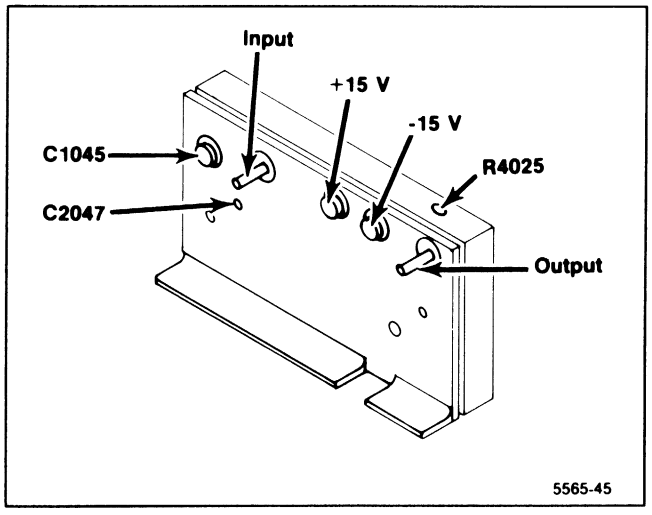


Figure 6-12. 110 MHz IF test points and adjustments.

110 MHz Three Cavity Filter

Alignment of this filter is not required unless the spectrum analyzer fails to meet bandwidth specifications. The filters are adjusted for center frequency and response shape so the resolution bandwidth is within specifications. The adjustment procedure is as follows:

1. With the CAL OUT signal applied to the RF INPUT, tune the signal to center screen and reduce the RESOLUTION BANDWIDTH to 1 kHz.

2. Tune the signal to center screen to establish center frequency reference; then increase the RESOLUTION BANDWIDTH to 1 MHz.

3. Adjust the tuning slugs for best response shape, centered around the reference. Ensure bandwidth (6 dB down) is 1 MHz.

4. Check resolution bandwidth accuracy over the range of the RESOLUTION BANDWIDTH control as per instructions in the Performance Check section to ensure that bandwidth is within specification.

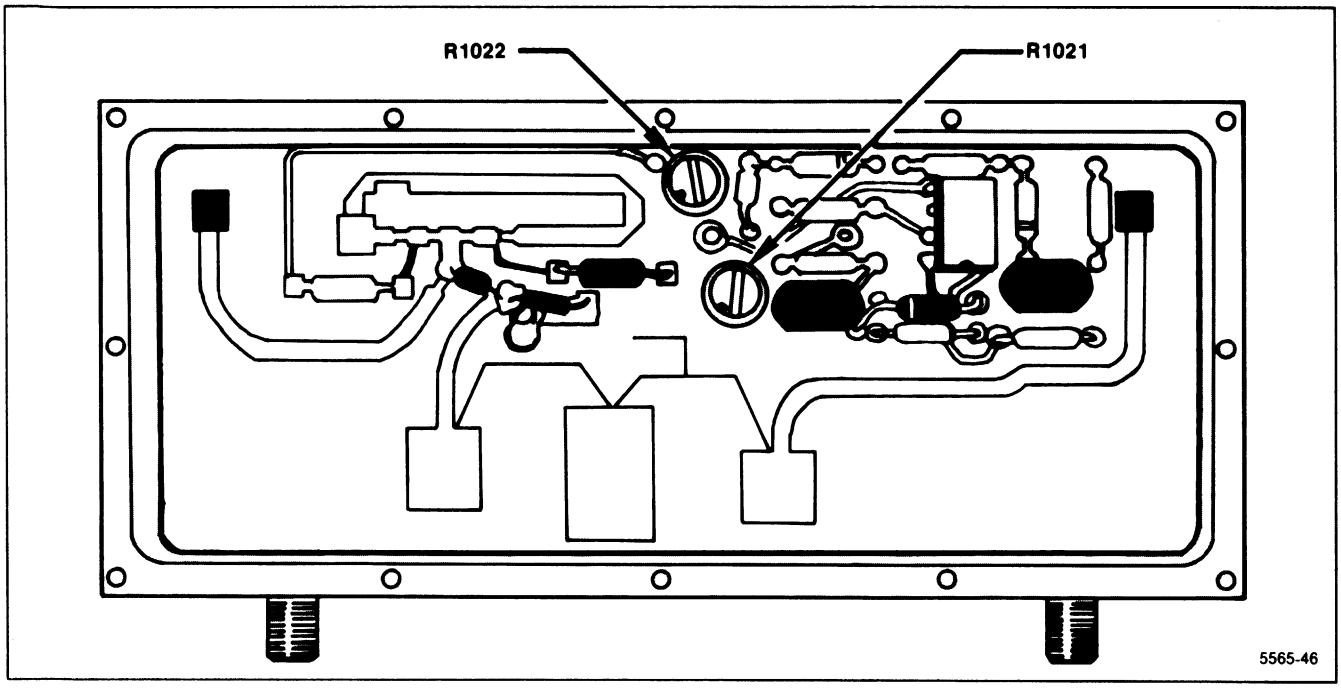


Figure 6-13. 2072 MHz Converter bias adjustments.

Troubleshooting and Calibrating the 2nd LO

The 2182 MHz Oscillator and 2200 MHz Reference Mixer contain critical printed elements that are difficult to repair. Therefore the board should be replaced if damaged. If the oscillator frequency is beyond adjustment with the frequency adjust tab after replacing either the varactor or the oscillator transistor for the 2182 MHz Oscillator, the circuit board must be replaced.

Even though repair can be accomplished by replacing the board, it is recommend that the instrument or assembly be returned to your Tektronix Service Center for repair to ensure best performance.

The 2182 MHz 2nd LO requires calibration only when a component within the assembly has been replaced.

Table 6-8 lists test equipment required to calibrate the L.O. section, and Table 6-8 lists equipment for the Phase Lock section.

1. Check 2nd L.O. Frequency (2182 MHz ±1 MHz)

The reference frequency position set up in this step will also be used in the adjustment procedure.

a. Connect the test equipment as shown in Figure 6-14.

b. Set the Spectrum Analyzer to Max Span.

c. Set the test spectrum analyzer front-panel as follows:

Frequency	2 GHz
Frequency Span/Div	10 MHz
Reference Level	+20 dBm
Auto Resolution	On
Vertical Display	10 dB/Div
Digital Storage	View A & View B
Time/Div	Auto
Triggering	Free Run

d. Set the Time Mark generator for 0.1 s markers. Markers should appear on the test spectrum analyzer display, approximately one marker/division.

e. Peak the 2.0 GHz signal for maximum amplitude with the peaking control, if available.

f. Using the 2 GHz signal as a starting point, begin counting markers until the 18th marker is located. The 2 GHz signal should be greater in amplitude than the time markers. The frequency must be tuned towards 2.18 GHz to locate the 18th marker. Increase the reference level as necessary to view the markers.

g. Center the 18th marker on the test spectrum analyzer (center frequency should be approximately 2.18 GHz).

h. Reset the test spectrum analyzer frequency span/division to 1 MHz.

i. Position the 18th marker 2 major divisions to the right of the center graticule line on the test spectrum analyzer (center frequency should be approximately 2.182 GHz), then activate SAVE A.

j. Disconnect the output of the comb generator from the rf input of the test spectrum analyzer.

k. Reset the Reference Level of the test spectrum analyzer to +10 dBm. Connect the 2ND LO output, from the spectrum analyzer under test, to the rf input of the test spectrum analyzer.

l. Check that the 2nd L.O. output signal is within one major division of the center graticule line (2.181 GHz to 2.183 GHz).

m. If the frequency of the 2nd L.O. is greater than 2.1813 MHz or less than 2.181 MHz, adjustment is required. The SAVE A display reference used in part l will be used in the adjustment procedure.

Table 6-8
EQUIPMENT REQUIRED FOR 2nd LO CALIBRATION

Test Equipment	Characteristics	Recommended Type
Spectrum Analyzer	Frequency range to 2.2 GHz	TEKTRONIX 275X-Series or 7L14 Option 39
UHF Comb Generator	500 MHz Pulse Input	Tektronix 067-0885-00 Calibration Fixture with TM 500 Series Power Module
Time Mark Generator	0.1 μs markers; accuracy 0.001%	TEKTRONIX TG 501 with TM 500 Series Power Module
Signal Generator	Calibrated 100 MHz, with ±20 kHz accuracy	Hewlett-Packard Model 8640 A/B
Voltmeter	Measures to within 0.01 V, impedance ⩾1 MΩ	TEKTRONIX DM 502A with TM 500 Series Power Module
Variable Power Supply	0 to 12.5 V, accurate to 0.1 V	TEKTRONIX PS 501 with TM 500 Series Power Module
Terminations (2)	50Ω, 3 mm connectors	Tektronix Part No. 011-0049-01

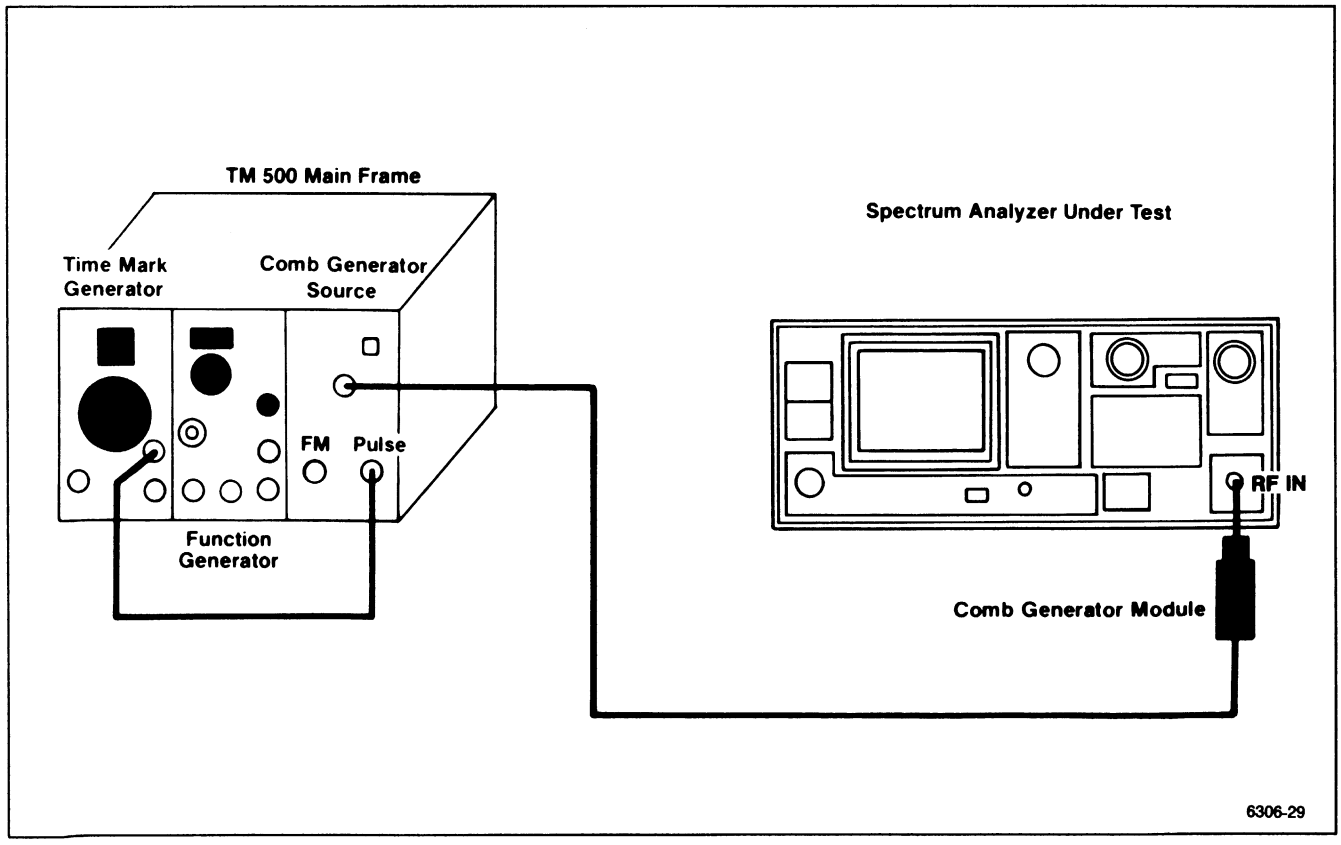


Figure 6-14. 2182 MHz 2nd LO frequency accuracy test setup.

Preparing the 2nd L.O. Assembly for Adjustment

Test equipment setup is shown in Figure 6-15. Turn the POWER off. Remove the cabinet. Place the Spectrum Analyzer on its side so the RF deck is exposed. Use a 5/16 inch wrench to loosen and remove the two semi-rigid cable connections to the assembly. Remove the flexible coaxial cable connection to the 100 MHz input.

Remove the 14 screws that hold the cover on the mu–metal section and remove the cover. Unsolder the leads to feedthrough capacitors C2203 and C2204. (These are the center two feedthrough terminals that feed through the circuit board, as shown in Figure 6-16.)

Replace the cover using two or three screws to hold the cover in place.

Remove the mounting screws for the 2nd L.O. assembly. Carefully lift the 2nd L.O. assembly from the chassis and turn it over so the machined aluminum housing is up. Be sure that the power input connections remain intact. Place the assembly on a flat surface. Use a 5/64 Allen wrench to remove the screws holding the lid on the machined aluminum housing, and remove the lid, exposing the three RF circuit boards within the oscillator section.

Install a 50Ω terminator on the 2182 MHz buffered output port, P222 (see Figure 6-17).

2. Adjust 2nd L.O. Frequency (2182 MHz ±1 MHz)

a. Connect the test equipment as shown in Figure 6-15.

b. Set the variable power supply to 0 V. Connect the plus positive (+) terminal to the 2nd LO housing and the negative (–) terminal to the exposed end of C2203 and L2031, through a 1 kΩ resistor.

c. Apply a 100 MHz, 0 dBm signal from the signal generator to the 100 MHz Reference input port, P221. (Frequency must be within 20 kHz of 100 MHz.)

d. Connect the test spectrum analyzer to the 2182 MHz unbuffered output port, P220. This is the test spectrum analyzer with the reference frequency position already set up in step 1. DO NOT POSITION ANY OF THE CABLES OVER THE 2ND LO ASSEMBLY OSCILLATOR SECTION BECAUSE THEY CAN AFFECT THE FREQUENCY OF THE OSCILLATOR.

e. Bend the feedback and frequency adjusting tabs, C1021 and C1022 (C and D in Figure 6-17) so they are approximately 30 degrees above the board surface.

f. Apply power to both the Spectrum Analyzer and the variable power supply. Set the voltage output from the variable power supply to 5.0 V. Voltage on C2203 should now equal, –5 V and a signal should appear on the test spectrum analyzer.

g. Check for a voltage of +10.0 V, ±0.7 V across C2023.

h. Check Vbe at TP1015 (B in Figure 6-17). If Vbe is greater than +0.5 V, push the feedback adjustment tab down slightly and if less than –0.3 V, lift the tab. If Vbe is greater than +0.8 V, replace the microstrip oscillator board. If Vbe is more negative than –1 V, check the bias circuitry. Adjust the tab so Vbe is +0.15 V, ±0.05 V at TP1015. Do not touch the feedback tab while measuring voltages.

i. Check that the 2nd L.O. signal (frequency) is within one major division of the center graticule line (2.181 GHz to 2.183 GHz). Bend the frequency adjustment tab C1022 (D in Figure 6-17) to bring the oscillator within tolerance. (Bend the tab up to increase frequency and down to lower frequency.)

j. If unable to bring the oscillator frequency within range with the adjustment tab, the frequency of the 2182 MHz oscillator can be brought within range of the adjustment tab by shortening a transmission line stub (A in Figure 6-17). Graduation marks along the side of the stub provide a guide to calculate frequency correction. Each minor mark from the end or cut across the stub, represents an approximate change of 25 MHz.

k. Check the frequency by noting the test spectrum analyzer display. If the frequency is too high, the stub must be lengthened by soldering a bridge across the cut. Recheck the frequency. If the frequency is too low, the stub must be shortened.

l. Shorten the line so the frequency is near 2200 MHz. For example: The frequency difference between the desired and the actual divided by 25 MHz, equals the number of minor divisions from the line end for the new cut. Make a cut across the line and check that the new frequency is near 2200 MHz. Repeat as necessary, the use the adjustment tab to bring the oscillator within tolerance.

m. Check 2182 MHz output power.

NOTE

Before making power measurements, ensure that the unused port is terminated into 50Ω. Unterminated ports will degrade both frequency and power measurements.

(1) Check for 0 dBm ±3 dB output power at the unbuffered port, P220.

(2) Connect the test spectrum analyzer to P222, terminate P220 in 50Ω, then check for an output level of +10 dBm ±3 dB from the buffered port.

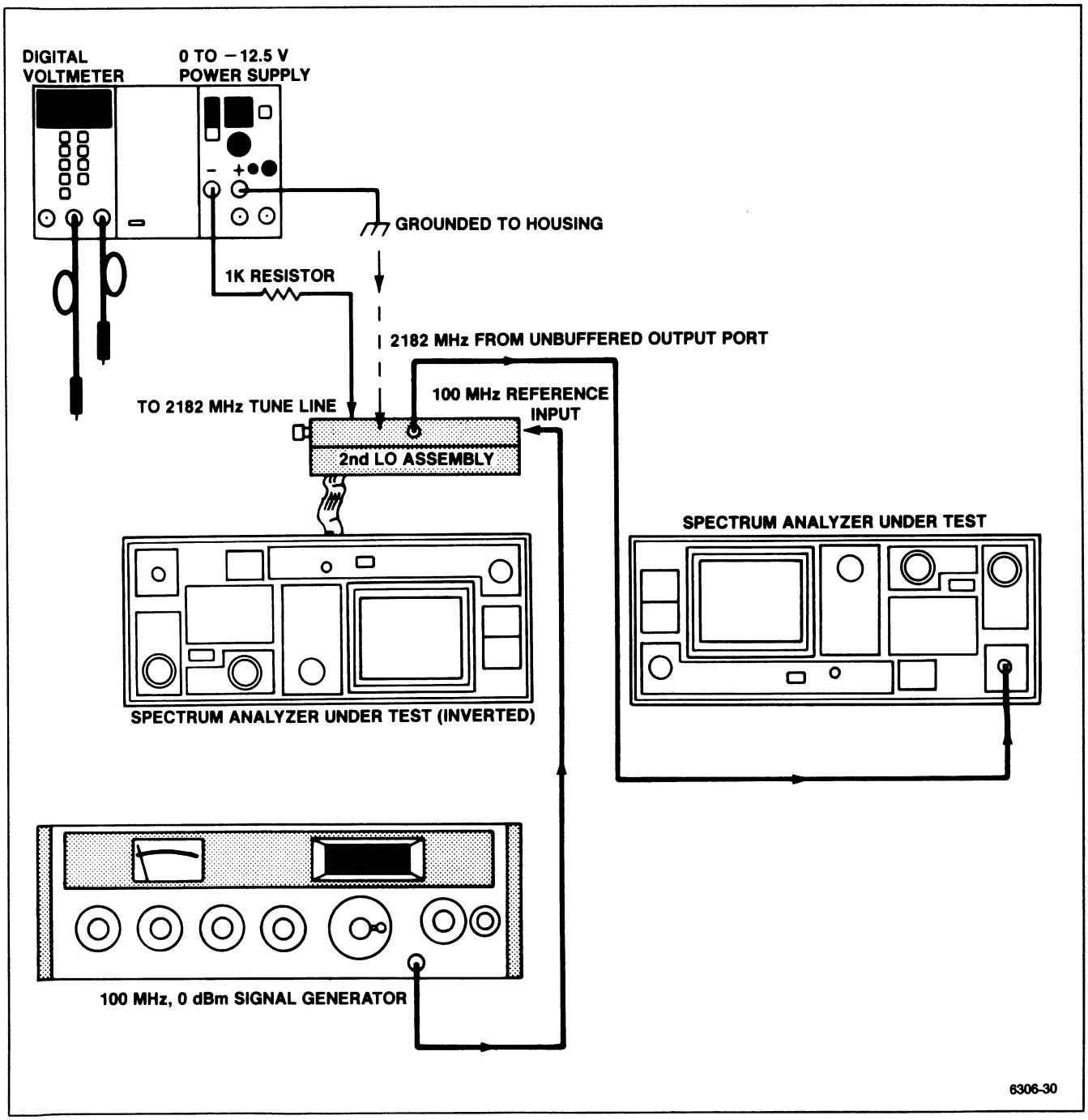


Figure 6-15. 2182 MHz Phase Locked 2nd LO adjustment setup.

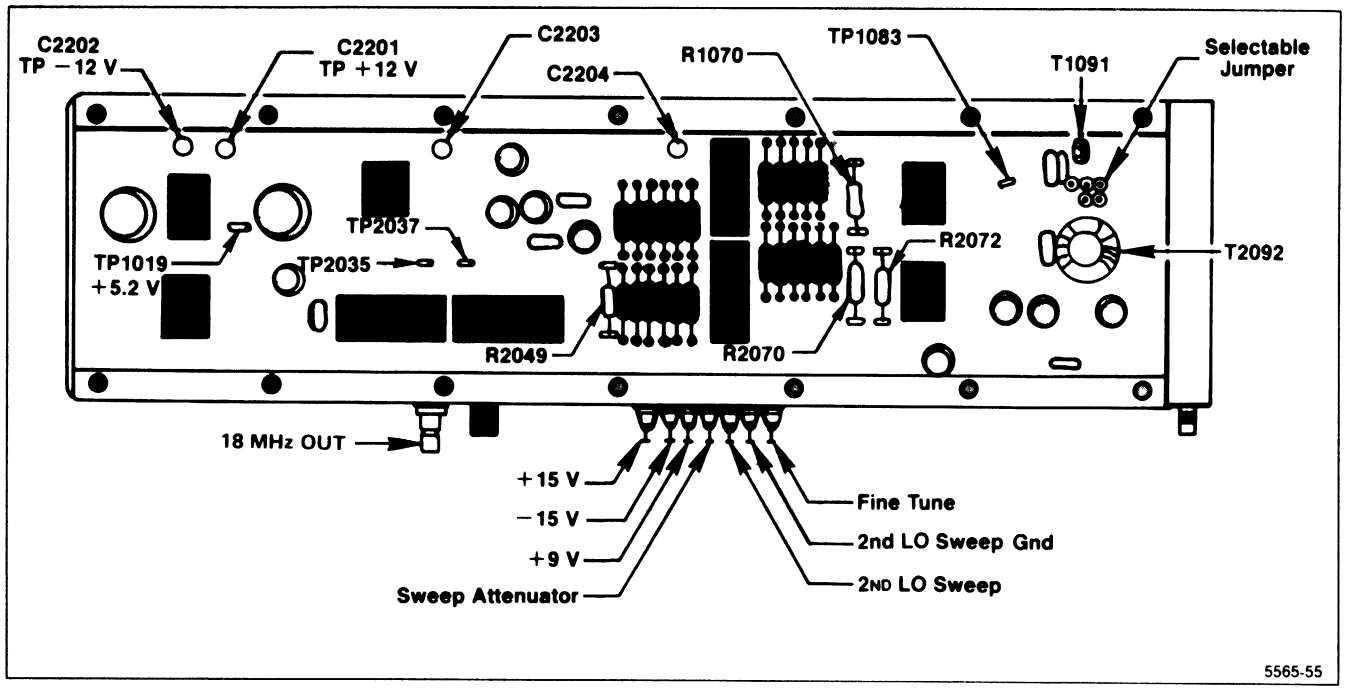


Figure 6-16. 16—20 MHz Phase Lock circuit test point and component locations.

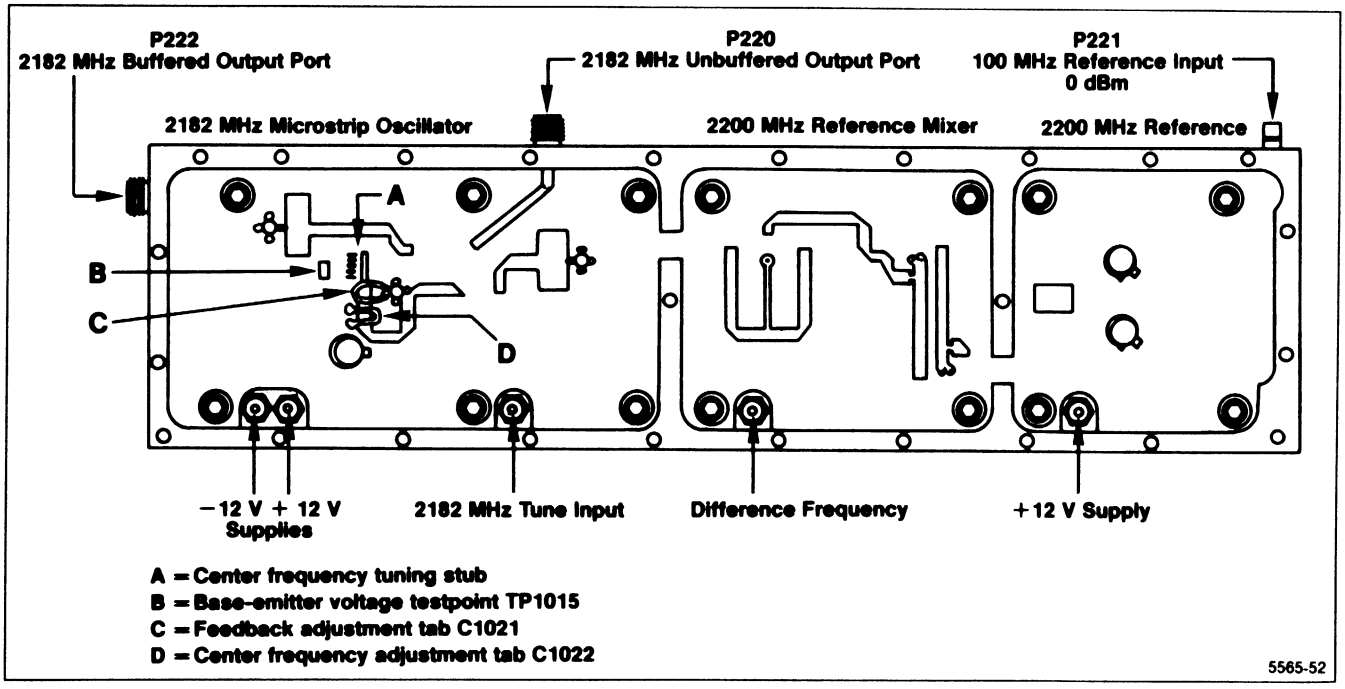


Figure 6-17. 2182 MHz Phase Locked 2nd LO adjustment and test point locations.

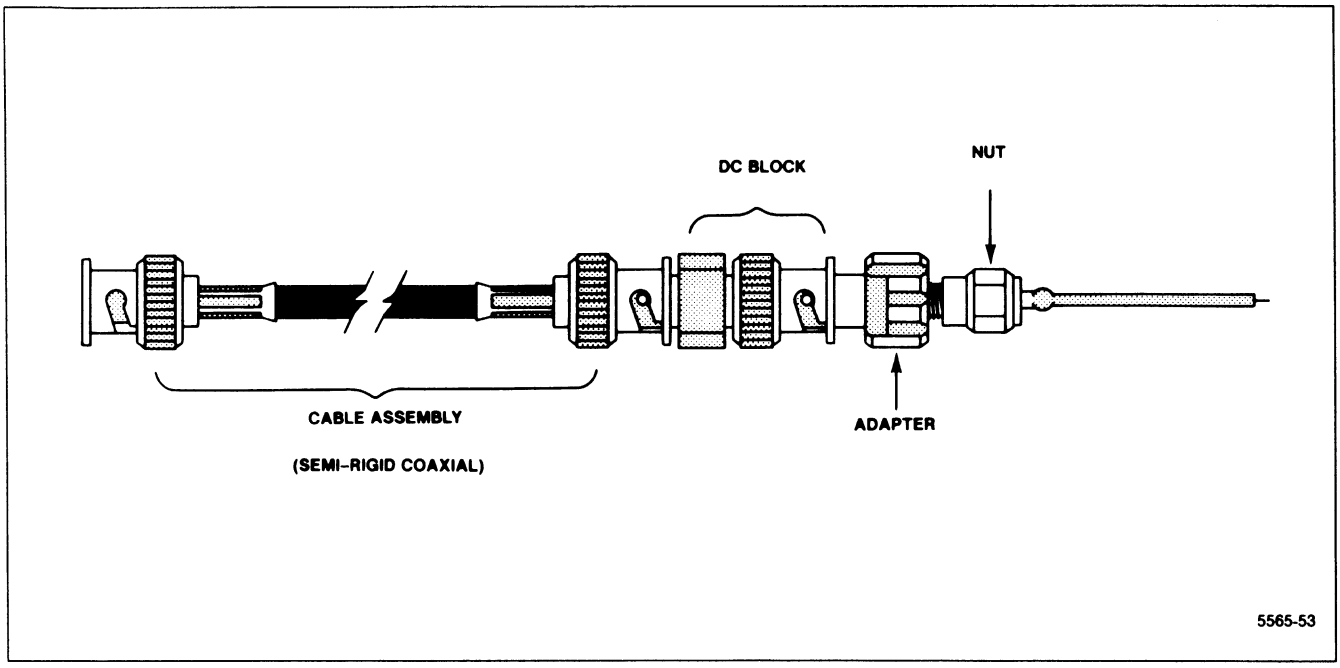


Figure 6-18. Coaxial test probe construction details.

3. Check the 2200 MHz Reference Mixer

a. Use a probe, consisting of a short length of semi-rigid coaxial cable with a dc block (see Figure 6-18), to connect the output of the reference mixer at C2204 to the input of the test spectrum analyzer. Ground the outer shield of the coaxial cable against the 2nd LO housing.

b. Confirm that the output signal frequency is 18 MHz ±1 MHz. Adjust the tab C1022 (Figure 6-17) for the 2182 MHz Microstrip Oscillator, to bring the 18 MHz within the 1 MHz tolerance.

c. Confirm that the output level of the 18 MHz signal is approximately −36 dBm. If the level is below −46 dBm, check the signal levels from the 2200 MHz Reference Mixer and the 2182 MHz Microstrip Oscillator (−28 dBm, ±8 dB from the 2200 MHz Reference Mixer and +8 dBm, ±3 dB from the oscillator).

d. Check the 2182 MHz tune range.

(1) Vary the voltage to the 2182 MHz tune line between 0 V and −12.5 V and note the frequency change at C2204 (the output of the 2200 MHz Reference Mixer).

(2) The frequency should vary between 20 MHz and 35 MHz as the tune line voltage is varied between 0 V and −12.5 V.

Reassembling the 2nd LO Assembly

1. Disconnect and remove the connections from the variable power supply and the test spectrum analyzer.

2. Replace the lid for the oscillator housing and install the 26 screws. Install the screws loosely, then tighten them starting from the center of the lid and progress along the edges toward the corners to insure that no gaps exist between the lid and the housing. Any gaps will allow RF leakage that can produce spurious responses.

3. Reinstall the assembly on the RF deck. Remove the 50Ω terminations and reconnect the cables. Use a 5/16 inch open-end wrench to tighten the semi-rigid coaxial connectors to 8 to 10 inch-pounds.

4. Remove the mu−metal lid and reconnect the leads to feedthrough capacitors C2203 and C2204, on the Phase Lock board (Figure 6-16). Replace the lid and install the 14 screws. Tighten the screws from the center toward the corners of the lid to prevent gaps between the lid and the housing. Do not overtighten because the screws are easily stripped.

Table 6-9
EQUIPMENT REQUIRED FOR CALIBRATING THE
16—20 MHz PHASE LOCK CIRCUIT

Test Equipment	Characteristics	Recommended Type
Digital Voltmeter	Measures to within 0.01 V, impedance ≥1MΩ	TEKTRONIX TM 500-Series DM 501A, DM 502A, or DM 5010
Frequency Counter	Frequency to 80 MHz	TEKTRONIX TM 500-Series DC 503A, DC 508A, DC 509
Time-Mark Generator	Marker output, 1 s to 1 μs; accuracy 0.001%	TEKTRONIX TG 501
Service Kit Extender Board		Tektronix Part No. 672-0865-00

Troubleshooting and Calibrating the 16—20 MHz Phase Lock Section

Replacing oscillator components in this section may alter sweep linearity and frequency of the 16—20 MHz oscillator. The following checks and calibration should aid in repairing and returning the assembly to satisfactory operation.

1. Preliminary

a. Test equipment setup is shown in Figure 6-19. Remove and install the Center Frequency Control board on an extender board.

b. Switch POWER on and set the FREQ SPAN/DIV to 1 MHz.

2. Check Voltages

a. Check all input voltages at the feedthrough capacitors in the housing wall. Refer to Figure 6-16 or the data printed on the lid. The voltage LEVEL at the sweep and tune input lines should be 0 V ±0.05 V with the FREQ SPAN/DIV ≥500 kHz.

b. Switch the POWER off. Remove the lid from the mu–metal housing assembly to gain access to internal circuitry.

c. Switch POWER on, then check the internal regulated voltages; +12 V ±0.4 V at C2201, −12 V ±0.4 V at C2202, and +5.2 V ±0.25 V at TP10109 (see Figure 6-16). Check the output of the shaper at TP1083 for a level between +0.3 V and −0.3 V (0 V ±0.3 V).

3. Setting Center Frequency

a. Connect a frequency counter to TP2035 and note the frequency. If the frequency is 18 ±0.050 MHz no correction is necessary; proceed to part 4 (Setting Tune Sensitivity and Range). If outside the range proceed as follows:

(1) Turn POWER off. Unsolder and remove one end of Shaper Offset resistor R1070. Unsolder the wire strap between T2092 and T1091, at the T1091 end, and lift it free.

(2) Solder a flexible wire jumper to the T2092 end; then, by means of a a plastic tuning tool, attach the free end to one of the three pads for T1091 and note the frequency readout of the counter.

CAUTION

If this flexible wire touches ground while the circuit is operating, the supply regulators can be damaged. The regulators are not protected against a short circuit.

(3) If one of the pads provides a frequency that is within the range of 17.5 MHz ±0.25 MHz, solder the wire strap to this pad. If the frequency is still outside the range, move the jumper to the other pad for T2092 and repeat the procedure. Frequency must equal 17.5 MHz ±0.25 MHz.

b. Turn POWER OFF. Replace R1070 with a 10 turn 25 kΩ potentiometer in series with a 5 kΩ resistor.

c. Turn POWER on and with the counter connected to TP2035, adjust the potentiometer for a frequency readout of 18 MHz ±50 kHz.

d. Turn POWER off, measure the total resistance value and replace R1070 with a 1% resistor of this measured value. Switch POWER on and recheck the frequency to ensure that it is 18 MHz ±50 kHz. Disconnect the counter from TP2035.

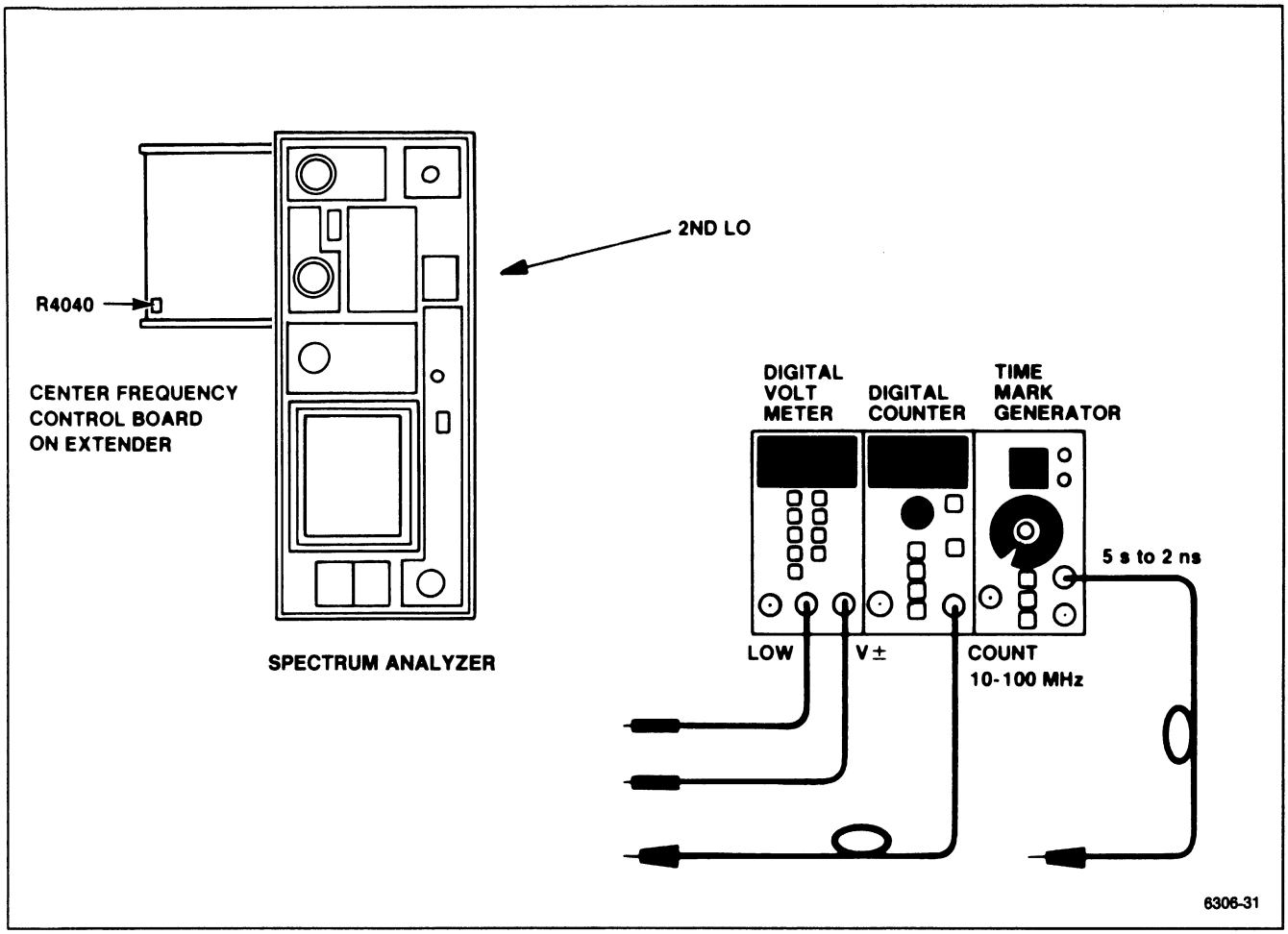


Figure 6-19. 2182 MHz 2nd LO Phase Lock adjustment setup.

4. Setting Tune Sensitivity and Range

a. Center the Fine Tune adjustment R4040, on the Center Frequency Control board and the 2nd LO Sweep adjustment R1067, on the Span Attenuator board (Figure 6-20).

b. Decrease the FREQ SPAN/DIV to 200 kHz or less. The 2nd LO is now in the center of its tune range.

c. Press <SHIFT> 0, 6 to disable continuous tuning of the 2nd LO. Press <SHIFT> 0 and select item #0 (ALTERNATE FREQUENCY DISPLAY), then item #2 (2nd LO FREQUENCY DISPLAY). Readout will now indicate the 2nd LO frequency.

d. Tune the 2nd LO to one end of its range where the frequency readout no longer changes. Note the frequency and measure the voltage on the Tune Line at the input feed-through capacitor (Figure 6-16).

e. Tune the 2nd LO to the other end of its range and again note the frequency and the new voltage reading.

f. Calculate the frequency change per volt (frequency range versus voltage range). Frequency change per volt should equal 128.0 kHz ±10% or range between 115.2 kHz and 140.8 kHz.

g. If the frequency/volt change is low, decrease the value of R2072 (Figure 6-16).

h. Press <SHIFT> 0 and menu item #1, then select the 2nd LO for calibration. Perform the procedure that is called out for adjusting the Fine Tune Range R4040 and Fine Tune Sensitivity R3040 to calibrate the 2nd LO tuning range.

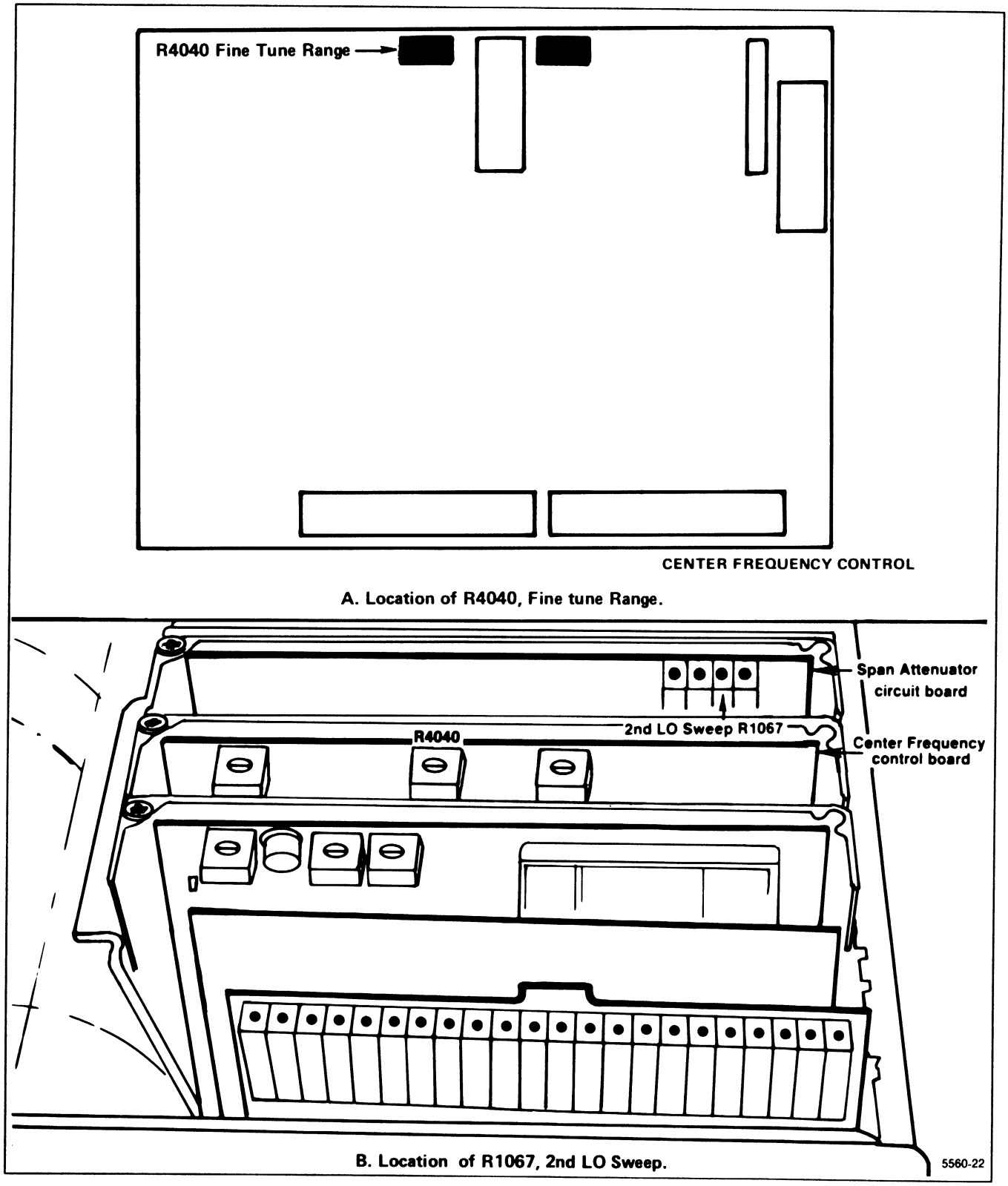


Figure 6-20. Tune and Sweep Range adjustments.

5. Setting Sweep Range

a. Apply 5 μS time markers from the Time Mark Generator to the RF INPUT. Set the FREQ SPAN/DIV to 500 kHz then back to 200 kHz to center the 2nd LO frequency.

b. Adjust the REF LEVEL to display the 200 kHz markers then center one of the markers with the CENTER FREQUENCY control.

c. Adjust the 2nd LO Sweep R1067, on the Span Attenuator board (Figure 6-20), so the comb lines on opposite sides of the screen, are exactly 8 major divisions apart.

6. Check and Adjust Tune Linearity

a. With Frequency Corrections disabled (see part 2), apply 5 μs markers from a Time Mark Generator to the RF INPUT. Set the FREQUENCY to 20 MHz, FREQ SPAN/DIV to 200 kHz and activate AUTO RES. Adjust the REF LEVEL so a comb of 200 kHz markers is displayed.

b. Turn the CENTER FREQUENCY control counterclockwise until the center frequency stops tuning, decrease FREQ SPAN/DIV to 50 kHz then tune the CENTER FREQUENCY up until a marker signal is one major division from the left edge of the graticule. A comb line (or marker signal) should appear on or near the first major division in from the right side of the screen.

c. If the right marker is not exactly 8 divisions from the left marker, note the error to the nearest 0.5 minor division.

d. Turn the CENTER FREQUENCY control clockwise, to increase center frequency, until the next marker signal is one division in from the left edge and again note the spacing between this marker and the marker near the right edge.

e. Continue this process of tuning up in frequency until the center frequency stops tuning, noting the signal spacing at each check point.

f. If the peak-to-peak error is 2.5 minor divisions (25 kHz) or less, the linearity over the center 2 MHz of sweep is satisfactory; if more, the shaper needs adjustment or repair.

g. Switch the FREQ SPAN/DIV to 200 kHz, tune to the low end of the sweep range and note the linearity over the center eight divisions of span, then tune to the high end of the 2nd LO range and again note the linearity. Peak-to-peak deviation should not exceed 0.5 minor division.

h. If the shaper needs adjustment or repair proceed as follows:

(1) A shaper diode or resistor may be defective if the comb line spacing is consistent for part of the tuning range and 30 kHz or more off for the other parts of the sweep. To test the diodes for forward conduction, tune to the low end of the range and short R2049 (Figure 6-16). The output of U1073A (pin 1) should equal about +3 V. U1059 diodes B through G and U2059 diodes A through F should all have a 0.48 V forward drop. Use a floating or digital voltmeter to check the drop.

(2) Turn POWER off then temporarily replace Shaper resistor R2049 with a 20 kΩ potentiometer. Switch POWER on, and adjust the potentiometer to obtain the best overall linearity; decreasing resistance will decrease the spacing between comb lines in the upper portion of the tune range and spread the spacing for the lower portion. Increasing the resistance of R2049 will reverse the effect. When the correct setting is found, turn POWER off, measure the resistance, and replace with a fixed resistor of the same or near the same value.

i. Check the tune sensitivity and sweep range of the 2nd LO. Repeat steps 4, 5, and 6 if necessary.

7. Conclusion

a. Replace the housing lid with its 14 screws.

b. Tighten the screws sequentially, starting from the center of the lid and progressing toward the corners to prevent gaps between the lid and the housing. Use care to not strip the screws as you tighten them.

c. This completes the 2182 MHz Phase Locked 2nd LO calibration. Refer to "Adjust Frequency Control System" in Section 5 for readjusting the system.

Troubleshooting Aids for the 2182 MHz Phase Locked 2nd LO Assembly

NOTE

If the Phase Locked assembly is in the instrument, set the FREQ SPAN/DIV to 500 kHz or more so the 2nd LO is not swept.

The difference frequency from the 2200 MHz Reference Mixer is amplified and fed to output port P224. Nominally the signal at the 18 MHz port is 18 MHz with an output level of approximately −5 dBm into 50Ω. This port is convenient for monitoring the operation of the 16 MHz to 20 MHz voltage controlled oscillator. When phase lock is operating, the difference frequency exactly equals the frequency of the VCO. If loop lock is not functioning properly, the difference frequency signal will either disappear completely or tune to its range limit of approximately 6 MHz or 30 MHz.

Note that when the loop is unlocked, RF leakage from the 16—20 MHz oscillator buffer can be seen at P224 with a level of approximately −35 dBm. The amplified difference frequency can be monitored at TP2035.

Another check of phase lock operation can be done by measuring the dc voltage on the 2182 MHz Tune Line at feedthrough capacitor C2203. Nominally this voltage is approximately −5 V when phase locked. Use a FREQ SPAN/DIV of 500 kHz or greater before measuring. If there is no difference frequency, the voltage will be about 0 V. A voltage of −13 V may indicate loss of signal from the VCO.

Narrow-band noise on the 2nd LO signal may be due to noise modulation of the 16—20 MHz VCO. Monitor the signal at the 18 MHz port to see if the oscillator signal is noisy. Noise on this line is often caused by noise on the ±12 V lines. Use a differential oscilloscope with 1 Hz to 300 Hz bandwidth limits to check supply noise. Measure the ac differential between the supply and the 2nd LO housing. Less than 5 μV peak-to-peak of noise will cause noticeable performance degradation. Output noise from the shaper is typically less than 5 μV peak-to-peak.

When making power measurements of microwave circuitry, at circuit board interfaces, use a coaxial probe with very little stray inductance (see Figure 6-18). Ground the outer conductor of the probe to the circuit housing as close as possible to the measurement port. Disconnect other loads from the measurement point.

100 MHz Oscillator in the 3rd Converter

A variable capacitor, C3031, inside the cover (Figure 6-21), should only need adjusting after a component or components in the 100 MHz oscillator circuit is replaced.

1. With the cover removed, connect a DVM between TP3042 and TP1011 (ground) and adjust C1038 with a non-metallic tuning tool for a reading of +5 V.

2. The Cal Amplitude adjustment, R1045, is described in the Adjustment procedure section.

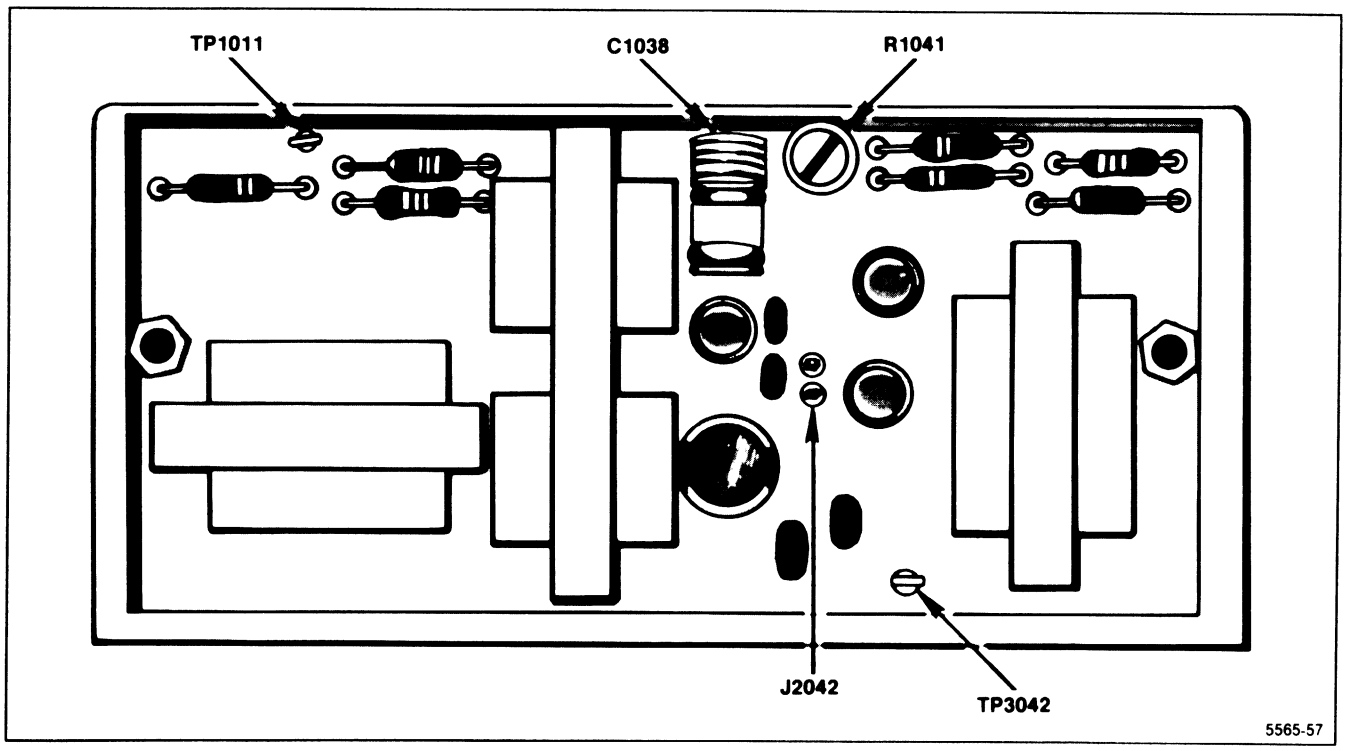


Figure 6-21. 3rd Converter test points and adjustments.

Adjust Baseline Leveling (Video Processor)

(R1013 through R1061 on the Video Processor board)

1. Reset the Spectrum Analyzer by pressing <SHIFT> RESET.

2. Set the Spectrum Analyzer controls as follows:

REF LEVEL	−10 dBm
MIN NOISE	on
VERTICAL DISPLAY	1 dB/DIV
PEAK/AVERAGE	Fully Counterclockwise

3. Connect the test equipment as shown in Figure 6-22. Set the ALC switch on the RF plug-in to MTR position. Set the Power Level for a 4-division excursion (approximately −10 dBm), then adjust the ALC gain on the Sweep Oscillator for stable operation (output stops oscillating).

4. Remove P3035 (Leveler Disable) from the Video Processor board (Figure 6-23).

5. Set the sweep oscillator to the Automatic Internal Sweep (Marker Sweep), sweep time to 100 s, and set it such that the oscillator sweeps from 10 MHz to 1.8 GHz.

6. Activate MAX HOLD, and allow the sweep oscillator to run until the Spectrum Analyzer display is a solid line with no breaks.

7. Activate SAVE A, and deactivate MAX HOLD.

8. Move P2060 (Figure 6-23) to the Invert Mode position (one pin to the left), and replace P3035.

9. Activate WIDE VIDEO FILTER, and set the REFERENCE LEVEL control to bring the noise floor to the center of the crt.

10. Activate B-SAVE A, and deactivate VIEW A and VIEW B.

11. Adjust the leveling potentiometers on the Video Processor board in sequence, starting with R1013 and ending with R1061, for minimum peak-to-peak deviation of the B-SAVE A trace over the full 8-division display. Maximum peak-to-peak deviation allowed is 2 dB.

NOTE

If any peaks and valleys that fall beyond the range of an adjustment are encountered, adjust R1069 to shift the baseline to the right or left then readjust the leveling potentiometers.

12. Replace P2060 to the Normal Mode position.

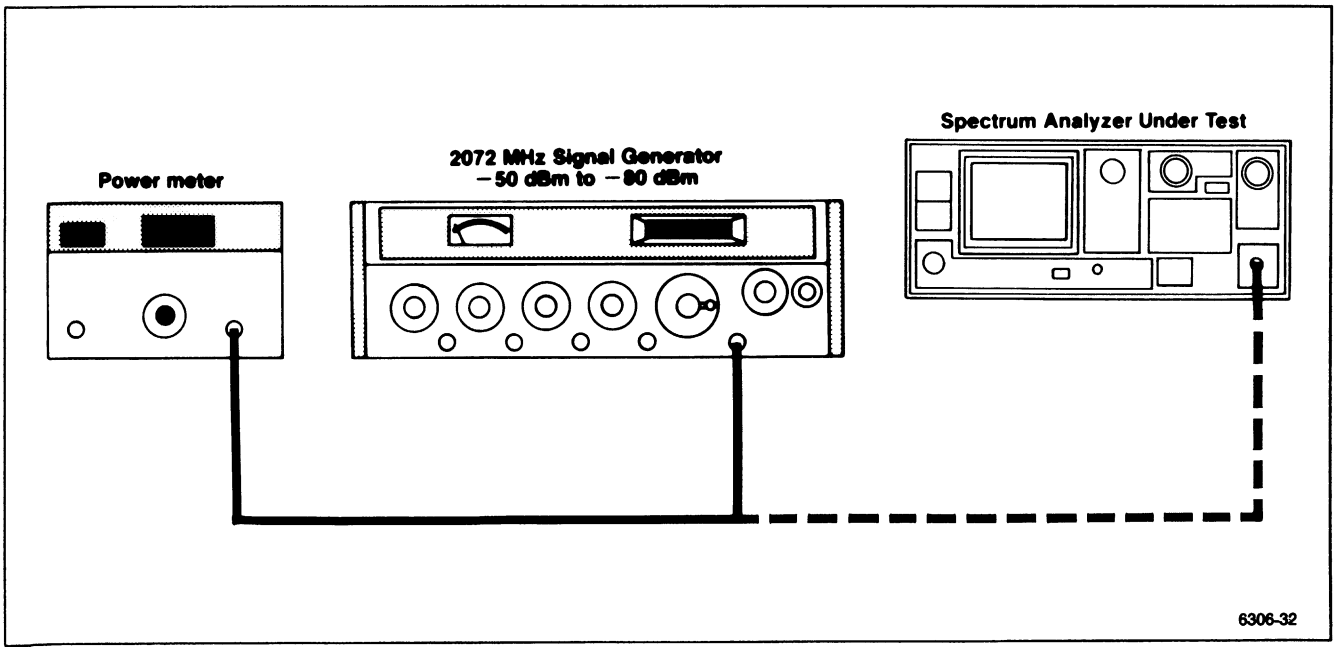


Figure 6-22. Test equipment setup for baseline leveling adjustment.

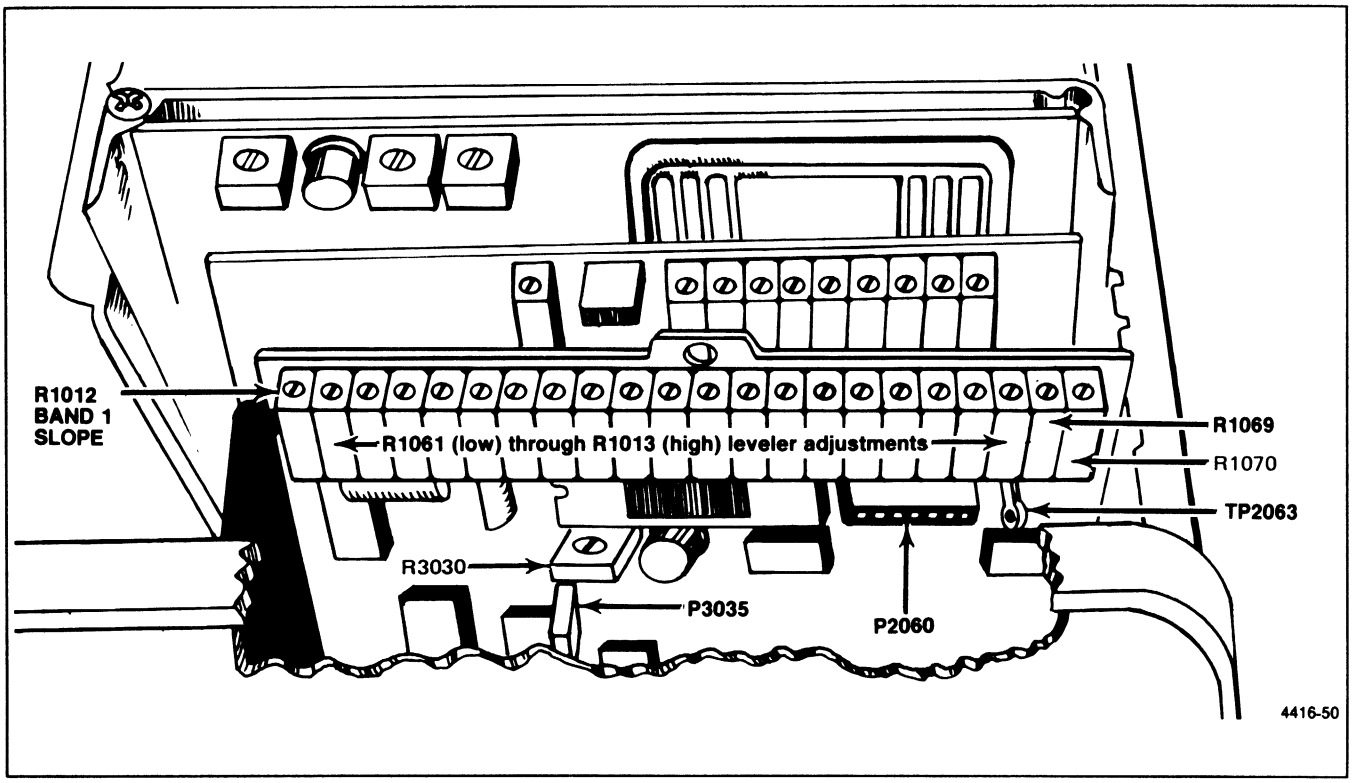


Figure 6-23. Video Processor board adjustment locations.

MICROCOMPUTER SYSTEM MAINTENANCE

Several maintenance aids are built into the microcomputer system. These operating tests demonstrate correct performance or indicate the location of a problem, if any.

The switch settings that set up two of these tests are described first. These are followed by descriptions of the three tests.

In the first test, the microcomputer executes a self-test that verifies, as much as possible, correct operation. RAM, ROM, and interface adapters are checked. Any failure found is indicated by LEDs on the GPIB board.

The second test forces the microcomputer to cycle through all of its addresses. This test requires less of the system to run than does the first test, so it may be used to troubleshoot problems that disable the first test mode.

The third test exercises the instrument bus to isolate problems in data transfer between the microcomputer and the instrument.

Option Switches

S1050 on the Memory board selects the microcomputer system test modes, as well as selecting some instrument options. S1010 on the Z-Axis board selects most of the instrument options exclusively. Table 6-10 shows the selections controlled by the individual switches of S1010 and S1050.

The microcomputer reads these switches only at power-up. Any change in a switch position takes effect when the instrument is next powered up.

Table 6-10
OPTION SWITCH SETTINGS

Switch Position	S1010	S1050
1	Open	Closed except in Option 7 and Option 8 instruments
2	Open	Open
3	Open	Closed
4	Not used	Open
5	Open	Open. This causes the instrument to output front-panel settings (no waveform) when RESET TO LOCAL is pressed in TALK ONLY mode. When set closed, causes the instrument to output both the front-panel settings and the current waveform.
6	Closed in Option 05	Open
7	Open except in Option 07 instruments	7 & 8 closed = Normal Operation 7 closed 8 open = Not defined 7 open 8 closed = Long version of the power-up self test which reports on the GPIB board. 7 & 8 open = Instrument bus test

Power-up Self Test

Normal instrument operation is selected by closing switches #7 and #8 of S1050. At power-up, the processor executes steps 1 and 2, the first part of step 3, and steps 4 and 5 of the Microcomputer System Test (described next). If the first two steps in the test are successful, any problems in the other three steps are reported on the crt. Possible error messages are:

"RAM XX TESTS BAD. PUSH A BUTTON TO CONT."

"ROM XX TESTS BAD. PUSH A BUTTON TO CONT."

"ROM XX MISPLACED. PUSH A BUTTON TO CONT."

"TIMER TESTS BAD. PUSH A BUTTON TO CONT."

Cross-reference tables between the ROM and RAM numbers given in error messages (XX) and the circuit numbers of the parts are given in Table 6-11 and Table 6-12.

If the entire test is successful, the instrument initializes and begins normal operation.

Microcomputer System Test

The microcomputer system test is chosen by setting switch #8 closed and switch #7 open in S1050. The display is inoperative while this test is being performed. The microcomputer reports the test results via the LEDs on the GPIB board rather than on the CRT. If a problem is encountered, the test stops and the problem is indicated by one of the LEDs on the GPIB board. If no problem is found, the system test takes two minutes.

The system test does not begin normal operation after the test is complete.

Addresses are specified as hexadecimal numbers in this description.

1. The microcomputer first verifies the check sum of the system ROM portion of U3050 on the Memory board. The check sum test uses no memory except for U3050. The correct ROM must be installed, the clock on the Processor board must be present, and the microcomputer system bus must be operating correctly.

If the correct check sum is not obtained, the routine halts and lights DS1047 on the GPIB board. If the test stops but does not light DS1047, and everything else seems to be in order, the Address Bus Test (described later in this section) should be performed.

2. The microcomputer next checks part of the processor interface to the instrument bus PIA, U1010, on the Processor board. If the test fails, the routine stops and lights DS1050 on the GPIB board. If the test succeeds, the processor assumes that the instrument bus interface is working, and displays PROCESSOR SYSTEM TEST, PLEASE WAIT. on the crt.

3. The microcomputer next checks RAM. The RAM test contains three parts. The first part performs a quick test of all non-battery backed-up RAM (U1010 and U3020 on the Memory Board). The microcomputer loads the bit pattern 01010101 into a RAM location, reads the location, and compares what is returned to what was stored. The microcomputer then repeats this test with the pattern 10101010. This step does not rely on the RAM being good to execute.

If a reading error occurs, the microcomputer stops the test and pulses LED DS1048 on the GPIB board the number of times corresponding to the RAM that failed the test (refer to Table 6-11).

The second part of the test is a Moving Inversions test of all RAM (volatile and non-volatile). This test assumes that a few byes of the RAM are good. If a RAM fails this test, DS1048 on the Memory board is pulsed as described earlier.

Table 6-11
RAM TEST

RAM Number	RAM Socket	DS1048 Pulses
1	U1010	1
2	U3020	2
3	U1030	3
4	U1020	4

The third part of the test is similar to the first part. However, the memory contents are allowed to reside in memory for thirty seconds before being read back. The results are reported via DS1048.

4. The microcomputer next performs a check sum test of all ROMs. The check sum stored in each ROM is compared to the check sum formed by the successive 16-bit spiral sum of each byte in the ROM, starting at the third location in the ROM. The ROM number coded into each ROM will cause an error if a ROM is installed in the wrong location.

The Tektronix part number is also coded into each ROM. If the part number suffix and its complement, which are stored in the fifth and sixth bytes of the ROM header, do not read as complements, the microcomputer assumes that no ROM is installed and does not attempt the checksum test.

If a bad or misplaced ROM is found, the microcomputer pulses DS1049 on the GPIB board N+1 times, where N is the number of the ROM in error (e.g., a bad ROM #3 will cause four pulses; refer to Table 6-12). Missing ROMs are reported as described in part 6.

Table 6-12
ROM TEST

ROM Number	ROM Socket	Board	DS1049 Pulses
0	U3060	A54 Memory	1
1	U3060	A54 Memory	2
2	U1010	A56 GPIB	3
3	U1010	A56 GPIB	4
4	U1020	A56 GPIB	5
5	U1020	A56 GPIB	6
6	U1025	A56 GPIB	7
7	U1025	A56 GPIB	8
8	U1035	A56 GPIB	9
9	U1035	A56 GPIB	10
10	U3015	A56 GPIB	11
11	U3015	A56 GPIB	12
12	U3020	A56 GPIB	13
13	U3020	A56 GPIB	14
14	U3030	A56 GPIB	15
15	U3030	A56 GPIB	16
16	U3050	A54 Memory	17
17	U3050	A54 Memory	18

5. The microcomputer next tests U2015, a timer chip on the Processor board. If any of the timers in U2015 result in time delays that are too short or too long, the test stops with LED DS1053 on the GPIB board lit.

6. The microcomputer resets the GPIA, U2050, on the GPIB board and checks to see that the GPIA is not addressed to talk or listen. The GPIA is set to the listen-only mode and checked to see that it is addressed to listen. The GPIA is then set to the talk-only mode and checked to see that it is addressed to talk. If any part of this step fails, the test stops and LED DS1052 on the GPIB board is lit.

If all steps in the test are successfully completed, the microcomputer lights LED DS1054 on the GPIB board. The LED is lit continuously if no empty ROM sockets are found, or pulsed the number of times corresponding to the number of empty ROM sockets found. If the number of pulses is greater than the number of absent ROMs, a ROM (or ROMs) was missed in step 4. Look for a problem on the chip-select line or on the D7 data bus line.

If the microcomputer system passes the test, but does not control the instrument, run the Instrument Bus Check described later in this section.

Address Bus Test

Select the address bus test by moving jumper P3015 on the Processor board to the TEST position. This forces the microprocessor (U1025) data lines to hexadecimal 5F. As a result, the microprocessor continuously executes a CLR B instruction, and repetitively cycles through all of its address space. There should be a known pattern on the microcomputer address and control lines and at the output of the address decoders. This allows qualified service personnel to correct problems that prevent the microcomputer from running its self-test.

The spectrum analyzer will not function while running this test.

Microcomputer Bus — As the microcomputer cycles through its address space, it toggles the address lines. The MSB, A15, has a period of approximately 1540 ms. Each line, A14 through A0, has a period half that of the previous line. Thus, the LSB A0 has a period of approximately 4.7 μs. High-order lines A15 through A12 are shown in Figure 6-24. Ignore the narrow pulses that may be evident during the low portion of each cycle.

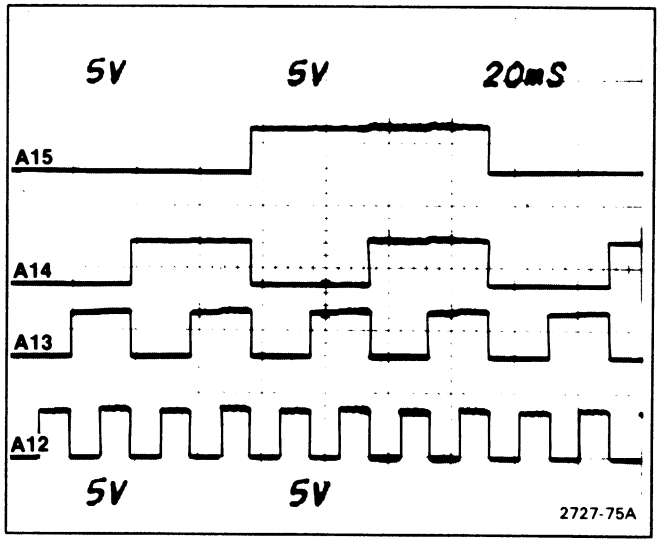


Figure 6-24. A15 through A12 in microcomputer test mode.

The data lines on the microprocessor side of U2025 on the Processor board are static; D7 and D5 are low, the others are high. The TEST position of P3015 disables U2025. On the bus side of this buffer, the data lines are driven by the various memory devices on the bus as they are addressed.

Examining the data lines can locate shorted or open lines; i.e., lines inactive at high, low, or in-between states or changing in unison, usually to indeterminate logic levels of +1 V to +2 V. A problem related to a particular device may be evident only while that device is addressed.

Memory Address Decoders — Address decoder U2045 on the Memory board sets its outputs low in turn to access blocks of memory space. The four main block-select outputs are shown in Figure 6-25.

OxU3025 on the Memory board decodes the RAM addresses. Because of the power-up condition of the bank select, only one of the non-volatile RAM chips will be selected. The RAM select outputs and their relationship to $\overline{0XXX}$ is shown in Figure 6-26. The non-volatile RAM select output is shown in Figure 6-27.

U3040 and U3045 on the Memory board decode the $\overline{I/O}$ select line and the select line for S1050. These signals are shown in Figure 6-28.

Ignore the narrow pulses evident during the time each output is asserted. The pulses result from address lines toggling between microcomputer cycles.

Processor Address Decoder — Address decoder U3035 on the Processor board decodes several chip-selects. Y0, Y1, Y5, and Y7 are shown in relation to the $\overline{I/O}$ line in Figure 6-29.

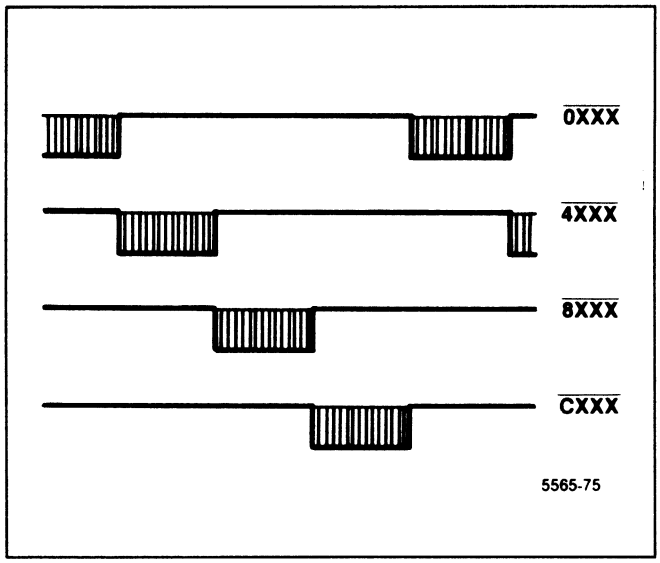


Figure 6-25. Four main block select outputs of address decoder U2045.

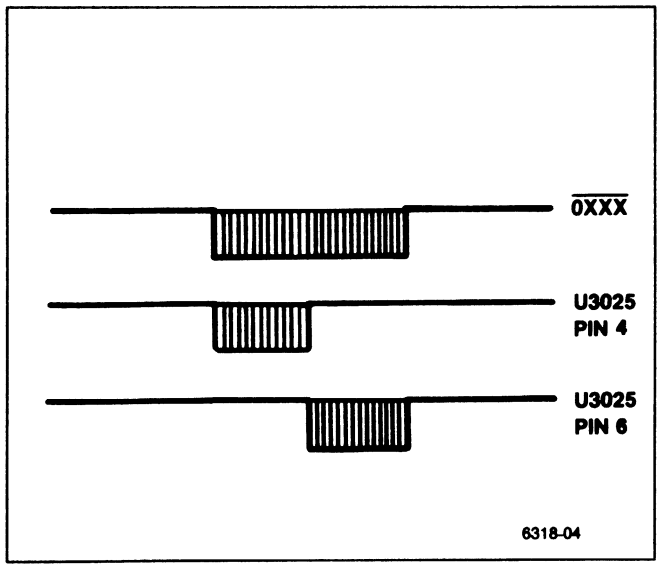


Figure 6-26. RAM select output in relation to $\overline{0XXX}$.

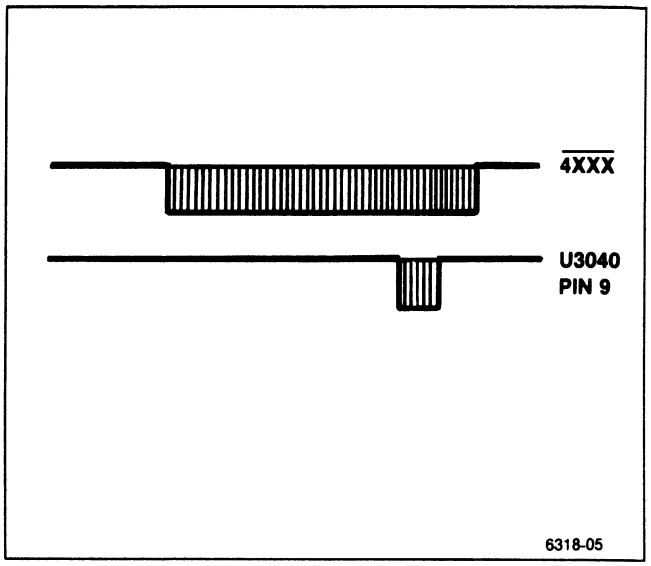


Figure 6-27. Non-volatile RAM select output in relation to $\overline{4XXX}$.

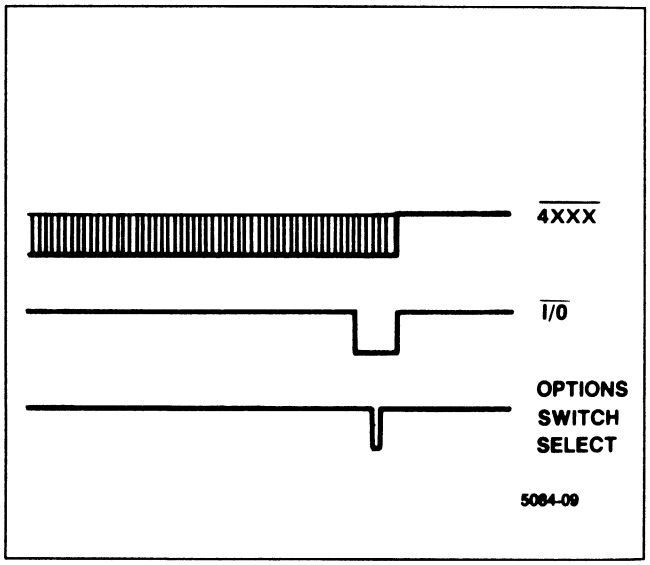


Figure 6-28. $\overline{I/O}$ and S1050 select lines in relation to $\overline{4XXX}$.

GPIB Board Address Decoders — Address decoder U1055 on the GPIB board sets its outputs low to select the GPIA, the GPIB address switch and the bank latch. Y2, Y4, and Y6 are shown in relation to $\overline{I/O}$ in Figure 6-30.

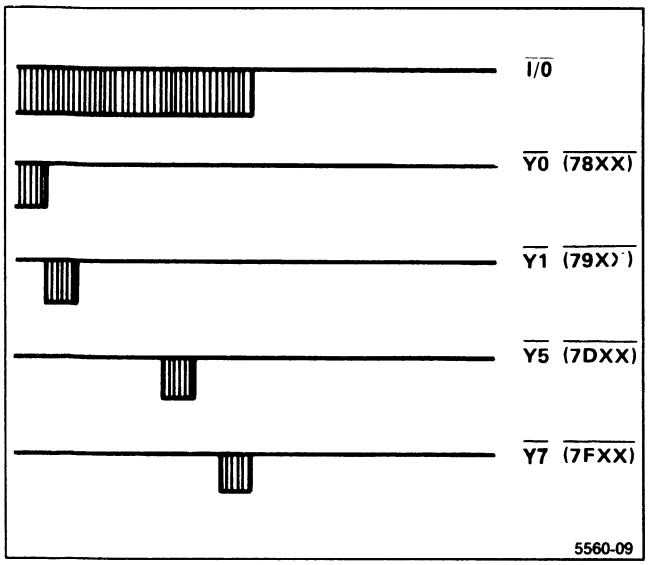


Figure 6-29. Chip selects Y0, Y1, Y5, and Y7 in relation to $\overline{I/O}$.

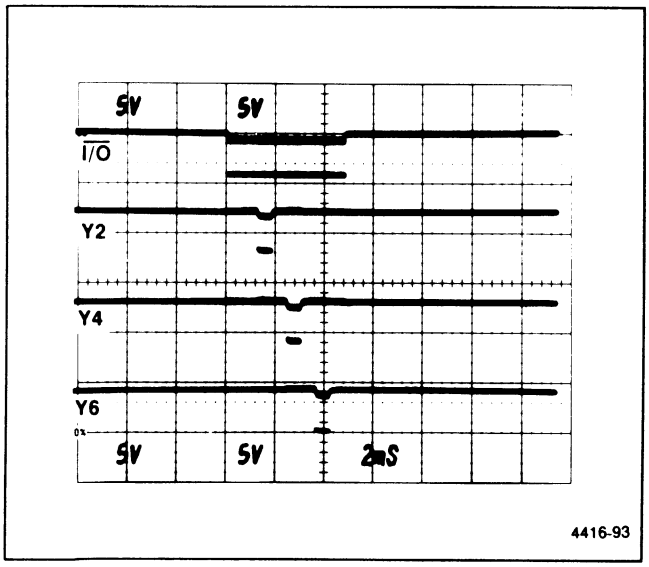


Figure 6-30. Chip selects Y2, Y4, and Y6 in relation to $\overline{I/O}$.

Clocks and Control Lines — The 6808 clock input line should be a square wave with a period of approximately 0.293 μs. The ϕ 2 output on pin 37 should have a period of approximately 1.17 μs. VMA, RESET, NMI, and R/W should be high. $\overline{IRQ}$ instrument bus power up.

Instrument Bus Test

If the microcomputer performs the power-up self-test, but fails to properly control the instrument, the instrument bus interface may be faulty. Select the instrument bus test by setting the option switch as shown in Table 6-10. The microcomputer continuously writes to the instrument bus in a repetitive manner, so the instrument does not operate normally.

The pattern on the instrument bus toggles DATA VALID and POLL and exercises the address and data lines. The address lines change when DATA VALID is low and the data lines change when DATA VALID is high. However, if an assembly on the bus is requesting service because of the way it powered up, DB0-DB4 may continue to change after DATA VALID goes low. In this case, an assembly or assemblies may respond to the high state of POLL and the changing state of AB7 and attempt to report status.

The pattern for the upper address and data lines is shown in Figure 6-31. From address or data line 7 to line 0, each line changes at twice the rate of the previous line, resulting in 128 cycles on the LSB lines. The initial Oxpulse on the upper four data lines is not part of the ÷2 pattern and is not repeated on the lower four data lines. It is possible to discover open or shorted lines by comparing the patterns to those in Figure 6-31, checking that they ÷2. Look for lines that stay high or low, change together or at wrong times in the pattern, or go to indeterminate logic levels (1 V to 2 V).

TROUBLESHOOTING ON THE INSTRUMENT BUS

Instrument Bus Data Transfers

There are two commands and queries provided to aid troubleshooting of circuit functions controlled by the instrument bus. These circuits get data from the microcomputer or respond with data for the microcomputer. The ADDR command and ADDR query set and return the instrument bus address for the DATA command. The DATA command and DATA query set and return data on the instrument bus.

CAUTION

Because the DATA command changes the status of internal hardware, its use may prevent normal Spectrum Analyzer operation. Incorrect settings of some hardware could cause instrument damage.

These commands and queries are transmitted to the Spectrum Analyzer with the PRINT statement. The Spectrum Analyzer response to a query is input into a string variable with the INPUT statement. A string variable is formed by ending the variable name with a dollar sign ($), e.g. A$, X1$.

For the GPIB PRIMARY ADDRESS, enter the decimal equivalent of the spectrum analyzer rear-panel GPIB ADDRESS switch settings.

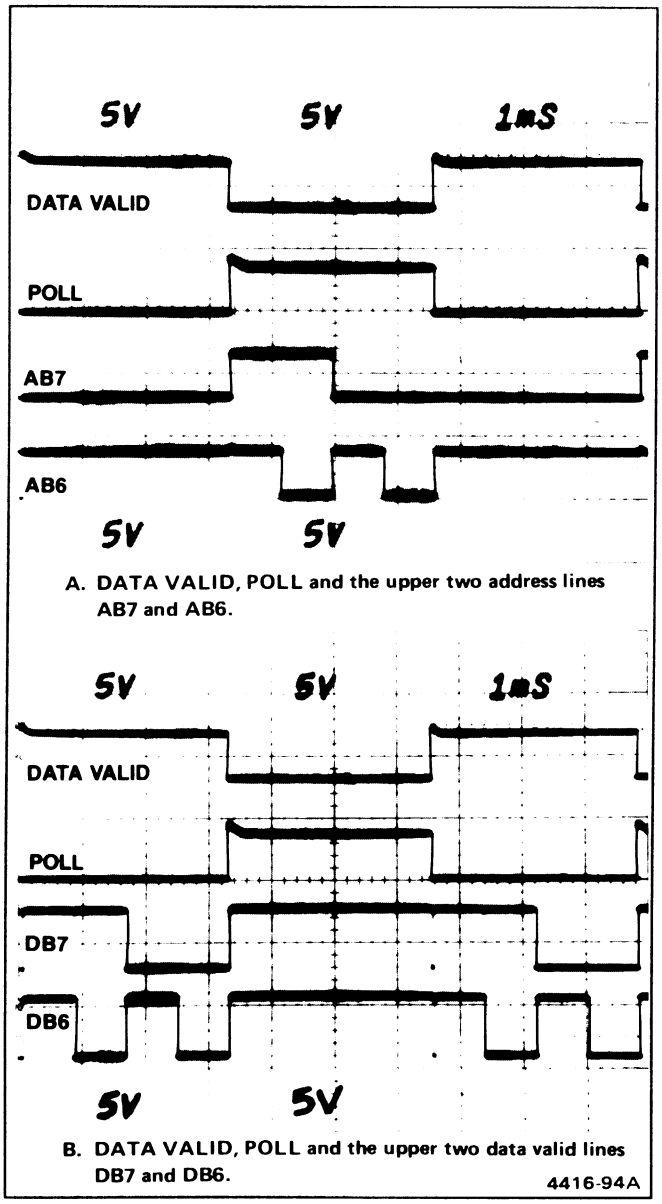
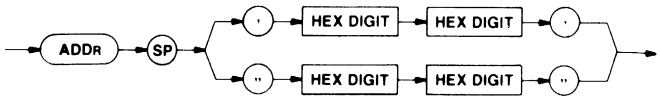


Figure 6-31. Instrument bus check.

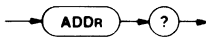
ADDR (instrument bus address) command



4416-04

HEX DIGIT — A character in the sequence 0 through 9 and A through F that represents a hexadecimal digit. The two digits (in order) form a number to represent a location on the instrument bus used by following DATA commands. If a character is not a hexadecimal digit or part of a pair of digits, it is not used to execute the ADDR command, and an error is reported.

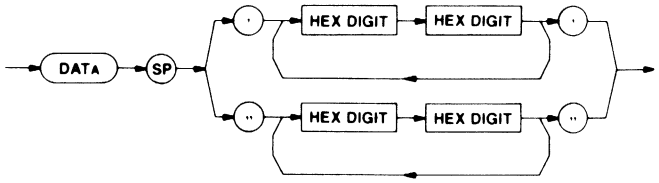
ADDR (instrument bus address) query



4416-05

Response to ADDR query

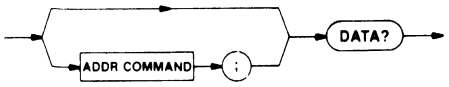
DATA (instrument bus data) command



4416-07

HEX DIGITS — As with ADDR, a pair of digits forms a hexadecimal number. The number is a data value to be sent on the instrument bus to the location specified by the last ADDR command. This allows internal spectrum analyzer parameters to be set for service; these parameters control functions by setting the status or mode of spectrum analyzer circuit assemblies. Up to 16 pairs of characters are accepted. If a character is not a hexadecimal digit or part of a pair of digits, the data byte formed by the pair is not executed and an error is reported. Also, an error is reported when data is sent to an invalid address.

DATA (instrument bus data) query

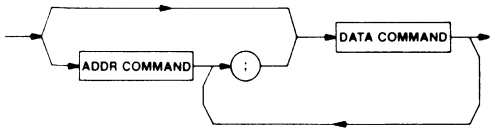


4416-08

Response to DATA query

4416-09

Combined ADDR command and DATA command



4416-10

The address command may precede a data command or query to identify the instrument bus location as part of the same message.

Errors related to these commands are 41, invalid DATA or ADDR argument contents, and 42, DATA direction not compatible with ADDR direction.

Instrument Bus Registers

Registers provide the link between the instrument bus and microcomputer controlled functions. The registers are defined here in the same order as they appear in the Diagrams section. The definitions are provided to help in constructing DATA commands and interpreting responses to DATA queries.

The data is presented here as binary. In some cases a data value occupies the entire register width; for instance, a value in digital storage. In other cases, a single bit or group of bits in the register forms a code; for instance, the upper five bits in the sweep rate and mode register indicate the sweep time/division. The meaning of the data is not fully defined here; refer to the description of the circuit module in Section 5 for details.

To use the binary codes presented here with the DATA command and query statements, you must convert binary to hexadecimal. The binary code number 01001011 is used as an example in the following steps.

1. Group the lower four bits and the upper four bits (break the data byte in half).

01001011 = 0100 1011

2. Convert each group of four bits to a hexadecimal digit. Hexadecimal digits range from 0 to F in the sequence 0123456789ABCDEF.

0100 = 4
1011 = B (i.e., 8+0+2+1=11, which is hexadecimal B)

3. Group the two hexadecimal digits together, keeping their respective places.

4 and B make the two-digit hexadecimal number 4B

The information in Table 6-13 is separated by registers. The following information is related to the table information by leading alpha designators.

A. Variable Resolution (refer to diagram 15)

The microcomputer writes to two variable resolution registers. The data MSB steers the other bits that are defined into the desired register. When DB7 equals 1, it steers DB0 through DB2 to select the resolution bandwidth. When DB7 equals 0, it steers DB6 through DB0 to select the amount of gain added in the VR section and the band leveling gain (gain adjustment related to front-end response in each band). These two functions are addressed and set together by the same data byte.

B. Log and Video Amplifier (refer to diagram 19)

There are two registers that receive data from the microcomputer. One register controls video offset (78) and the other controls the display modes and the vertical scale factor (79).

C. Video Processor (refer to diagram 21)

Register 7C controls out-of-band clamping, video filtering, and leveling.

D. Digital Storage, Vertical (refer to diagram 22)

Registers 7A and FA on the Vertical Digital Storage board transfer display data to and from the microcomputer for spectrum analyzer GPIB operations. Register 7B controls digital storage functions.

E. Z-Axis & RF Interface (refer to diagram 25)

Register 4F on the Z-Axis & RF Interface board enables Z-axis and RF attenuator control. Register CF reports power supply status.

F. Crt Readout (refer to diagram 27)

Register 5F controls crt readout and data steering. Register 2F accepts data from the microcomputer.

G. Sweep (refer to diagram 28)

The microcomputer writes to registers 0F and 1F to control sweep rate, mode, holdoff, interrupts, and triggering.

H. Span Attenuator (refer to diagram 29)

Registers 75 and 76 control the span attenuator.

I. 1st LO Driver (refer to diagram 30)

Register 72 controls functions on the 1st LO Driver board.

J. Center Frequency Control (refer to diagram 31)

Register 70 is provided for control functions and register 71 is provided for data values for center frequency DAC(s). A read, F0, returns the results of a comparison of the DAC output voltage and a memory voltage.

K. Auxiliary Synthesizer Control (refer to diagram 33)

Register 7D accepts data to set the synthesizer chip, U4041, to output 200 MHz to 220 MHz in 400 kHz steps. Values of R, A, and N are given to determine the output frequency as given by the formula

$$f_{out} = (1/R)(NP+A)$$

where R, the reference division ratio, is set at 5 and P is the prescale value of 32. N values needed are 31 through 34, while A ranges from 0 to 31. (Table 6-14 shows the f_{out} results for given N and A values.)

L. Phase Lock (refer to diagram 35)

Register 73 accepts data to preload the +2n counter and control the synthesizer. Successive reads from register F3 obtain status and counter outputs.

After the counter output register selector is reset, three read cycles return status bits and counter bits in the most significant byte and the remaining counter bits in following bytes.

M. Front Panel (refer to diagram 41)

Reading from F4 accesses the keyboard encoder and the CENTER/MKR FREQUENCY control encoder.

Table 6-13
INSTRUMENT BUS REGISTERS

Data Bits 7 6 5 4 3 2 1 0	Description
A. Variable Resolution (3F)	
	Resolution Bandwidth
1 x x x x 0 0 1	1 MHz Resolution Bandwidth
1 x x x x 0 1 0	100 kHz Resolution Bandwidth
1 x x x x 0 1 1	10 kHz Resolution Bandwidth
1 x x x x 1 0 0	1 kHz Resolution Bandwidth
1 x x x x 1 0 1	100 Hz Resolution Bandwidth
1 x x x x 1 1 0	30 Hz Resolution Bandwidth
	Gain, Leveling
0 0 0 0 0 x x x	Band 1 Leveling
0 x x x x 0 0 0	0 dB Gain
0 x x x x 0 0 1	10 dB Gain
0 x x x x 1 0 0	20 dB Gain
0 x x x x 1 0 1	30 dB Gain
0 x x x x 1 1 1	40 dB Gain
B. Log & Video Amplifier	
	Video Offset (78)
DB7–DB0	LSB = 1/4 dB Total range = 63.75 dB
	Modes and Scale Factor (79)
1 x x x x x x x	Pulse stretcher on
0 x x x x x x x	Pulse stretcher off
x 1 x x x x x x	Identify offset on
x 0 x x x x x x	Identify offset off
x x 0 1 x x x x	Lin
x x 1 0 x x x x	Log
x x 0 0 x x x x	Full-screen deflection
DB3–DB0	Log vertical scale factor in dB/div

Table 6-13 (cont)

Data Bits 7 6 5 4 3 2 1 0	Description
C. Video Processor (7C)	
0 1 1 x x x x x	Out-of-band clamp = no clamp
0 0 1 x x x x x	Out-of-band clamp = clamp upper 5 div
1 1 1 x x x x x	Out-of-band clamp = clamp lower div
0 1 0 x x x x x	Out-of-band clamp = clamp lower 5 div
x x x 0 0 0 0 x	Video filter off
x x x 0 0 0 1 x	Video filter 30 kHz
x x x 1 0 0 1 x	Video filter 3 kHz
x x x 1 1 0 1 x	Video filter 300 Hz
x x x 0 0 1 1 x	Video filter 30 Hz
x x x 1 0 1 1 x	Video filter 3 Hz
x x x 1 1 1 1 x	Video filter 0.3 Hz
x x x x x x x 1	Baseline leveling on
x x x x x x x 0	Baseline leveling off
D. Digital Storage	
	Horizontal Digital Storage Board
	7B
1 x x x x x x x	Digital Storage Acquisition Enable
0 x x x x x x x	Digital Storage Acquisition Disable
x 1 x x x x x x	Extended Address 2
x x 1 x x x x x	Extended Address 1
x x x 1 x x x x	Extended Address 0
x x x x 1 x x x	B–SAVE A on
x x x x 0 x x x	B–SAVE A off
x x x x x 1 x x	VIEW B on
x x x x x 0 x x	VIEW B off
x x x x x x 1 x	VIEW A on
x x x x x x 0 x	VIEW A off
x x x x x x x 1	SAVE A on
x x x x x x x 0	SAVE A off
Extended Address 2-0	Subaddress bits for Port 7A giving subaddresses 7–0. Addressing 7A.6 transfers the bus to the Vertical Digital Storage board.
	7A.0
DB1–DB7	Secondary Marker position bits
DB0	Secondary Marker trace bit

Table 6-13 (cont)

Data Bits 7 6 5 4 3 2 1 0	Description
D. Digital Storage (cont)	
	Horizontal Digital Storage Board (cont)
	7A.1
DB8, DB9	Secondary Marker position bits
DB1	Secondary Marker trace bit
	7A.2
DB1–7	Primary Marker position bits
DB0	Primary Marker trace bit
	7A.3
DB8–9	Primary Marker position bits
DB1	Primary Marker trace bit
	7A.4
ADDR7–ADDR0	Digital Storage address bits
	7A.5
DB6	Transfers the bus to the Vertical Digital Storage board.
DB5	Determines if bus transfer is for a single cycle or until it is returned by the Vertical Digital Storage board.
DB4	Disable Update Marker
ADDR9, ADDR8	Loading ADDR7–0 reloads the last ADDR9,8
	7A.7
DB4–7	Primary Marker intensity bits
DB0–3	Secondary Marker intensity bits
	FA
DB0–7	Digital Storage position bits
	FB
DB7	Always low to indicate that it is from the Horizontal Digital Storage board
DB0 & DB1	Digital Storage position bits

Table 6-13 (cont)

Data Bits 7 6 5 4 3 2 1 0	Description
D. Digital Storage (cont)	
	Vertical Digital Storage Board
	FA
DB7–DB0	Data values from digital storage. A write to 7B initializes output to begin at the left of the trace and proceed to the right
	FB
DB7	Always high to indicate that it is from the Vertical Digital Storage board
	7A
DB7–DB0	Data values for digital storage. A write to 7B clears the address counter so values are stored for points on the display starting at the left and proceeding to the right in order
	7B
x 1 1 x x x x x	Peak/Average cursor in knob position
x 1 0 x x x x x	Peak/Average cursor in Peak position
x 0 1 x x x x x	Peak/Average cursor in Average position
x x x 1 x x x x	Max Hold on
x x x 0 x x x x	Max Hold off
E. Z-Axis & RF Interface	
	Z-Axis & RF Attenuator (4F)
1 x x x x x x x	Baseline clipper on
0 x x x x x x x	Baseline clipper off
x 1 x x x 1 x 1	0 dB RF attenuation
x 1 x x x 1 x 0	10 dB RF attenuation
x 0 x x x 1 x 1	20 dB RF attenuation
x 1 x x x 0 x 1	30 dB RF attenuation
x 1 x x x 0 x 0	40 dB RF attenuation
x 0 x x x 0 x 1	50 dB RF attenuation
x 0 x x x 0 x 0	60 dB RF attenuation
x x 0 x x x x x	2 GHz 2nd converter
x x x 0 x x x x	RF INPUT
x x x x 0 x x x	100 ms to switch attenuator
	Power Supplies Status (CF)
x x x x x x 1 x	Fault
x x x x x x 0 x	Supplies okay

Table 6-13 (cont)

Data Bits 7 6 5 4 3 2 1 0	Description
F. Crt Readout	
	Crt Control (5F)
1 x x x x x x x	Spectrum chop enable
0 x x x x x x x	Spectrum chop disable
x 1 x x x x x x	32 characters/line
x 0 x x x x x x	40 characters/line
x x 1 x x x x x	2 lines
x x 0 x x x x x	16 lines
x x x x 1 x x x	Max span dot on
x x x x 0 x x x	Max span dot off
x x x x x x 1 x	Address 2F contains an address
x x x x x x 0 x	Address 2F contains data
x x x x x x x 1	Readout enabled
x x x x x x x 0	Readout disabled to load readout
DB4	A8 (address bit 8)
DB2	A9 (address bit 9)
	Address/Data (2F)
DB7,DB6	If DB1 in 5F = 1 — A7, A6 of address. With A8 and A9 in 5F, they specify the line number (0–F).
DB5–DB0	If DB1 in 5F = 1 A5–A0 of address. This specifies the character position in a line.
DB7	If DB1 in 5F = 0 1 = Character is a space 0 = Character is not a space
DB6	If DB1 in 5F = 0 1 = Skip a line 0 = Don't skip a line
DB5–DB0	If DB1 in 5F = 0 Character code (lower 6 bits of ASCII)
G. Sweep	
	1F
1 x x x x x x x	Extended Address 1
x 1 x x x x x x	Extended Address 0
x x 1 x x x x x	Marker DAC/Ramp Generator
x x x x 1 x x x	Trigger Single Sweep
x x x x x 1 x x	Disable Sweep Gate
x x x x x x 1 x	Disable Trigger
x x x x x x x 1	Abort Sweep
Extended Address 1 and Address 2	Subaddress bits for Port 0F giving subaddresses 3–0. Subaddresses 0 and 1 have the rest of the control bits not on Address 1F. Subaddresses 2 and 3 receive the 12 bits to set the DAC.

Table 6-13 (cont)

Data Bits 7 6 5 4 3 2 1 0	Description
G. Sweep	
	Holdoff, Interrupt, Trigger (0F.0)
x x 0 0 x x x x	Short sweep holdoff
x x 0 1 x x x x	Medium sweep holdoff
x x 1 0 x x x x	Long sweep holdoff
x x x x 0 0 x x	Free run trigger mode
x x x x 0 1 x x	Internal trigger mode
x x x x 1 0 x x	External trigger mode
x x x x 1 1 x x	Line trigger mode
x x x x x x 1 x	Enable end-of-sweep interrupt
x x x x x x x 1	Single Sweep Mode
	Sweep Rate and Mode (0F.1)
x x x 1 1 0 1 1	20 μs Time/Div
x x x 1 0 1 1 1	50 μs Time/Div
x x x 1 0 0 1 1	100 μs Time/Div
x x x 0 1 0 1 1	200 μs Time/Div
x x x 0 0 1 1 1	500 μs Time/Div
x x x 0 0 0 1 1	1 ms Time/Div
x x x 1 1 0 0 1	2 ms Time/Div
x x x 1 0 1 0 1	5 ms Time/Div
x x x 1 0 0 0 1	10 ms Time/Div
x x x 0 1 0 0 1	20 ms Time/Div
x x x 0 0 1 0 1	50 ms Time/Div
x x x 0 0 0 0 1	100 ms Time/Div
x x x 1 1 0 0 0	200 ms Time/Div
x x x 1 0 1 0 0	500 ms Time/Div
x x x 1 0 0 0 0	1 s Time/Div
x x x 0 1 0 0 0	2 s Time/Div
x x x 0 0 1 0 0	5 s Time/Div
x x x 0 0 0 0 0	10 s Time/Div
x x x 1 1 1 1 1	Manual
x x x 0 1 1 1 1	External
	0F.2 (U1045)
DB7-0	Marker DAC value bits
	0F.3 (U1035)
DB3-DB0	Marker DAC value bits
	9F
x x x 0 x x x x	Poll Bit
H. Span Attenuator	
	Span Magnitude (75)
DB7-DB0	Lower 8 bits of 10-bit attenuation code (000 is max attenuation)

Table 6-13 (cont)

Data Bits 7 6 5 4 3 2 1 0	Description
H. Span Attenuator (cont)	
	Span Magnitude and Attenuator (76)
1 x x x x x x x	Gain of U3032 is +1
0 x x x x x x x	Gain of U3032 is −1
x 0 0 x x x x x	×1.0 sweep decade attenuator
x 0 1 x x x x x	×0.1 sweep decade attenuator
x 1 0 x x x x x	×0.01 sweep decade attenuator
x x x 0 0 x x x	1st LO main coil output select and calibration
x x x 0 1 x x x	1st LO FM coil output select and calibration
x x x 1 0 x x x	2nd LO output select and calibration
DB2	For future use
DB1, DB0	Upper two bits of attenuation code
I. 1st LO Driver	
	1st LO Driver Functions (72)
1 x x x x x x x	Normal span mode
0 x x x x x x x	Max span mode
x 1 x x x x x x	Connect sweep voltage to driver
x 0 x x x x x x	Disconnect sweep voltage to driver
x x 1 x x x x x	Driver off (for degauss)
x x 0 x x x x x	Driver on
x x x 1 x x x x	Filter on at driver output (for unphase-locked narrow spans)
x x x 0 x x x x	Filter off at driver output
x x x x x 1 1 0	Internal mixer bias for Band 1
x x x x x 1 1 1	No internal mixer bias selected
J. CENTER/MKR FREQUENCY Control	
	Control (70)
1 x x x x x x x	1st LO storage gate open
0 x x x x x x x	1st LO storage gate closed
x 0 x x x x x x	Steers DAC data to 1st LO high byte
x x 0 x x x x x	Steers DAC data to 1st LO mid byte
x x x 0 x x x x	Steers DAC data to 1st LO low byte
x x x x 1 x x x	2nd LO storage gate open
x x x x 0 x x x	2nd LO storage gate closed
x x x x x 0 x x	Steers DAC data to 2nd LO high byte

Table 6-13 (cont)

Data Bits 7 6 5 4 3 2 1 0	Description
J. Center/Marker Frequency Control (70) (cont)	
x x x x x x 0 x	Steers DAC data to 2nd LO mid byte
x x x x x x x 0	Steers DAC data to 2nd LO low byte
	DAC Data (71)
DB7–DB0	Data for center frequency DAC(s) steered by control register
	CENTER/MKR FREQUENCY Control Read (F0)
DB7	1st LO DAC stored voltage comparator
DB0	2nd LO DAC stored voltage comparator
K. Auxiliary Synthesizer Control (7D)	
DB7–DB4	Synthesizer chip data (D3–D0)
DB2–DB0	Synthesizer chip addresses (A2–A0)
x x x x 1 x x x	VCO enable
x x x x 0 x x x	VCO disable
0 1 0 1 x 1 0 1	This section sets R, the reference divider to 5 yielding a 200 kHz reference frequency.
0 0 0 0 x 1 1 0	
0 0 0 0 x 1 1 1	
A A A A x 0 0 0	This section sets the value of A from 0 to 31
0 0 0 A x 0 0 1	LSB
N N N N x 0 1 0	This section sets N from 31 to 34
0 0 N N x 0 1 1	
0 0 0 0 x 1 0 0	31=1111 32=0000 01 10 33=0001 34=0010 10 10

Table 6-13 (cont)

Data Bits 7 6 5 4 3 2 1 0	Description
L. Phase Lock Control	
	Write (73)
1 x x x x x x x	Clocks data on DB0 into a latch
x x 1 x x x x x	Clears the counters
x x x 1 x x x x	Transfers DB0 serial data to control latch outputs
x x x x 1 x x x	Resets the counter output register selector
x x x x x x 1 x	Transfers DB0 serial data to synthesizer N latches
DB6	Gate mode latch
DB2	NVRAM switch latch
DB0	Serial data for control of synthesizer N latches
	Read (F3)—Most Significant Byte
1 x x x x x x x	Error voltage below a preset amount
x 1 x x x x x x	Error voltage above a preset amount
x x 1 x x x x x	Valid count is in counters
DB4–DB0	Upper five bits of counter output; the remaining 16 bits are in the following two bytes
M. Front Panel	
	Reading Data From Switch Encoders (F4)
1 x x x x x x x	CENTER/MKR FREQUENCY down
0 x x x x x x x	CENTER/MKR FREQUENCY up
DB6–DB0	Switch codes (see Figure 7-33 in Section 7)

Table 6-14
AUXILIARY SYNTHESIZER VALUES AS A FUNCTION OF N AND A

N	A	F_{out} Result	N	A	F_{out} Result	N	A	F_{out} Result	N	A	F_{out} Result
31	8	200.0 MHz	32	1	205.0 MHz	32	26	210.0 MHz	33	19	215.0 MHz
31	9	200.2 MHz	32	2	205.2 MHz	32	27	210.2 MHz	33	20	215.2 MHz
31	10	200.4 MHz	32	3	205.4 MHz	32	28	210.4 MHz	33	21	215.4 MHz
31	11	200.6 MHz	32	4	205.6 MHz	32	29	210.6 MHz	33	22	215.6 MHz
31	12	200.8 MHz	32	5	205.8 MHz	32	30	210.8 MHz	33	23	215.8 MHz
31	13	201.0 MHz	32	6	206.0 MHz	32	31	211.0 MHz	33	24	216.0 MHz
31	14	201.2 MHz	32	7	206.2 MHz	33	0	211.2 MHz	33	25	216.2 MHz
31	15	201.4 MHz	32	8	206.4 MHz	33	1	211.4 MHz	33	26	216.4 MHz
31	16	201.6 MHz	32	9	206.6 MHz	33	2	211.6 MHz	33	27	216.6 MHz
31	17	201.8 MHz	32	10	206.8 MHz	33	3	211.8 MHz	33	28	216.8 MHz
31	18	201.0 MHz	32	11	207.0 MHz	33	4	212.0 MHz	33	29	217.0 MHz
31	19	202.2 MHz	32	12	207.2 MHz	33	5	212.2 MHz	33	30	217.2 MHz
31	20	202.4 MHz	32	13	207.4 MHz	33	6	212.4 MHz	33	31	217.4 MHz
31	21	202.6 MHz	32	14	207.6 MHz	33	7	212.6 MHz	34	0	217.6 MHz
31	22	202.8 MHz	32	15	207.8 MHz	33	8	212.8 MHz	34	1	217.8 MHz
31	23	203.0 MHz	32	16	208.0 MHz	33	9	213.0 MHz	34	2	218.0 MHz
31	24	203.2 MHz	32	17	208.2 MHz	33	10	213.2 MHz	34	3	218.2 MHz
31	25	203.4 MHz	32	18	208.4 MHz	33	11	213.4 MHz	34	4	218.4 MHz
31	26	203.6 MHz	32	19	208.6 MHz	33	12	213.6 MHz	34	5	218.6 MHz
31	27	203.8 MHz	32	20	208.8 MHz	33	13	213.8 MHz	34	6	218.8 MHz
31	28	204.0 MHz	32	21	209.0 MHz	33	14	214.0 MHz	34	7	219.0 MHz
31	29	204.2 MHz	32	22	209.2 MHz	33	15	214.2 MHz	34	8	219.2 MHz
31	30	204.4 MHz	32	23	209.4 MHz	33	16	214.4 MHz	34	9	219.4 MHz
31	31	204.6 MHz	32	24	209.6 MHz	33	17	214.6 MHz	34	10	219.6 MHz
32	0	204.8 MHz	32	25	209.8 MHz	33	18	214.8 MHz	34	11	219.8 MHz
									34	12	220.0 MHz

Front-Panel Registers

See Table 6-15.

Table 6-15
FRONT-PANEL REGISTERS
Writing Data to Shift Registers for Lights (74)
DB3=1 — initializes encoder at power up

Write Number	DB7	DB6	DB5	DB4	DB2	DB1	DB0
A	not used	not used	ΔF	SPAN/DIV	UNCAL	EXT	SAVE A
B	not used	not used	COUNT	MAX SPAN	AUTO RES	INT	VIEW A
C	THRESHOLD	not used	FREQ START/STOP		MIN NOISE	FREE RUN	VIEW B
D	BANDWIDTH	not used	not used	SHIFT	FREQUENCY	SINGLE SWEEP	B–SAVE A
E	SIGNAL TRACK	not used	READOUT	not used	2 DB/DIV	LINE	NARROW
F	not used	not used	BASELINE CLIP	ADDRESSED	10 DB/DIV	READY	WIDE
G	PULSE STRETCH	not used	Δ MKR	REF LVL	RESET TO LOCAL	FINE	LIN
H	PLOT	not used	not used	MAX HOLD	ZERO SPAN	GRAT ILLUM	TUNE CF/MKR

TAPE DATA TRANSFER PROGRAM

CAUTION

Macros stored in battery-backed up memory cannot be down-loaded to tape. Consequently, the macros will be lost each time the battery is removed from the Memory board.

If the battery on the Memory board is removed while the board is not powered up, data stored in battery-backed up memory will be lost. A Tektronix 4041-Series Computer, connected to the spectrum analyzer via the GPIB, will move this data to a tape and back into memory using the following program.

```
100  Integer a1,s1,t1,w1,i,v,y,z,v1
110  Print "Spectrum Analyzer Address is: ";
120  Input a1
130  Print
140  Print #a1:"RQS OFF"
150  Print "Save memory on tape? ";
160  Input b$
170  B$=seg$(b$,1,1)
180  If b$="y" or b$="Y" then goto 2000
190  Print
200  Goto 1000

1000 ! This routine moves data from TAPE to the SPECTRUM ANALYZER
1010 Print "Displays and Settings are on the following data files"
1020 Print "(3060 x 9 for displays, 1020 x 10 for settings)"
1030 Print
1040 Dir
1050 Print
1060 Print "Enter number of first data file 'FIL' :";
1070 Input t1
1080 Gosub 9000
1090 Print "Write over all Displays and Settings (0),"
1100 Print "Or write only in blank ..... memory (1):";
1110 Input y$
1120 If y$="0" or y$="1" then goto 1150
1130 Print """0"" or ""1"", Please: ";
1140 Goto 1110
1150 Y=val(y$)
1160 Delete var i$
1170 Dim i$ 700
1180 Print #a1:"SET?"
1190 Input #a1:i$
1200 W1=0
1210 Print #a1:"BVIEW OFF"
1220 Print
1230 Print
1240 For i=1 to 9
1250   Gosub 8000
1260   Gosub 6000
1270   If z=0 then goto 1300
1280   Print w1;"= Waveform from Data File FIL";t1
1290   Goto 1310
1300   Print w1;"= ..... not written. FIL";t1;"  not used."
1310   W1=w1+1
```

```
1320   T1=t1+1
1330   Next i
1340 S1=0
1350 Print
1360 Print
1370 Print
1380 For i=1 to 10
1390   Gosub 5000
1400   If z=0 then goto 1430
1410   Print s1;"= Settings from Data File ";t1
1420   Goto 1440
1430   Print s1;"= ..... not written. FIL";T1;"  not used"
1440   S1=s1+1
1450   T1=t1+1
1460   Next i
1470 Print #a1:i$
1480 Print
1490 Print
1500 Print
1530 Print
1540 Print "*** FINISHED ***"
1550 Goto 10000

2000 ! This routine moves data from the SPECTRUM ANALYZER to TAPE
2010 Delete var i$
2020 Dim i$ to 700
2030 Print #a1:"SET?"
2040 Input #a1:i$
2050 Dir
2060 Print
2070 Print "WARNING! This could overwrite existing files!"
2080 Print "Enter the Number of the last tape file: ";
2090 Input t1
2100 Gosub 9000
2110 Print
2120 Print
2130 Print #a1:"BVIEW OFF"
2140 W1=0
2150 For i=1 to 9
2160   Gosub 3000
2170   Gosub 7000
2180   If z=0 then goto 2210
2190   Print w1;"= Waveform sent to File FIL";t1
2200   Goto 2220
2210   Print w1;"= ..... skipped over. FIL";t1;" is empty"
2220   W1=w1+1
2230   T1=t1+1
2240   Next i
2250 Print #a1:i$
2260 ! Settings are sent to tape
2270 S1=0
2280 Print
2290 Print
2300 Print
2310 For i=1 to 10
2320   Gosub 4000
2330   If z=0 then goto 2360
2340   Print s1;"= Settings sent to File FIL";t1
2350   Goto 2370
2360   Print s1;"= ..... skipped over. FIL";t1;" is empty."
```

```
2370   S1=s1+1
2380   T1=t1+1
2390   Next i
2400 Print #a1:i$
2410 Print
2420 Print
2430 Print "*** FINISHED ***"
2440 Goto 10000
3000 ! Acquire Waveform and Settings.
3010 ! X9 is 500 point waveform, l$ is lower readout,
3020 ! m$ is upper readout, and e$ is an error message
3030 Delete var e$,h$,l$,m$,x9
3040 Z=0
3050 Dim h$ to 1100
3060 Integer x9 (1000)
3070 Dim l$ to 50,m$ to 50
3080 Print #a1:"SAVEA OFF;DRECAL A:",w1
3090 Print #a1:"ERR?"
3100 Input #a1:e$
3110 E$=seg(e$,5,2)
3120 If e$<>"62" then goto 3180
3130 V=0
3140 X9=0
3150 M$=""
3160 L$=""
3170 Goto 3280
3180 V=1
3190 Print #a1:"UPRDO?"
3200 Input #a1:m$
3210 Print #a1:"LORDO?"
3220 Input #a1:l$
3230 M$=seg$(m$,8,40)
3240 L$=seg$(l$,8,40)
3250 Print #a1:"WFM WFID:A,ENCDG:BIN;CURVE?"
3260 Input using "fa,+8%" dels "," #a1:h$,x9
3270 Z=1
3280 Return

4000 ! Remove memory settings (S$) from SPECTRUM ANALYZER
4010 Z=0
4020 Delete var s$
4030 Dim s$ to 700
4040 Print #a1:"RECALL ";s1
4050 Print #a1:"ERR?"
4060 Input #a1:e$
4070 E$=seg$(e$,5,2)
4080 If e$<>"62" then goto 4120
4090 V1=0
4100 S$="NULL"
4110 Goto 4170
4120 Print #a1:"SET?"
4130 Input #a1:s$
4140 Print #a1:"RQS OFF"
4150 V1=1
4160 Z=1
4170 Open #100:"FIL"&str$(t1)&"(OPE=REP,SIZ=1020)"
4180 Print #100:v1,s$
4190 Close 100
4200 Return
```

```
5000 ! Retrieve taped Settings (S$) and send to memory locations (S1)
5010 Z=0
5020 Delete var s$
5030 Dim s$ to 640
5040 Open #100:"FIL"&str$(t1)&"(ope=old)"
5050 Input #100:v1,s$
5060 If v1=0 then goto 5150
5070 If y=0 then goto 5120
5080 Print #a1:"RECALL ";s1;";RQS OFF;WAIT;ERR?"
5090 Input #a1:e$
5100 E$=seg(e$,5,2)
5110 If e$<>"62" then goto 5150
5120 Print #a1:s$
5130 Print #a1:"STORE ";s1;";RQS OFF"
5140 Z=1
5150 Close 100
5160 Return

6000 ! Send waveform (X9) & readouts (M$,L$) to memory location (W1)
6010 Z=0
6020 If v=0 then goto 6180
6030 If y=0 then goto 6080
6040 Print #a1:"SAVEA OFF;DRECAL A:";w1;";ERR?"
6050 Input #a1:e$
6060 E$=seg$(e$,5,2)
6070 If e$<>"62" then goto 6180
6080 Print #a1:"WAIT;TRI?"
6090 Input #a1:h$
6100 Print #a1:"RDOUT '";m$;"'"
6110 Print #a1:"RDOUT '";l$;"'"
6120 Print #a1:"WFM WFID:A,ENCDG:BIN;SIG;SAVEA ON"
6130 Wbyte atn(mta,32+a1),x9,eoi
6140 Wbyte atn (unt,unl)
6150 Print #a1:"DSTORE A:",w1
6160 Print #a1:h$
6170 Z=1
6180 Return

7000 ! Store readouts (M$,L$), and waveforms (X9) on TAPE File (T1)
7010 Open #100:"FIL"&str$(t1)&"(OPE=REP,SIZ=3060)"
7020 M$=m$
7030 L$=l$
7040 Print #100:v
7050 Print #100:m$
7060 Print #100:l$
7070 Print #100:x9
7080 Close 100
7090 Return

8000 ! Retrieves readouts (M$, L$), and waveform (X9) from TAPE
8010 ! From selected TAPE File (T1)
8020 Open #100:"FIL"&str$(t1)&(ope=old)"
8030 Delete var x9,m$,l$
8040 Integer x9 (1000)
8050 Dim m$ to 50,l$ to 50
8060 Input #100:v
8070 Input #100:m$
8080 Input #100:l$
8090 Input #100:x9
8100 Close 100
```

```
8110 Return

9000 ! This routine shows the contents of Memory displays and settings
9010 Print "Display Memory"
9020 Print "--------------"
9030 Print #a1:"RQS OFF"
9040 Delete var s$
9050 Dim s$ to 660
9060 Print #a1:"SET?"
9070 Input #a1:s$
9080 W1=0
9090 For i=1 to 9
9100   Print #a1:"SAVEA:OFF;DRECAL A:";w1
9110   Print #a1:"ERR?"
9120   Input #a1:e$
9130   E$=seg$(e$,5,2)
9140   if e$="62" then goto 9170
9150   Print w1;"= Waveform"
9160   goto 9180
9170   Print w1;"= ....."
9180   W1=w1+1
9190   Next i
9200 ! NOTE: "RECALL" may recall a RQS-ON
9210 ! state, so this must be turned off again by RQS OFF
9220 Print
9230 Print "Settings Memory"
9240 Print "---------------"
9250 S1=0
9260 For i=1 to 10
9270   Print #a1:"RECALL ";s1;";RQS OFF;WAIT"
9280   Print #a1:"ERR?"
9290   Input #a1:e$
9300   E$=seg$(e$,5,2)
9310   If e$="62" then goto 9340
9320   Print s1;"= Settings"
9330   Goto 9350
9340   Print s1;"= ....."
9350   S1=s1+1
9360   Next i
9370 Print
9380 Print #a1:s$
9390 Return
10000 End
```

THEORY OF OPERATION

This section describes the spectrum analyzer circuitry. The section begins with a functional description of the major circuit blocks. This is followed by more detailed descriptions of the circuitry within each block.

While reading these descriptions, refer to the corresponding block or schematic diagram in Volume 2 of the Service Manual. (This manual is an optional accessory. Contact your local Field Office or Tektronix representative for more information). The description titles use the diagram names and numbers for easy reference.

The Functional Block diagram, located at the front of the Diagrams section in Volume 2, shows how the major sections in the instrument relate and the paths of most major signals. Block diagrams showing more detail of these main sections follow the Functional Block diagram. Circuit schematic diagrams follow the major block diagrams.

Adjacent to each schematic is a third level of block diagram, a circuit board parts location illustration, and cross-reference look-up tables. The third level block diagram shows the function of the components shown on the schematic. The parts location illustration and look-up tables aid in finding components on either the schematic or circuit board.

FUNCTIONAL DESCRIPTION

What It Does

The spectrum analyzer accepts an electrical signal as its input and displays the signal's power distribution as a function of frequency. The display of the input signal appears on the crt as a graph where the horizontal axis is frequency and the vertical axis is amplitude. The display can be plotted on a chart recorder or a GPIB-compatible plotter.

The instrument can be operated manually with front-panel controls, or remotely via the GPIB with an easy-to-use programming language.

How It Works

The Spectrum Analyzer operates as a swept, narrow-band receiver. The crt beam sweeps horizontally as a range of frequencies is spanned. When a frequency component of an input signal is detected, the beam is deflected vertically as a function of input power at that frequency. The center frequency or marker frequencies in each span are set by the CENTER/MARKER FREQUENCY control or FREQUENCY entry via DATA ENTRY pushbuttons. The frequency range of each span is set by the FREQ SPAN/DIV control or pushbutton entry. The power reference level, represented by the top of the screen, is set by either the REFERENCE LEVEL control or the Data Entry keyboard.

First, Second, and Third Converters

Swept-frequency analysis is achieved by a triple-conversion, superheterodyne technique. Each of the three frequency converters consists of a mixer, a local oscillator, and appropriate filters. Only one frequency is converted in each mixer to pass through band-pass filters to the detector. This frequency can be changed by tuning the local oscillator frequency in the first or second converters. The third converter uses the fixed 100 MHz calibrator signal as a stable local oscillator.

The first converter, usually referred to as the front end, converts the input signal frequency to an intermediate frequency (IF) of 2072 MHz. The first mixer converts signals over the input range of 100 Hz to 1.8 GHz. (The first local oscillator phase locks in narrow frequency sweep spans to provide a stable display.)

The second converter down-converts the signal from 2072 MHz to 110 MHz.

The third converter amplifies the 110 MHz IF signal and converts it to the final intermediate frequency of 10 MHz. The third converter passes the signal to the main IF section for processing and detection.

IF Section

This section processes the signal for frequency resolution. Several functions are performed here: bandwidth filtering, amplitude calibration and logarithmic conversion, and signal detection.

The 10 MHz IF signal is processed through one of several band-pass filters selected by the RESOLUTION BANDWIDTH control. In the auto mode the microcomputer will select the best combination of bandwidth and sweep time for the selected span, unless overridden by the operator.

Weak signals can be amplified by a set of switchable amplifiers so the dynamic display range (vertical window) is shifted up or down. The REFERENCE LEVEL control selects the gain and input RF attenuation to frame this window between the reference level at the top of the display screen and the bottom of the display. A leveling circuit helps provide flat frequency response across the range. The signal is amplified by a logarithmic amplifier to produce the vertical signal calibrated in dB/div.

The detector produces a voltage that corresponds to the input signal strength in decibels. The detector output is then sent to the vertical channel of the display section to drive the vertical axis of the crt and display the signal.

Display Section

The display section draws the signal on the crt screen. Vertical deflection of the beam (Y axis) is increased as the output of the amplitude detector increases. The horizontal position (X axis) of a signal is controlled by the frequency control section and corresponds to the frequency of the detected signal. The Z axis, or brightness, is controlled by the INTENSITY control and the Z axis blanking circuits. (However, marker brightness is actually controlled by stopping the digital storage sweep for a period of time to brighten the spot.)

As the spectrum analyzer spans from low to high frequencies the beam sweeps from left to right. When the spectrum analyzer tunes through a signal frequency, a vertical deflection shows the strength of the signal. The result is a signal displayed at a position on the span that corresponds to its frequency, or in other words, the display shows amplitude as a function of frequency.

The video amplifier scales the detector output for vertical deflection in dB/div or performs a log/linear conversion, depending on the vertical display mode. The video processor provides additional bandwidth filtering if either the wide or narrow filter is selected.

The display section also provides crt readout to show control settings and measurement data. This readout is based on data from the microcomputer which is reading the settings of the front panel controls or data on the instrument and GPIB buses.

Digital storage circuits provide two functions; they provide a flicker-free display at slow sweep rates, and they store the display for later viewing. Up to nine different displays with their readouts can be stored in the battery-powered memory. The stored display data can then be transmitted through the IEEE-488 port to a plotter, or to GPIB compatible controllers or instruments.

Frequency Control Section

The spectrum analyzer sweeps through a frequency range that is set by the frequency control section. The CENTER/MARKER FREQUENCY control sets the frequency the 1st and 2nd local oscillators.

The output of a sweep generator is scaled by a span attenuator to sweep a range or span of frequencies. The output of the span attenuator drives the 1st LO for wide spans and the 2nd LO for narrow spans. The output sweep also deflects the crt beam across the horizontal axis as the local oscillators are swept so the display is a spectrum of power versus frequency.

Counter and Phase Lock Section

The Counter, Harmonic Mixer, and Auxiliary Synthesizer form the nucleus of the frequency control hardware. Both the 1st LO and 2nd LO frequencies are controlled via the firmware-based control loop. Data from the Counter is used as feedback to control the oscillator frequency. In Option 05 instruments, accurate signal frequency measurement is also possible by counting the frequency of the 3rd IF.

The Phase Lock system stabilizes the 1st LO frequency. This minimizes display jitter and increases resolution.

Digital Control Section

Operational modes and internal functions of the spectrum analyzer are selected and controlled directly from the front panel. The modes and functions that are selected are processed and activated by the instrument master microcomputer which talks and listens to all circuits over the instrument bus. The instrument can also be remotely controlled from an external controller through the IEEE-488 (GPIB) connector. This connector interfaces to the instrument microcomputer through the GPIB.

Front panel control and selector data is processed by a front panel CPU that interfaces with the master microcomputer over the instrument bus. The master microcomputer receives and sends all of its information over the instrument bus to the internal circuits. It can communicate with other instruments through the GPIB connector. The programmable control language corresponds to front-panel controls.

Power Supply Section

The power supply section provides regulated dc power and forced air cooling for all circuits within the instrument. The switching supply is capable of providing regulated voltages over a wide range of input line frequencies and voltages. The cooling system consists of an intake on the bottom of the case, air passages within the instrument, a fan, and a rear panel exhaust. Air is routed to all sections of the instrument in proportion to the heat generated by circuits within those sections. Internal temperature variations are minimized to provide reliable operation.

Other Sections

Interconnections between assemblies are made through a common Mother board. Most circuit board assemblies plug into the top side of the Mother board. Assemblies on the RF deck are connected to the bottom side of the Mother board through cables and connectors.

DETAILED DESCRIPTION

The following description is arranged by sections or systems (such as 1st Converter, 2nd Converter, etc.) followed by analysis of the circuits within that section. Each system or section is introduced with a description of the system using the section block diagram found in the Diagrams section of the Service Manual, Volume 2. This is followed by a description of each circuit board or major circuit within the system. The appropriate block or schematic diagram number is included in the text headings for each section or part.

1ST CONVERTER SECTION (Diagram 2)

The 1st Converter signal path consists of:

- 0-60 dB Step Attenuator
- 1.8 GHz Low-Pass Filter
- 1st Mixer
- 2.072 GHz Directional Filter
- 4.5 GHz Low-Pass Filter
- 1st Local Oscillator (LO)
- Power Divider
- Phase Gate Detector

Other circuits that control or drive the assemblies within the 1st Converter are the 1st LO Driver, the Counter and Phase Lock system, and the RF Interface circuits.

The 1st Converter converts the incoming RF signals to the 1st IF. Input signals are applied through Step Attenuator, 1.8 GHz Low-Pass Filter, and 2072 MHz Directional Filter to the 1st Mixer.

The RF Step Attenuator limits the input power to the analyzer. It provides 0 dB to 60 dB of attenuation in 10 dB steps. The 1.8 GHz low-pass filter attenuates out-of-band signals, preventing them from reaching the mixer input and creating unwanted images. A 3 dB pad matches the mixer impedance and protects the mixer diodes from spurious or static discharges. The four-port directional filter passes the input signal to the 1st Mixer and couples the 1st IF to the 2nd Converter.

The RF signals mix with the output from a tunable local oscillator (LO). The directional filter picks the 2072 MHz product present at the mixer RF input port (the unused mixer port is terminated). The 2072 MHz IF is applied through a 4.5 GHz Low-Pass Filter to the 2nd Converter. This further reduces any unwanted mixer products or out-of-band input signals.

The 1st LO is a voltage-controlled Yttrium-Iron-Garnet (YIG) oscillator that provides a tunable signal for the 1st mixer. The phaselock system is activated when spans of 200 kHz/division or less are selected (50 kHz or less in the Sideband Analyzer mode). The Power Divider splits the LO signal to apply it to the 1st mixer and to the Phase Gate Detector. The Phase Gate Detector compares the phase of the 1st LO to the strobe signal of the 1st LO phaselock system.

RF Interface Circuits (Diagram 25)

The RF interface circuits receive instruction from the microcomputer and produce control signals for the RF Attenuator (and Transfer Switch S13 for Option 07). These RF control circuits are located on the Z-Axis/RF Interface board (A70). Their operation is described as part of the Display section.

1st Converter (Diagram 11)

RF Input

The 50Ω RF INPUT connector accepts the input signals. Option 07 instruments also have a 75Ω input. In those instruments, Transfer Switch S13 selects between the 50Ω and 75Ω inputs.

The RF input signal goes through a 0-60 dB Step Attenuator (AT10) consisting of relay-controlled 10 dB, 20 dB, and 30 dB sections. The relays are actuated by control signals from the RF Interface circuit. The signal flows from the step attenuator to the 1st mixer through a low-pass filter, a pad, and a directional filter. The 1.8 GHz Low-Pass Filter (FL10) strips the incoming signal of any frequency components above 1.8 GHz and passes all frequency components below 1.8 GHz. The 3 dB pad matches impedances and helps protect the mixer diodes.

Directional Filter

The Directional Filter (FL16) couples the 2072 MHz signal to the 2nd Converter via low-pass and band-pass filters FL11 and FL14. As mixing products pass through FL16, they induce a selected current into a one-wavelength distributed ring, which couples the 2072 MHz IF signal out to the low-pass filter FL11. The remainder of the mixing products pass on through since the ring is excited only with 2072 MHz signals. The bandwidth of this Directional Filter is approximately 45 MHz. The unfiltered signals are passed on to the Diplexer.

2072 MHz IF Filters

The 2072 MHz signal, from the Directional Filter, passes through a 4.5 GHz Low-Pass Filter (FL11). The signal is then sent through a 2072 GHz band-pass filter (FL14) which rejects mixing products either side of a 15 MHz bandwidth centered on the 2072 MHz IF.

1st Mixer

The 1st Mixer receives the RF signal through the Directional Filter and the 1st LO signal through the Power Divider. These signals combine to produce mixing products that are filtered to yield the 2072 MHz IF signal. The mixer is a single balanced design, which has a lower conversion loss than unbalanced mixers. The local oscillator input is split through a broadband multi-section coupler, whose outputs are equal in power but 90° out of phase. An additional 90° phase shift is cascaded with the appropriate signal to create a 180° phase difference that is applied across a pair of series-connected Schottky diodes. The result is that the diodes are alternately switched on and off at the local oscillator frequency.

The node between the two diodes is isolated from the 1st LO input by about 30 dB so the RF input is applied to this node. The 2072 MHz IF output is also taken from this node as one of the mixer products. The 50 Ω termination on P124 provides a dc path and terminates the unused mixer port.

Excluding losses in the IF filtering circuitry, the fundamental conversion loss of the 1st Mixer is about 14 dB. The Schottky diodes are mounted in a mixer sub-assembly (A12A1) so that they can be easily replaced. However, the diodes are extremely sensitive to static charges. See the Maintenance section before attempting removal or replacement.

1st Local Oscillator

The 1st LO (A16) is a YIG (Yttrium-Iron-Garnet) oscillator that has a tuning range of 2.072 to 3.872 GHz. The oscillator assembly includes the interface circuit board that couples operating and tuning voltages from the 1st LO Driver, Span Attenuator, and Error Amplifier circuits to the oscillator.

The +15 V_1 voltage provides operating bias for the oscillator. The supply is protected and decoupled by VR1010, C1016, and L1011. VR1018 and VR1019 clamp transient voltages, preventing damage to the tune voltage coil and the driving circuits.

When the FM coil is used to sweep the oscillator, relay K1015 closes and couples C1012 and C1014 across the tune coil. The capacitors lower the noise bandwidth of the main coil driving circuit while the FM coil is in operation. The heater provides temperature stability by keeping the YIG sphere at a constant temperature.

The second supply, +15 V_2, is not used in this instrument.

Power Divider

The Power Divider (A13) splits the output of the 1st LO (YIG oscillator) to isolate the 1st Mixer from the 1st LO OUTPUT front-panel connector. Basically, the Power Divider is two multi-section directional couplers that are cascaded to produce two ports having equal power. The isolation between output ports is 15 dB or more at the operating frequency. The Power Divider also provides an improved load to the local oscillator.

2ND CONVERTER SECTION (Diagram 2)

The 2nd Converter mixes the 2072 MHz from the 1st Converter with the output of a 2182 MHz phase-locked 2nd local oscillator (LO). The 2072 MHz IF signal passes through a four-cavity band-pass filter (FL14) to prevent other signals, generated within the 2nd Converter, from getting back to the 1st Converter. A diode mixer combines the 2072 MHz IF input and the local oscillator signal to generate the 110 MHz IF output, which then passes through a 110 MHz low-pass filter to reject any higher order signals from the mixer.

2ND CONVERTER (Diagram 11)

The 2nd Converter converts the 2072 MHz signal output from the 1st Converter to 110 MHz for eventual application to the 3rd Converter. The assembly consists of a four-cavity filter connected to a narrow-band mixer through an external cable, a 110 MHz low-pass filter, and a mixer-biasing circuit.

Four-Cavity Filter

The four-cavity filter (FL14) is a low-loss narrow-band filter that only passes the 2072 MHz IF signal to the mixer. Any other frequencies are reflected back to the 1st Converter and terminated. In addition, the filter prevents the converter LO and mixer products from entering the 1st Converter.

This filter has a 1 dB bandwidth of 15 MHz and an insertion loss of 1.2 dB. Each end resonator is capacity coupled to external circuits through a coupling hat. Intercavity coupling is provided by coupling loops that protrude from the machined filter top. The resonant frequency of each cavity is determined primarily by the depth of a gap in the underside of the filter top, and is fine tuned with a tuning screw on the side of each cavity. When properly tuned, using a network analyzer, the filter return loss is greater than 25 dB from either end. Figure 7-1 shows a cross sectional view of the filter and Figure 7-2 shows the equivalent electrical circuit.

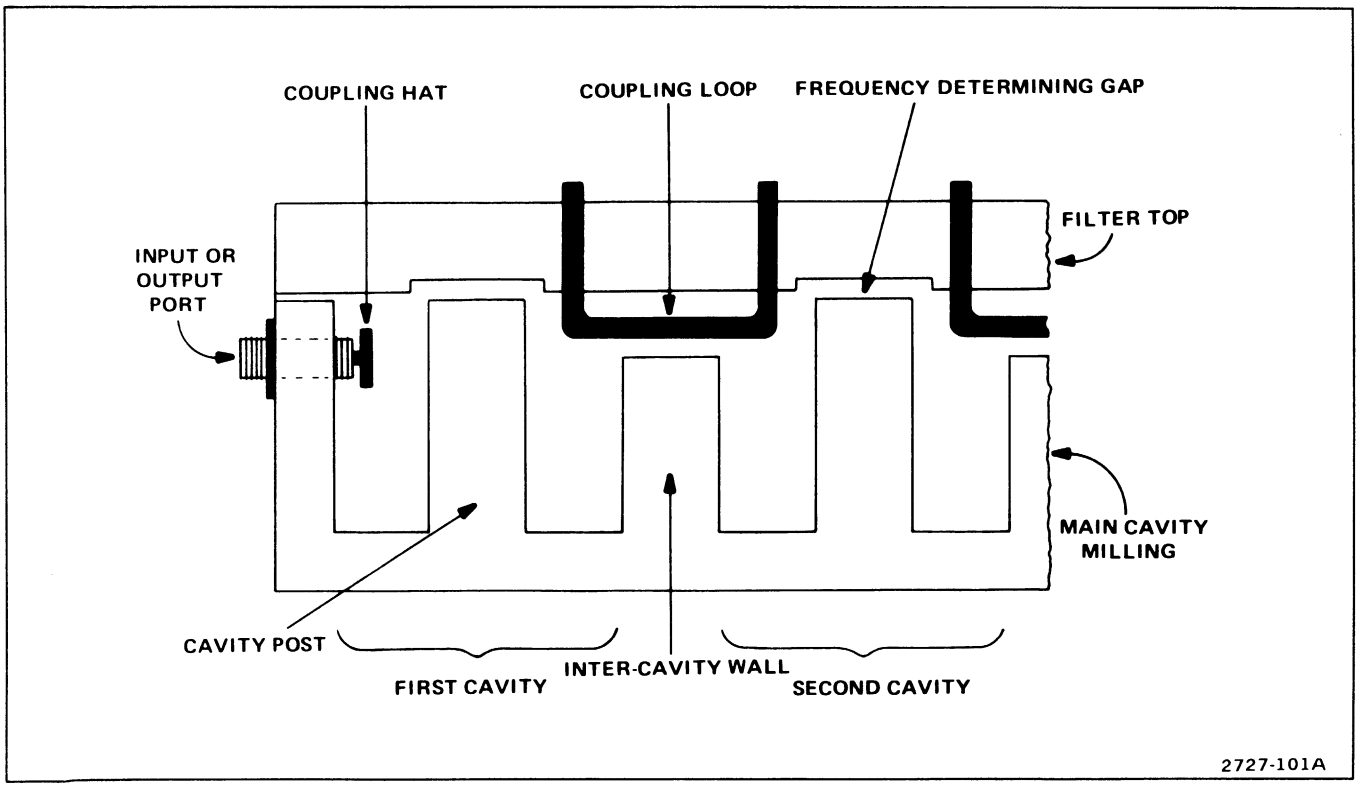


Figure 7-1. Cross section of a four-cavity filter.

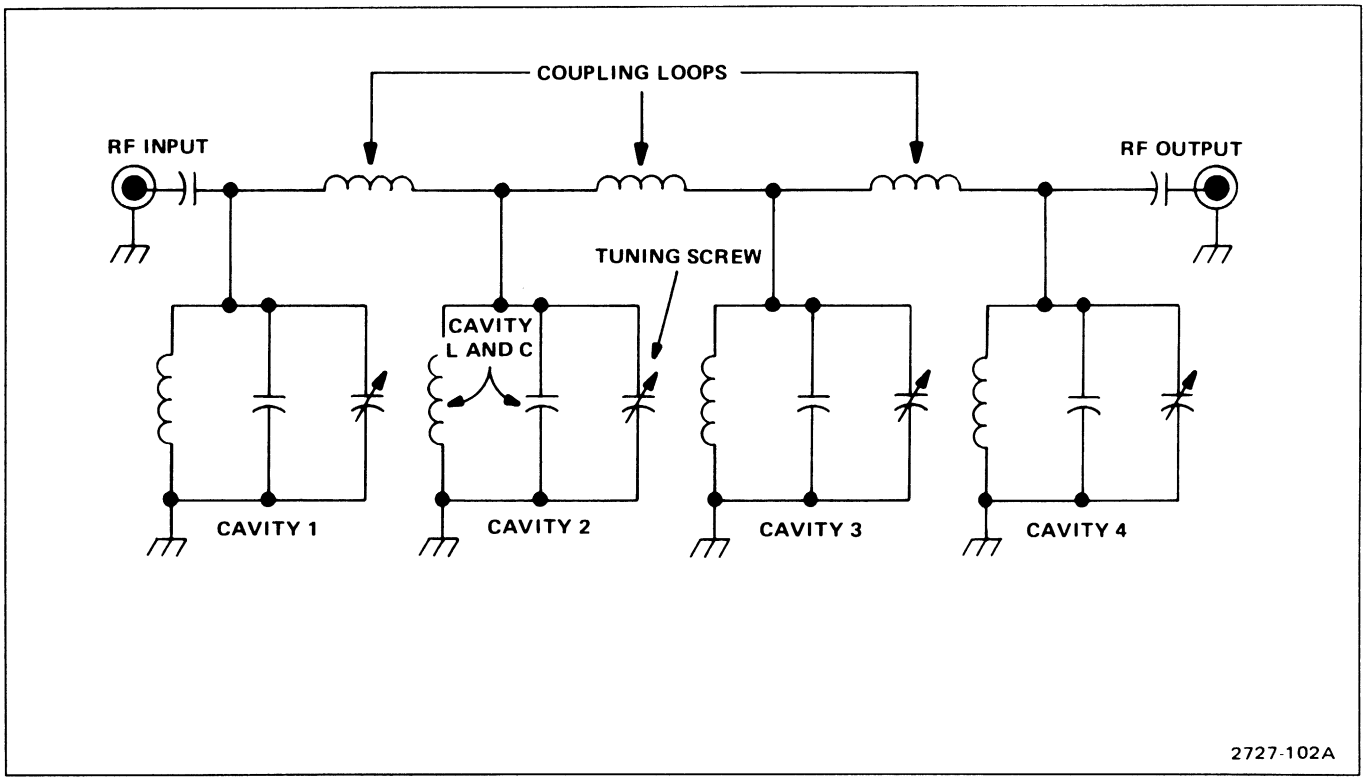


Figure 7-2. Equivalent circuit of the four-cavity filter.

Mixer Circuit

The mixer circuit consists of a single-balanced mixer, a mixer bias circuit, a delay line, and a 110 MHz low-pass filter.

The 2072 MHz signal from the four-cavity filter (FL14) enters the mixer, where it is switched on and off at a 2182 MHz rate by the the two mixer diodes. Both mixer diodes are turned on and off by the 2182 MHz 2nd LO signal. The difference frequency of 110 MHz is separated from the other mixer products by a low-pass filter for use as the IF output. Although the diodes are connected for opposite polarity, both are turned on at the same time because of the 180 degree phase shift delay line in the input path to one of the diodes. Note that the diodes are matched and must be replaced as a pair if one fails.

At the output of the mixer, two inductors, one capacitor, and printed circuit elements form a low-pass filter that passes the 110 MHz signal to the 110 MHz IF Amplifier. Dc-blocking capacitors at the three inputs to the mixer keep the diode bias from being applied to the RF and local oscillator lines.

The bias circuit establishes the bias for the mixer diodes. Each diode has approximately 2 mA of forward bias. The IF SELECT line from the Z Axis/RF Interface circuits (applied through feedthrough capacitor C182) is low. This causes the output from comparator U1014A to be at +14 V and the output from U1014B to be −14 V. Diodes CR1014 and CR1018 are thereby reverse-biased. Thus, the series resistances of potentiometer R1019 plus resistor R1014, and potentiometer R1010 plus resistor R1017, provide forward bias to the diodes. The potentiometers are set to balance the bias levels. The comparator switching capability is for use in other instruments with another 2nd Converter to select.

Precision External Cables

The external cable that connects the four-cavity filter output to the mixer RF input (W140) and the external cable that connects the 2nd LO to the mixer LO input (W222) are both critical length cables.

Filter to Mixer RF Input Cable. Several products and harmonics of the local oscillator and RF input frequencies will exit the mixer via the RF input port of the

mixer. The image (RF input minus the 2nd LO) and the sum (RF input plus the 2nd LO) are two significant products. There is enough energy in these two signals to warrant efforts to recover that energy.

Only the RF signal at 2072 MHz can pass through the four-cavity filter. Thus, any other signal frequency that is applied to the filter (that is, signals exiting the mixer via the RF port) is reflected back to the mixer by the filter. If the cable between the filter and the mixer is the correct length, the most significant reflected signals (i.e., the image and the sum) can be returned to the mixer in phase and converted into additional energy at the intermediate frequency. This technique is called "image enhancement mixing" and typically improves conversion loss by approximately 3 dB at the design frequencies.

The image frequency, in this instance, is very near the RF frequency. A very sharp cut-off filter is required to pass the RF, yet reflect the image. The four-cavity filter performs this function.

2nd LO to Mixer LO Input Cable. The image and sum products are also present at the LO port of the mixer. These signals leave the mixer via the cable to the 2nd LO and are reflected back to the mixer by the LO .The oscillators resonator appears highly reflective to the image and sum signals because it is tuned to the LO frequency. Again, the length of the cable from the LO to the mixer LO port is adjusted so the image and sum signals are reflected back to the mixer, in the proper phase, for re-conversion to supply additional energy at the IF frequency.

2182 MHz PHASE LOCKED 2nd LO (Diagrams 12 and 13)

The 2182 MHz phase locked 2nd LO assembly contains a tunable microwave oscillator, frequency reference, and phase lock circuitry. A two-section housing contains the circuitry. Microwave circuitry is packaged within the machined aluminum portion of the housing. Low frequency phase lock circuitry is within the mu-metal compartment.

In the microwave or LO portion of the assembly, the 2182 MHz Microstrip Oscillator generates 2182 MHz for the 2nd converters and the 2nd LO internal reference circuitry. The 2200 MHz Reference circuit receives a 100 MHz drive signal from the 3rd converter crystal oscillator and produces 100 MHz harmonics. The 22nd harmonic or 2200 MHz is mixed with 2182 MHz from the microstrip oscillator in the 2200 MHz Reference Mixer circuit. The difference frequency of 18 MHz is then fed to the phase lock side of the module.

A phase/frequency detector, on the 16-20 MHz Phase Lock circuit board, compares the 18 MHz difference frequency with a signal from a linearized varactor tuned, 18 MHz voltage controlled oscillator. The detector output tunes the 2182 MHz Microstrip Oscillator such that the difference frequency exactly matches the frequency of the 18 MHz reference VCO.

Sweep and tune signals from the Span Attenuator and Center Frequency Control circuits tune the 18 MHz VCO. The output voltage from the phase/frequency detector forces the Microstrip Oscillator to tune the same amount.

2182 MHz Microstrip Oscillator (Diagram 13)

This oscillator consists of a printed 1/2 wavelength resonator driven by a common-emitter feedback amplifier (Q1021). The base of Q1021 is capacitively tapped into the resonator. The resonator serves as a tuned phase inverter and impedance transformer, connected between the base and collector of Q1021. Part of the base feedback capacitance is provided by a bendable tab (C1021). This allows fine adjustment of the total feedback. This feedback RF signal is detected, by the base- emitter junction of Q1021, to produce a change in bias voltage that is related to the amount of feedback. The base voltage can be monitored at TP1015 with a high impedance voltmeter without significantly disturbing the oscillator.

The dc collector voltage and current for Q1021 is regulated by an active feedback circuit containing transistor Q2021. Voltage at the junction of R2023 and L2023 is a function of Q1021 collector current. This voltage is sensed by Q2021, which alters the base current to Q1021 thereby regulating the collector current and maintaining +10 Vdc on the resonator. Decoupling and control of bias loop dynamics are provided by C2104. Resistor R2016 swamps the negative base resistance of Q1021 to provide stabilization. Resistor R2015 protects the base- emitter junction of Q1021 from excessive reverse bias in the event the +12 V supply fails.

The oscillator is tuned by varactor diode CR1028, connected to one end of the resonator. Decoupling for the varactor is provided by the low-pass elements in the tune line. Bendable tab C1022 can be used to fine tune the oscillator center frequency.

Three output taps are coupled to the resonator through printed capacitors under the resonator. One output supplies 2182 MHz through a 6 dB attenuator to the Harmonic Mixer in the 829 MHz 2nd Converter. The other two output taps couple LO power through 6 dB attenuators to buffer amplifiers Q1031 and Q1011. The amplifiers provide approximately +10 dBm to the 2072 MHz 2nd Converter and +8 dBm to the Reference Mixer.

Since the two buffers are nearly identical, only the 2nd Converter buffer is described. Gain is provided by Q1011. Printed elements provide input and output impedance matching. Out-of-band damping is provided by R1011 in series with a 1/4 wavelength shorted stub. Dc is blocked by C1014 and C1011. A 1/4 wavelength open stub is used at the output to reflect one of the 2nd Converter's image frequencies at 4254 MHz (the other buffer does not use nor need this stub). Collector bias for Q1011 is provided through R1012, L1011, the 1/4 wavelength shorted stub, and R1011. The 1/4 wavelength shorted stub is grounded through C2011 (C2011, C1013, and L1011 are also used for decoupling). Collector voltage is determined by divider R1013 and R2013; this controls the dc feedback to the collector-base junction of Q1011. The bias network is decoupled from the RF path by L1014. Diode CR2013 protects the base of Q1011 from excessive reverse bias if the +12 V supply fails.

2200 MHz Reference Board (Diagram 13)

This circuit generates harmonics of the 100 MHz input. The 22nd harmonic or 2200 MHz is used by the Reference Mixer. The input 100 MHz signal is applied through a matching network (consisting of L1034, L1025, C1036, C1029, and C1025) to a differential amplifier (Q1024 and Q2024). The emitters of this amplifier are ac coupled through C2026, reducing low frequency gain and ensuring balanced operation. A snap-off diode (CR2014) is driven by the amplifier, via transformer T2015, to generate multiple harmonics of the 100 MHz signal including the 2200 MHz reference. The output passes through a 3 dB attenuator, for isolation, to the Reference Mixer circuit.

2200 MHz Reference Mixer (Diagram 13)

Signals from the 2200 MHz Reference circuit are filtered by a printed 2200 MHz bandpass filter. Diodes CR1011 and CR1012 are the switching elements of a single-balanced mixer. The microstrip oscillator output is applied to CR1011 and through a 1/2 wavelength delay line to CR1012. The delay line shifts the oscillator signal 180 degrees so both diodes switch together. Mixing the 2200 MHz with the oscillator 2182 MHz signal produces the difference frequency of 18 MHz. This 18 MHz signal is fed through a 37 MHz low-pass filter to the 16-20 MHz phase lock circuit. The low-pass filter prevents unwanted products, such as 82 MHz (product of 2100 MHz and 2182 MHz), from passing into the phase lock circuit.

16-20 MHz Phaselock Board (Diagram 12)

This board contains regulated power supplies, a 16-20 MHz (18 MHz nominal) voltage controlled oscillator with linearizing circuitry, and a phase/frequency detector circuit. Its main function is control of the 2182 MHz Microstrip Oscillator. The entire circuit board is housed in a magnetic shield to reduce spurious effects of external ac fields. All power supply and control inputs enter the circuit board via feedthrough capacitors in the housing wall. All connections with the microwave circuitry are through feedthrough capacitors C2200 through C2204, in the floor of the housing.

The +15 V, −15 V, and +9 V supply inputs are re-regulated down to +12 V, −12 V, and +5.2 V by regulators using operational amplifiers. IC U2025 provides a stable −6.2 V reference that is filtered by R2018 and C2015 and amplified by U2016B to produce the −12 V supply. IC U2016B uses emitter-follower Q2024 to increase the current capability of the supply. Resistor R2013 ensures sufficient base drive, while collector resistor R2025 reduces power dissipation in Q2024. Diode CR2019 protects the base-emitter junction during power supply shutdown. Feedback resistors R2016 and R2017 set the gain of U2016B and control the −12 V, +12 V, and +5.2 V supply voltages.

The −12 V supply is applied to inverting amplifier U2016A to produce the +12 V supply, and inverting amplifier U1017 to produce the +5.2 V supply. The output circuitry for the +12 V and +5.2 V supplies are similar to the −12 V supply.

Differential amplifier U2072A accepts the 2nd LO sweep voltages. One input senses the sweep voltage while the other input senses the ground potential at the Sweep board. Sweep sensitivity is adjusted by selecting resistor R2070. In wide spans, the sweep signal passes through parallel resistors R2082 and R2083. In narrow spans, R2082 may be switched out by Q2084, which reduces the weep sensitivity by a factor of ten. When the TTL signal to Q2076 is high, Q2076 is turned off, R2086 holds the gate of Q2084 to −15 V, Q2084 is turned off, and R2082 is switched out. This reduces the sweep sensitivity. When the TTL signal is low, Q2076 saturates with the collector slightly above 0 V, Q2084 turns on, and full sweep sensitivity is restored.

Amplifier U2072B accepts the 2nd LO tune voltage. the Tune board senses the ground potential of the 16-20 MHz Phase Lock board and floats the tune voltage. Tune sensitivity is adjusted by selecting resistor R2072.

The sweep and tune signals combine at the summing node input of a non-linear shaping amplifier. The non-linearity of the shaping amplifier compensates for the non-linear tuning of the reference oscillator varactor to give a linear tuning characteristic from 16 to 20 MHz. The shaping function is produced by a resistor-diode array in the feedback loop of inverting amplifier U1073A.

All of the amplifier's feedback is through R1072 when the output swings to the negative limit. As the output voltage swings less negative, it sequentially passes the tap-point voltages of a series of voltage dividers connected between 0 V (the summing node at pin 12) and a negative reference set by Q1047. If the output becomes positive with respect to a given divider tap, a corresponding diode in U2059 forward biases and connects the output to the tap, which creates additional feedback through one leg of the divider to the summing node. This causes R2051, then R2052, then R2053 (as so on through R2056) to be connected in parallel with R1072 as the amplifier output becomes less negative. This progressively increases the feedback, which causes the gain of U1073A to decrease.

Another series of dividers connected between the amplifier's output and a negative voltage reference causes the diodes in U1059 to sequentially conduct as the output becomes more positive. Resistors R2060, then R2061, then R2062 (as so on through R2065) are sequentially added in parallel with the existing feedback. Soft diode turn-on characteristics and a large number of breakpoints result in smooth gain changes. The nonlinear amplifier's voltage-gain characteristic is controlled by the shaper reference voltage, which is set by R2049. Altering R2049 will make the breakpoints either closer together or further apart; in practice, this resistor is selected to correct the tolerance variations of the 18 MHz VCO varactor.

The forward drop of the shaper diodes gives U1073A an offset voltage. Temperature correction diodes CR1086, CR1087, and CR1088 correct this offset over a wide temperature range by summing a correction voltage through R1074. These diodes also compensate for the lack of series diode drop across R1072 and eliminate offsets at the summing input of U1073B. Selecting R1070 provides fine adjustment of the VCO's center frequency. IC U1073B is an inverting amplifier that increases the shaper output voltage swing to a level that can control the varactor of the 18 MHz VCO.

A differential amplifier with well-defined limiting characteristics is used for the 18 MHz VCO. Emitter degeneration is used to control loop gain. Transistors Q2096 and Q2087 form the differential pair of transistors, with the emitters coupled through C2091. Transformer T2092 provides ac feedback for the collector-base junction of Q2096 and also creates the majority of the resonator inductance. The total resonator inductance may be adjusted by trying different combinations of connections between taps on inductor T1091 and transformer T2092. These taps allow coarse adjustment of the VCO center frequency. The capacitor of the resonator is varactor CR1089. Capacitor C1088 completes the resonator ac path and acts as a dc block, which allows a bias voltage to be impressed on the varactor. Resistor R2092 and capacitor C2090 damp the Q2096 collector, which prevents high-frequency instability in the oscillator. Transistor Q2087 provides a buffered oscillator output.

A discrete two-stage amplifier provides an unsaturated voltage gain of approximately 43 dB for the 18 MHz signal from the 2200 MHz Reference Mixer board. Transistor Q1041 is the common-emitter first stage while Q1042 and Q1043 form the differential second stage. The differential stage limits the output swing to 0.8 V to prevent over- driving the following ECL circuitry. Dc bias is maintained by Q1041, which has dc collector-base feedback via R1046 and the R1043/R1048 voltage divider. Transistor Q1043 receives its base bias through R1042. Each transistor operates with 5 mA of quiescent current.

ECL line receivers U2041D and U2041B amplify and buffer the 18 MHz signals from the Reference Mixer and the VCO, respectively. These two signals are then applied to the phase/frequency detector for comparison.

A pair of ECL D-type flip-flops, U2031A and U2031B, comprise the phase/frequency detector. The flip-flops drive a common reset line with a wired-AND output. The clock input of U2031B is driven with the signal from the 18 MHz VCO, and the clock input of U2031A is driven with the signal from the 18 MHz signal from the Reference Mixer.

Both flip-flops are configured to reset together whenever both are set. If they are clocked with signals that exactly match in frequency and phase, then both flip-flops set simultaneously and then almost immediately reset. If the Reference Mixer signal has a slight phase lead, U2031A will remain set longer than U2031B. If the Reference Mixer signal has a slight phase lag, U2031B will set first and remain set the longest. The signal that has the phase lead will cause the associated flip-flop to be set a greater percentage of time than the lagging flip-flop. If there is a frequency difference between the two inputs, the flip-flop with the higher input frequency will be set more of the time than the other flip-flop. The ratio between the filtered output signals of the two flip-flops indicates whether the Reference Mixer signal leads, lags, or differs in frequency from the 18 MHz VCO signal.

The outputs of the flip-flops are low-pass filtered by C1031 and C1028 and applied to differential amplifier U1031. U1031 compares the outputs of the flip-flops and produces an output that controls the tuning of the 2182 MHz microstrip oscillator. The phase-lock loop bandwidth is controlled by R1026, C1029, R1027, and C1026. The gain slope breaks to −12 dB/octave for frequencies below 16 kHz. Resistors R1033 and R1034 divide and offset the output of U1031 so the tune voltage ranges between 0 and −12.5 V.

The output of divider R1033/R1034 is applied to the varactor of the 2182 MHz microstrip oscillator (2nd LO). This closes the phase-lock loop, tuning the 2nd LO so that it tracks the 18 MHz VCO. When the 18 MHz VCO is tuned, U1031 simultaneously tunes the microstrip oscillator an equal amount. Within the loop bandwidth, the 2nd LO performance is determined by the 18 MHz VCO instead of the microstrip oscillator, giving a significant improvement in frequency stability and reduction of phase noise.

3RD CONVERTER (Diagram 3)

The 110 MHz IF Amplifier (A32)and 3rd Converter (A34) down converts the 110 MHz output signal from the 2nd Converter to 10MHz for the Variable Resolution circuits. A 100 MHz crystal controlled oscillator provides the third LO signal. In Options 05 instruments, this oscillator is phase locked to either a precise internal 10 MHz reference or an external 1, 2, 5, or 10 MHz reference. The 100 MHz LO signal is applied to the mixer and is distributed through output amplifiers to many other circuits throughout the instrument as a reference signal. It is also available for external use at the front-panel CAL OUT connector.

The 110 MHz signal is amplified in a three-stage gain block and applied to a three-section band-pass filter. This filter uses helical resonators and has a nominal bandwidth of 1 MHz. From the band-pass filter, the signal is applied to the converter, which consists of a mixer, an oscillator, and various output amplifiers.

110 MHz IF AMPLIFIER (Diagram 13)

Initial gain for the analyzer is provided by the 110 MHz IF Amplifier. This gain compensates for conversion losses in the three mixers. Typical gain for the amplifier is 21 dB. The amplifier consists of three stages of amplification and an attenuator. The first two mixers in the RF system offer no high-frequency gain; therefore, it is important that this amplifier exhibit low noise characteristics. It must also be relatively free from third-order intermodulation distortion.

Signal input is applied through an impedance matching band-pass filter (L2044 and C1054) to a parallel tuned circuit. The signal is injected into the parallel-tuned circuit through a tap in the inductor and taken out at the high impedance side through variable capacitor C2047. Inductive input provides for conversion to high impedance within the tuned circuit; the extra capacitor on the output provides for conversion back to 50 ohms nominal. The primary tuning capacitor, C1054, adjusts the resonant point; the output capacitor, C2047, is adjusted in combination with C1054 for good impedance match at 110 MHz. This is done with a return loss bridge. The nominal return loss is 35 dB. The Q of the input filter is approximately 20.

From the input filter, the signal is applied to Q4053, which is the first stage of amplification. This is a broad-band feedback amplifier to provide good input and output impedance and controlled gain. All feedback is through reactive components (transformer T3054), not resistive components. Thus, the impedance and gain can be controlled without significant noise problems.

The second amplifier stage, Q4037, is essentially the same as the first, with only minor bias differences. Gain through each of these stages is approximately 9 dB. The output is applied through a 3 dB attenuator, to preserve the impedance figure, to the bridged "T" adjustable attenuator. The 3 dB attenuator consists of resistors R2039, R2038, and R2043.

From the 3 dB attenuator, the signal is capacitively coupled through C2037 to the adjustable attenuator. This attenuator uses two PIN diodes, CR3030 and CR1029, in the mode when the resistance to RF signal flow is controlled by the current through the diodes. Refer to Figure 7-3 to aid in understanding the following description.

If resistor R1 in Figure 7-3 were set to infinite resistance and resistor R2 were set to zero resistance, the RF signal path would be through R2 to ground, to produce infinite signal attenuation. If resistor R1 were set to zero resistance and resistor R2 were set to infinite resistance, the RF signal path would be through R1 to the load, to produce almost no attenuation. This, basically, is how the adjustable attenuator operates, except that resistors R1 and R2 are actually PIN diodes and the RF path resistance through these diodes is controlled by the current through the diodes in an inverse proportion (higher current results in less resistance to RF).

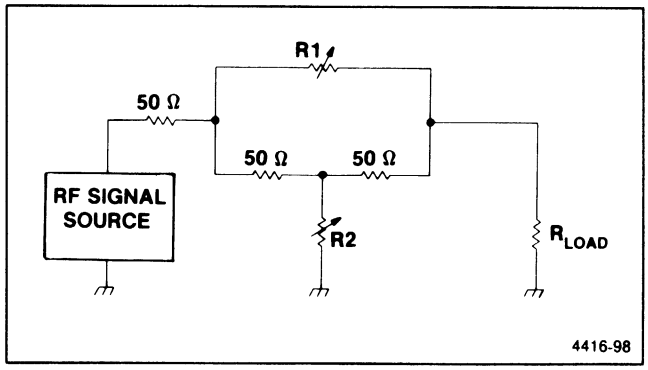


Figure 7-3. Bridged "T" attenuator equivalent circuit.

Resistors R3035 and R2030 on the detailed schematic diagram establish a constant current of approximately 2 mA from the 15 V supply to the diodes. This current is divided according to the bias on the diodes. The bias, in turn, is established by gain adjustment R1015, from the +15 V supply. If R1015 is set low (near ground), diode CR3030 is reverse biased and the 2 mA flows through diode CR1029. This routes the RF signal through resistors R2032 and R3029 and capacitor C2029, with the impedance characteristics of

CR1029 added for maximum attenuation.

If R1015 is set higher (nearer +15 V), diode CR3030 is forward biased and starts to conduct. Since the 2 mA supply current is relatively constant, this subtracts from the current through CR1029. Thus, the impedance of the diodes is relatively constant, which results in a good impedance match over a broad range. The RF signal path is determined by the exact amount of current through CR3030; part of the RF signal path is through CR3030 to the output amplifier and part is through R2032 and diode CR1029 to ground. This results in reduced signal attenuation.

If R1015 is set to the positive limit, the entire 2 mA flows through CR3030. This routes the RF signal through CR3030 (which exhibits little resistance with high current) to the output amplifier with almost no attenuation. (The insertion loss is approximately 1 dB.)

From the adjustable attenuator, the signal is applied to the final amplifier Q3018. This stage is a broad-band feedback amplifier that supplies relatively substantial output current and exhibits good intermodulation distortion performance. This is provided primarily through the large current capacity, by negative feedback through resistor R3014, and emitter degeneration through resistor R4029. These resistors are sized to provide a reasonably good impedance match at 110 MHz. Nominal gain of the stage is 13 dB.

With Gain potentiometer R1015 set for maximum gain (least attenuation), the gain of the 110 MHz IF Amplifier is approximately 26 dB to 27 dB. R1015 is normally adjusted for total gain of 21 dB.

The output signal from the 110 MHz IF Amplifier is applied through the 110 MHz band-pass filter, FL36, to the 3rd Converter.

110 MHz BAND-PASS FILTER (Diagram 14)

The 110 MHz band-pass filter is a three-section filter using helical resonators, which determine the widest resolution bandwidth of the analyzer. The filter provides image rejection to prevent the mixer from producing 10 MHz outputs from input signals of 90 MHz, and it also limits the noise spectrum that appears at the 10 MHz IF circuits to those frequencies at which signals also appear.

Though the filter is a sealed unit, in the interest of system understanding, the following brief description is provided.

The filter consists of three small encapsulated helical resonators that are tuned with multi-turn trimmer capacitors. For purposes of impedance matching, the filter is symmetrical. The end resonators are connected to external circuits by 10 pF capacitors attached to taps on the coils. Coupling between resonators is accomplished through holes in the resonator cans.

Adjustment of the filter for minimum attenuation is performed by setting the three trimmer capacitors. Insertion loss is approximately 4 dB to 4.5 dB. From the filter, the 110 MHz signal is applied to the 3rd Converter board.

3rd CONVERTER (Diagram 14)

The 3rd Converter consists of a 100 MHz crystal oscillator and a mixer. It outputs the 3rd IF of 10 MHz, for the Variable Resolution (VR) circuits, and a stable 100 MHz reference for other circuits within the instrument.

100 MHz Oscillator

A Colpitts oscillator is formed by Q2038, Y3038, L1041, C1038, and related components. Y3038 is a 100 MHz crystal that operates in a series resonant mode in the feedback loop of the oscillator. The oscillator output couples through C2042 to differential amplifier Q2042/Q2041. The two separate outputs of approximately 2 V peak-to-peak amplitude go to three hybrids (mixer U3051, distribution amplifier U3031, and calibrator U2022) on the 3rd Converter board.

In Option 05 instruments, P2042 is removed and L3041, varactor diode CR3039, and Y3038 form a series resonator that tunes the oscillator approximately ±1 kHz. The RPL VOLTS TUNE line varies from 0 V to +12 V, changing CR3039's capacitance to phase lock the oscillator to the Reference Lock source. RPL GND is tied to ground in the Reference Lock module.

Mixer

At mixer U3051, 100 MHz enters on pin 2 and is amplified to drive a ring diode mixer. 110 MHz enters on pin 10 and is mixed with the 100 MHz to yield mixing products at 10 MHz and 90 MHz. The 10 MHz signal passes through a low-pass filter and is sent to the Variable Resolution Input circuit, while the unwanted 90 MHz signal is terminated within the mixer.

Distribution Amplifier

U3031 distributes a 100 MHz signal to other modules in the instrument. The input level on pin 2 is typically 2 V peak-to-peak, while the output level is 0 dBm into a 50 ohm load.

Calibrator

U2022 and related components regulate a 100 MHz signal to −20dBm for the front-panel CAL OUT connector. VR1051 serves as an accurate 6.2 V reference, which is divided to approximately 1.2 V and applied to pin 6 of U2022. The exact level is set by R1041 the Cal Level adjustment.

The 100 MHz signal enters pin 1 and passes through a pin diode variable attenuator. The signal is then amplified and passed through a low-pass filter to remove any harmonics. The signal then enters a peak detector and comparator where the peak amplitude of the 100 MHz signal is compared to the 1.2 V reference on pin 6. An operational amplifier then adjusts the attenuation level of the pin diode to maintain a constant signal level. The output of this operational amplifier can be measured on TP3011. A small portion of the 100 MHz signal is attenuated through R2011 to -20 dBm. R1021 and R1022 supply bias current to the peak detector circuits. The voltage on pins 7 and 8 should typically be +5 V.

C2023, C2011, and related components form a high-pass filter to allow harmonics of 100 MHz to pass through to the front panel. The final result is a calibrator signal rich in harmonics with an accurate 100 MHz amplitude.

In Option 07 instruments, the CAL OUT signal goes through a set of relay switches. In 50Ω mode, the output goes straight to the CAL OUT connector. In the 75Ω mode, the output is routed through a 50Ω-to-75Ω matching pad and the output is +20 dBmV.

REFERENCE LOCK (Diagram 46) (Option 05 Only)

The Reference Lock module (A36) consists of a stable 10 MHz crystal oscillator (A36A3), reference detector, frequency synchronizer, phase/frequency detector, and tune window detector. Either the internal 10 MHz reference or an external 1,2,5, or 10 MHz reference frequency is routed through the reference detector to the frequency synchronizer. The local oscillator's 100 MHz output is divided by 100 and applied to one input of a phase/frequency detector which compares it with the 1 MHz reference frequency. The resultant error signal is amplified by the tune amplifier and applied, as a corrective voltage, to the voltage controlled 3rd LO.

External Reference Detector

Buffer amplifier Q2014 converts External Reference signals, within the range of −15 dBm to +15 dBm, into TTL compatible level. When an external signal,within the level range, is applied, it triggers multivibrator U2046B. The output of U2046B enables external signal control NAND gate U2032D, and disables the internal signal control gate U2032A. It also disables the internal 10 MHz reference oscillator by turning Q1031 on, which biases Q1033 off, and removes the +5 V_s supply for the oscillator. The output of U2046B, pin 9, is sent to the processor, on the EXT REF line, to indicate that an external reference frequency is in use. During a diagnostic test, the microprocessor can also pull the INTERNAL SHUT-DOWN line down to turn the Internal Reference Oscillator off and check for loop unlock. U2032B gates either the 10 MHz from the internal gate U2032A, or the external reference from U2032D, to the frequency synchronizer U2046A.

Frequency Synchronizer

Multivibrator U2046A, synchronizes its 1 MHz output with any of the allowed input frequencies by edge-triggering the time-out period. The 1 MHz output frequency is set by the timing components R2039,C2038, and adjustment R2042. With a 10 MHz signal applied to U2046A, adjustment R2042 is set for a 1μs period, with 65 ns between the falling edge at TP2046 and the next falling edge at TP1044.

Phase/Frequency Detector

The 100 MHz from the 3rd Local Oscillator is divided by 100 and converted to a TTL level by prescaler U2020. The 1 MHz from U2020, is fed to the clock input of D-type flip-flop U1044A. The 1 MHz from U2046A, is applied to the clock input of D-type flip-flop U1044B. The two flip-flops and NAND gate U2032C, form the Phase/Frequency Detector. R1034,R1035,and C1037, along with it's counterpart, on the output of U1044A, form a low-pass averaging filter for the outputs of the flip-flops. When the two input frequencies are equal and in phase, the composite output of the averaging filter is +2.5 V_{dc}.

Tune Amplifier

The FET-input operational amplifier (U1034) takes the output of the phase/frequency detector, amplifies the error and supplies an appropriate tune voltage to the 100 MHz voltage controlled oscillator. The tune amplifier, with feedback components C1031, C1038, R1028, and R1029, determine the loop transfer characteristics. The loop dc gain is very high which takes advantage of the high accuracy of the internal or external references. The loop ac gain (determined by C1031) rolls off very quickly so any phase noise, on an external reference signal, is not amplified.

Lock Detector

U1012 is used as a tune volts window detector. R1013, R1012, and R1011 set the upper threshold at 11 V_{dc}, and the lower threshold at 2 V_{dc}. As long as the tune volts stays within these limits, a high output tells the processor that the 3rd LO loop is locked. A low output from U1012, indicates that the reference oscillator frequency is beyond the 3rd LO's tune range. This REF LOCK status line, along with the other two processor interface lines, is routed through the Sweep board for processor interrupt generation. The processor reads the lines and displays their status on the crt readout.

IF SECTION (Diagram 4)

The IF section receives the 10 MHz IF signal from the 3rd Converter, establishes the system resolution, levels the gain across the frequency range, logarithmically amplifies the signal, and detects the signal to produce the video output to the Display section.

System bandwidth resolution is selectable from 1 MHz to 100 Hz in decade steps, plus 30 Hz. This selection is performed by the Variable Resolution circuits and is controlled over the instrument bus. Two sets of filters are used to establish the bandwidth. Band-pass filters are also included at the circuits input and output.

Significant gain is also provided by several stages of amplification within the Variable Resolution circuit block. Other gain steps are also provided by switching gain blocks in or out of the signal path. These gain blocks provide −10, +10, +20, or +30 dB of additional gain when switched in combination.

Logarithmic amplification of the signal is required to calibrate the graticule in dB/division. This is performed by a seven stage amplifier that produces an output proportional to the logarithm of the input. Thus, the screen displacement can be selectable for the amount of change per division, and can be proportional to the input level change. For example, in the 10 dB/div display mode, each division of displacement on the screen represents a signal level change of 10 dB regardless of whether it is at the top or bottom of the screen.

The detector follows the logarithmic amplifier to produce a positive-going output signal that is applied to the display section as the VIDEO signal.

Variable Resolution (Diagrams 15, 16, 17, and 18)

The Variable Resolution (VR) assembly (A68) establishes the resolution bandwidth and provides approximately 41 dB of system gain. The assembly consists of two sets of filters plus gain stages. Since the input to the VR circuits is nominally at −35 dBm and the Log Amplifier input requires +6 dBm for full screen, the VR circuits must provide the gain difference. The VR supplies 30 dB of additional gain and 10 dB of gain reduction for all vertical display modes.)

Physically, the VR assembly contains two sub-assemblies that connect together and plug onto the instrument Mother board. The input circuits are in one sub-assembly and the output circuits and digital interface are in the other. Each of the sub-assemblies consists of boards that plug onto a four-layer VR Mother board with a ground plane on both outside layers. Only power supply and control voltages travel through the VR Mother board. All signal connections are by coaxial cable.

VR Input (Diagram 16)

The VR Input circuit receives the −35 dBm 10 MHz signal from the 3rd Mixer through J693. This signal goes through a bandpass filter, an amplifier, and an output attenuator.

The filter augments the 1 MHz filter that precedes the 3rd Mixer. That 1 MHz filter provides initial selectivity. This filter has 1.2 MHz bandwidth and is a two-pole design. The filter includes C1037 and C1031 and all of the components between. Filter tuning is provided by variable capacitors C1033 and C1026 (Input Align).

Two-pole Bandpass filters like this, with a bandwidth over ten percent of the center frequency, tend to degenerate into either high-pass or low-pass filters. This filter design tends to degenerate into a high-pass filter. A complementary output filter in the Post VR amplifier degenerates into a low-pass filter. Together, the two filters provides the desired 1.2 MHz bandpass characteristic.

From the filter, the signal is applied to broadband feedback amplifier Q1023, which is biased for a large output current (approximately 50 mA) to reduce intermodulation distortion. This performance is provided primarily through the large current capacity by negative feedback through resistor R1025 and by emitter degeneration resistor R1023.

A 6 dB attenuator at the output of amplifier Q1023 provides a clean 50 ohm output to the 1st Filter Select circuit and reflects a 50 ohm termination back through the amplifier for proper termination of the 1.2 MHz band-pass filter. The output signal is sent through jumper B.

1st Filter Select (Diagram 16)

The 1st Filter Select circuit operates with the 2nd Filter Select circuit through banks of switched filters to set the overall system bandwidth. Data bits 0, 1, and 2 from the data bus are applied to decimal decoder IC U4035 (it provides a low signal on the appropriate output pin to enable the selected filter). Bandwidth selections are 1 MHz to 100 Hz in decade steps, and 30 Hz. The data bits select a bandwidth filter according to Table 7-1.

Table 7-1
BANDWIDTH SELECTION

Bandwidth	DB0	DB1	DB2
1 MHz	1	0	0
100 kHz	0	1	0
10 kHz	1	1	0
1 kHz	0	0	1
100 Hz	1	0	1
30 Hz	0	1	1

Filter selection is done by PIN diode switching. At the input and output of each filter are series and shunt diodes. When a filter is selected, the series diodes are biased on and the shunt diodes are biased off. For the filters that are not selected (only one can be selected at a time), the diode conditions are opposite. Since the switching operation is the same for all filters, the description for the 100 kHz filter selection is applicable to all filters.

With a content of 010 for the three data bits, line 2 from U4035 will be low. This turns on switching transistors Q3019 and Q3055. With input switch Q3019 turned on, the current path is through R4012, L3012, CR3010, L3013, R3014, and Q3019. This current is determined by decoupling resistor R3014 and resistor R4012. The voltage drop across R3014 and R4012 is enough to turn CR3010 on and reverse bias CR3012. The same case exists for the filter output switch, Q3055. Resistors R3057 and R1067 establish the current to forward bias CR3061 and reverse bias CR3060.

Thus the signal from the input circuit, via jumper B, is applied through the selected filter and transmitted to the 10 dB Gain Steps circuit via jumper K. Nominal loss through the filter circuit is approximately 6 dB, with slight variations among the filters. The 1st Filter Select output level is nominally −25 dBm.

In the non-selected filter sections, the input and output switch transistors are turned off by the high outputs from decimal decoder U4035. The collectors are pulled toward −15 V through the resistors that forward bias the shunt diodes in the input and output. Since one filter is always selected, the voltage drop across the common input and output resistors (R4012 and R1067, respectively) back biases the series diodes. The number 6 output from U4035 pin 7 is always high in this instrument. Therefore, Q1019 and Q1055 are never switched on. This circuit is intended to switch filters when used in other instruments where FL680 is a switchable filter.

A filter is not used in the 1 MHz section, because this circuit section is preceded by two filters that accomplish the required function; the first is the 1 MHz filter between the 2nd and 3rd Converters, the second is the 1.2 MHz filter in the input circuit. Instead of a filter, a 6 dB attenuator is contained in the 1 MHz selection circuit. This attenuator provides initial leveling to compensate for the loss when a filter is used.

The 100 kHz filter is a double-tuned LC circuit designed for a good time-domain response shape. The filter is tuned with composite variable capacitors consisting of small air variables paralleled with switched fixed capacitors. A third variable capacitor may be adjusted to establish the desired bandwidth. For Option 07 instruments, a similar 300 kHz filter replaces the 100 kHz filter.

The 10 kHz filter uses a pair of two-pole monolithic crystal filters that are interconnected by variable shunt capacitor C2037. Input and output impedances are matched with broadband transformers T3026 and T3055. A 3 dB attenuator consisting of R2027, R2026, and R2028 is included at the filter input.

The 1 kHz resolution filter consists of a single two-pole monolithic crystal filter, matched to the 50 ohm impedance with broadband transformers T2035 and T2055. A 2 dB attenuator consisting of R2024, R2023, and R2025 is also part of the filter.

The 100 Hz/30 Hz filter, FL680, is an electronically switched crystal filter mounted on the crt shield. It is matched with FL6015 on the 2nd Filter Select board, A68A8. The filter has a bandwidth of 100 Hz when its input and output ports are low (−15 V) and 30 Hz when high (+15 V). When 100 Hz is selected, output 5 (pin 6) of decoder U4035 is low. This turns transistor Q1020 on, forward biasing CR1010 and reverse biasing CR1011. This applies the IF signal to the filter input.

When output 6 (pin 7) of decoder U4035 is high, Q1019 and Q1055 are off. This applies −15 V to the input and output ports of the filter so that it is in the 100 Hz mode. When output 6 of U4035 is low, Q1019 and Q1020 are on in addition to Q1055 and Q4050. This provides forward bias for CR1010 and CR4064. At the same time, Q1019 and Q1055 are turned off, applying +15 V to the input and output ports, and switching the filter to the 30 Hz mode.

Diodes pairs CR1017-CR1021 and CR1018-CR1022 provide limiter and clamping action at the filter input to remove RF excursions when the dc potential at the filter input and output switches.

10 dB Gain Steps (Diagram 17)

The 10 dB Gain Steps circuit provides system gain, a 30 Hz gain adjustment, a 10 dB switchable gain step, and the front panel overall gain (AMPL CAL) control. The circuit consists of three stages of amplification. The nominal input signal level from the 1st Filter Select circuit is −25 dBm for a resolution bandwidth of 100 kHz. (All levels listed in this description relate to the 100 kHz resolution.)

The input signal is applied through impedance transformer T4019 to the first amplifier stage consisting of a differential pair, Q3016 and Q2027, driving emitter follower Q1036. The signal feeds back to the base of Q2027 through divider R2034 and R2031. Signal output resistor R2035 presents approximately 50 ohms output impedance to the next stage.

Gain of the input stage is the same for all resolution bandwidths except 30 Hz. When 30 Hz is selected, Q2015 connects the 30 Hz Level control (R2025) and R3029 across R2031.

The 1st stage output drives a common emitter stage (Q2043). Gain of this stage changes by +10 dB when Q4039 is switched on. Data bit 0 from the gain steps decoder circuit on the VR Mother board #2 (A68A2) controls this gain step. When the bit is high, emitter resistor R2048 sets the stage gain. When low, Q4039 saturates and shunts R2048 with R3038 and 10 dB Gain adjustment R3035. This increases the stage gain by 10 dB.

The output of Q2043 drives the input of the third amplifier stage. This stage operates the same as the first stage except the gain is adjustable by the front panel AMPL CAL screwdriver control. PIN diode CR1053 and resistor R1056 shunt resistor R1060 to control the gain of this stage. The AMPL CAL control biases CR1053. The amount of current through the diode determines its high-frequency resistance. As the current through the diode increases, the resistance decreases and the gain of the stage increases. Gain range is approximately 14 dB.

Output impedance of the stage is 50 ohms as set by resistor R1064. Nominal output level is −1 dBm for a full screen display. This level may be as high as +9 dBm when MIN NOISE is active. In the MIN NOISE mode, 10 dB of attenuation is removed from the instrument input step attenuator. VR Input signals are higher. Hence, 10 dB of gain is removed from the VR.

20 dB Gain Steps Circuit (Diagram 17)

This circuit provides gains of −8 dB, +2 dB, +12 dB, and +22 dB in precise 10 dB steps. The nominal −1 dBm input is supplied through pin P from the 10 dB Gain Steps circuit. This signal is applied to a chain of three amplifiers, each using emitter degeneration. A change of the emitter resistance changes the amplifier gain. The gain step decoder on the VR Mother board #2 supplies the switching signals that select the amplifier gain. These amplifiers are similar to the 10 dB Gain Step amplifier previously described. On this board, the first two amplifiers are cascaded for the 20 dB step and the third amplifier provides the additional 10 dB step.

The nominal gain of the complete circuit is −8 dB, with the gain steps switched off. This provides a nominal −9 dBm output. In this condition, control pins V and Y are high, biasing Q2018, Q2042, and Q1062 off.

For the 20 dB gain step, Q2018 and Q2042 turn on (pin V is low), increasing the gain of the first two amplifiers by 10 dB each, for a 20 dB gain step. Potentiometer R2023 (20 dB Gain) adjusts the first stage (Q1025) gain shift while the second stage (Q1035) gain shift is fixed at about +10 dB. The adjustment allows setting the gain step to exactly +20 dB.

For the 10 dB step, pin Y is low, saturating Q1062. This raises the gain of the third amplifier (Q1043) by 10 dB, as set by R2060.

Gain of the 20 dB and 10 dB gain step circuits is controlled by data bits 0, 1, and 2. Data is latched on the output of decoder U3017 on the VR Mother board #2. When the bits are high, transistor Q4035, Q3035, and Q4037 switch on. The resultant low out turns on the respective gain step circuit. Table 7-2 shows the state of bits 2, 1, and 0 and the gain shifts obtained.

The output signal from the 20 dB Gain Steps circuit is applied through a coaxial cable to the VR Band Leveling circuit.

Band Leveling Circuit (Diagram 17)

The two amplifiers in the VR Band Leveling circuit (A68A7) correct gain variations through the front end. Nominal signal input level for 100 kHz resolution in the Min Distortion mode is −9 dBm. The output level is about 0 dBm.

The two amplifier stages on this board are similar to the 10 dB gain steps circuits. A stage consists of a three-transistor circuit using a differential pair driving an emitter-follower. The gain is controlled by altering the feedback network.

The first stage (Q2015, Q2019, and Q1025) has a gain range of 13.5 dB by controlling the bias of PIN diode CR2021. Bias for this diode is controlled by a circuit on the VR Mother board #2 (A68A2).

The second stage (Q1031, Q1033, and Q1041) is similar, except the gain is not variable. (This board is also used in multi-band instruments where Q2046 can switch in an extra 12.5 dB of gain on bands requiring it.)

The output from this board is applied through connector EE to the 2nd Filter Select circuit.

Table 7-2
GAIN STEP COMBINATIONS

Gain Required	Data Bits			A68A5	A68A6	
	2	1	0	Pin N (10 dB)	Pin V (20 dB)	Pin Y (10 dB)
10 dB	0	0	1	0	1	1
20 dB	1	0	0	1	0	1
30 dB	1	0	1	0	0	1
40 dB	1	1	1	0	0	0

VR Mother Boards (Diagram 15)

The circuits on the VR Mother boards provide address and data decoding, band leveling control, and power supply and control signal interfacing to the other VR boards. The VR Mother board #1 (A68A1) provides decoupled power supplies and interface lines to the VR Input (A68A3), 1st Filter Select (A68A4), 10 dB Gain Steps (A68A5), and 20 dB Gain Steps (A68A6) boards.

The VR Mother board #2 provides address and data decoding and gain control for the Band Leveling circuit. (This assembly is also used in multi-band instruments, and so contains band identification and band leveling control circuits for bands not available in this instrument.) The VR Mother board #2 provides power supply voltages and control lines to the VR Mother board #1 (A68A1), Band Leveling (A68A7), 2nd Filter Select (A68A8), and the VR Post Amplifier (A68A9).

Address and data valid lines from the analyzer address bus are applied to address decoder U4022. Data bit 7 is applied to the decoder's select input A as a supplemental address bit. This bit selects either an address to latch data for the resolution bandwidth selection or an address to latch data for gain step selection and band identification.

Data latches U3010 and U3017 monitor the data bus at the selected address. Latch U3010 stores the filter select data that controls the 1st and 2nd Filter Select circuits.

U3017 latches the gain selection and band identification data. Latched data bits 0, 1, and 2 (output pins 2, 5, and 6) switch transistors Q4035, Q3035, and Q4037 to control the gain switching circuits in the 10 dB and 20 dB Gain Step circuits through VR Mother board #1.

The output on pins 15, 16, 19, and 12 of U3017 (corresponding to data bits 3, 4, 5, and 6) are applied to band decoder U3023, an open collector decoder. Band 1 is always selected in this instrument, so pin 1 of U3023 is low, enabling the Band 1 Gain control (R2031) in the Band Leveling control circuit. The other output lines are all high, causing the gain controls for the other bands to have negligible effect.

The band 1 control current, in conjunction with a 7.5 V reference source (provided by operational amplifier U3038B and driver transistor Q3036), produces a voltage at the output of a operational amplifier U3038A.

The output of U3038A is applied through edge connector pin BB to the gain control PIN diode in the Band Leveling circuit.

Summarizing, current through Band 1 Gain control R2031 and the emitter of Q3036 sets the voltage through R2033 to the summing input of operational amplifier U3038A. The output of U3038A sets the current through a PIN diode on the Band Leveling board. This changes the gain of the stage according to the setting of Band 1 Gain control. If the PIN diode current increase, its effective resistance decrease, thus increasing the gain.

The board has space to install diodes at the band 2 through 11 outputs of U3023. These are only installed when needed in multi-band instruments. The extra diodes are not installed in this instrument.

The +5 V regulator circuit, U3041, supplies a noise-free +5 V source for the VR system. This is required because of noise in the +5 V main supply.

2nd Filter Select Circuits (Diagram 18)

Circuits on the 2nd Filter Select board (A68A8) operate in conjunction with the circuits on the 1st Filter Select board (A68A4) to set the overall system bandwidth. Banks of filters are selected under the master microcomputer control. Data bits 0, 1, and 2, from the data bus, are applied to decimal decoder U3070 (which outputs a low on the appropriate output pin to enable the selected filter). Bandwidth selections are 1 MHz to 100 Hz in decade steps, plus 30 Hz.

Filter selection is accomplished as previously described for the 1st Filter Select circuit except for the 100 Hz/30 Hz selections.

When 100 Hz resolution is selected, pin 6 of U3070 is low. Diode CR3068 turns on and pulls line 5 low. Q2020 turns on to enable the 100 Hz path through CR1017. Q3013 is also biased on and shunts R3013 to ground through C4014. When 30 Hz resolution is selected, U3070 pin 7 (output 6) goes low, Q2020 is again biased on to enable the 100 Hz/30 Hz path. Q3013 is biased off and R3013 now becomes part of the attenuator network at the input side to the crystal filter FL6015. This decreases the amount of attenuation and compensates for signal loss when in 30 Hz resolution. The 30 Hz level is set by a control on the 10 dB Gain Steps board (A68A5), as previously described.

The input signal, from the Band Leveling circuit via jumper EE, is routed through the selected filter to the Post VR Amplifier circuit, via jumper JJ. Nominal loss through the filter circuit is approximately 12 dB, with internal adjustment compensation for variations between the filters. The output level is nominally −12 dBm.

The filter for each bandwidth ranges from no filter at all to a temperature compensated crystal filter. An important difference between the 1st and 2nd filter select circuits is the addition of a gain adjustment in all except the 100 kHz circuit. This adjusts the amount of attenuation through the other filters and matches the output level to that of the 100 kHz filter. Since the Band Leveling circuit furnishes compensation gain to obtain equal signal levels for all bands, this adjustment compensates for variations between the filters.

No filter is used in the 1 MHz path because of the 1 MHz band-pass filter (FL 36) between the 2nd and 3rd Converters and the 1.2 MHz filter in the VR Input stage. An adjustable attenuator, adjusted by R1065, is used to provide initial signal leveling to compensate or offset the gain loss associated with the other filters in the resolution circuits.

The 100 kHz filter is a double-tuned LC circuit designed for a good time-domain response shape. The filter is tuned with composite variable capacitors consisting of small air variables paralleled with switched fixed capacitors. A third variable capacitor may be adjusted to establish the desired bandwidth. For Option 07 instruments, a similar 300 kHz filter replaces the 100 kHz filter.

The 10 kHz filter uses a two-pole monolithic crystal filter. The impedances at the input and output are matched to 50 ohm by T5047 and T7050. An attenuator that contains Gain adjustment R3039 is included at the filter input for filter variation compensation.

The 1 kHz filter is also a two-pole monolithic crystal with impedance matching transformers T4044 and T7043. A Gain adjustment is also part of the attenuator.

The 100 Hz/30 Hz filter is a temperature-compensated high-Q crystal filter. The actual filter bandwidth is about 200 Hz. This filter augments the filter in the 1st Filter Select circuit and reduces noise produced in the intervening stages. Freq Adjust R4025, in a voltage divider circuit, sets the center frequency of the crystal filter.

Post VR Amplifier Circuit (Diagram 18)

The Post VR Amplifier circuit provides the final VR system gain to bring the signal to the required +6 dBm output level and provides the final band-pass filtering. The circuit consists of two stages of gain followed by a filter.

The input signal, at a nominal −12 dBm, is applied through toroid transformer T2063 to the base of common-emitter amplifier Q2056. Gain adjustment R2038, in the emitter circuit, sets the Post VR amplifier gain. The output is transformer coupled, by T1059, to the base of feedback amplifier Q1048. This circuit includes emitter degeneration through resistor R2042 and collector-to-base feedback through resistor R1052. The collector feedback helps to provide a well-defined output impedance of 50 ohms. Input impedance is a function of transformer T1059 and resistor R1058 across the primary winding.

From the final amplifier, the signal is applied through the 1.2MHz band-pass filter comprised of capacitors C2033 and C2018 and the components between. This filter is a double-tuned design with an insertion loss of approximately 2 dB. The output filter is the complement of the 1.2 MHz VR Input filter. As mentioned in the VR Input description, two-pole bandpass filters with a bandwidth over ten percent of the center frequency tend to degenerate into either high-pass or low-pass filters. The VR Input filter acts as a high-pass filter and this filter acts as a low-pass filter. The combination of the two gives the desired bandpass characteristic for the overall VR system. The +6 dBm output signal from the filter is applied through coaxial connector J682 to the Log Amplifier.

LOG AMP and DETECTOR (Diagram 19)

The Logarithmic (Log) Amplifier and Detector accepts input signals from the VR circuits with a dynamic range to 90 dB. The signals are amplified so the output is proportional to the logarithm of the input. The output is then applied to a linear detector which outputs a video signal. By controlling the compression curve characteristics, each dB change in the input signal level results in an equal increment of change in the output. In the 10 dB/div mode, each division of displacement on the screen represents a 10 dB change of input signal level.

Table 7-3
PROGRESSION OF GAIN REDUCTION

Input Level	Point 1	Point 2	Point 3	Point 4
	Beyond Logging Range			
X−10 dB	0.00316	0.01	0.316	0.1
				0.216
X Level	0.01	0.316	0.1	0.316
				0.684
X+10 dB	0.0316	0.1	0.316	1.0
			0.684	0.684
X+20 dB	0.1	0.316	1.0	1.684
		0.684	0.684	0.684
X+30 dB	0.316	1.0	1.684	2.368
	0.684	0.684	0.684	0.684
X+40 dB	1.0	1.684	2.368	3.052
X+50 dB	3.16	Beyond Logging Range		

Log Amplifier Circuits

The Log Amplifier circuits logarithmically amplify the input signal from the VR circuits and apply the output signal to the Detector circuit. This circuit consists of seven ac-coupled amplifier stages. Each stage has two gain values that depend on signal amplitude. In addition, the first three stages have an extra automatically selected gain value. The combined circuits provide high gain for low-level signals and low gain for high-level signals. For the output signal to be proportional to the logarithm of the input, more gain is required for a change from −80 dBm to −79 dBm than a change from −1 dBm to 0 dBm. For a given stage of the circuit, the gain starts at approximately 10 dB for a low-level signal and decreases to unity as the input signal level increases. In the first three stages, the gain becomes less than unity as the signal amplitude increases.

Input signal levels nominally range between −84 dBm and +6 dBm. As the signal level increases, the gain decrease begins with the final stage and proceeds, in succession, back through the remaining six stages to the first. Each stage initially produced approximately 10 dB of gain. That gain was reduced to unity, so the total gain reduction is 70 dB. With further increases in input signal level, three more gain change steps take place. The gain of the first three stages is reduced below unity approximately 7 dB for each stage. This reduction starts with the first stage and proceeds to the third, to provide an additional gain reduction of approximately 20 dB.

As the input signal increases from −84 dBm to +6 dBm, the gain through the amplifier decreases logarithmically so that the output signal is exactly proportional to the logarithm of the input. This is accomplished through a system of series diode limiting in each stage, with a second set of diodes for extra limiting in each of the first three stages.

The following description of a simple three-stage log amplifier, with one gain step in each stage, provides an aid to understanding the concept of a logarithmic amplifier. For the example amplifier described and shown in Figures 7-4, 7-5, and 7-6, the gain of each stage is 3.16 V (10 dB) up to an output level of 1 V peak, then unity for output levels greater than 1 V peak; that is, each stage uses one breakpoint. That breakpoint voltage is used for ease of illustration; the actual breakpoint voltage is significantly lower.

The amplifier is shown in Figure 7-4. The source has a step attenuator that allows the input signal to be incremented in 10 dB steps. Table 7-3 shows the progression of gain reduction above 1 V at each amplifier output. Note that with each input level change of 10 dB, the output change at point 4 is 0.684 V. The gain curve for one stage is shown in Figure 7-5. Also note that when the level at point 1 is increased beyond 1 V, it is beyond the logging range of the amplifier. Similarly, if the input level is decreased 10 dB below the minimum input level, the output increment is different. A curve of the logging range is shown in Figure 7-6.

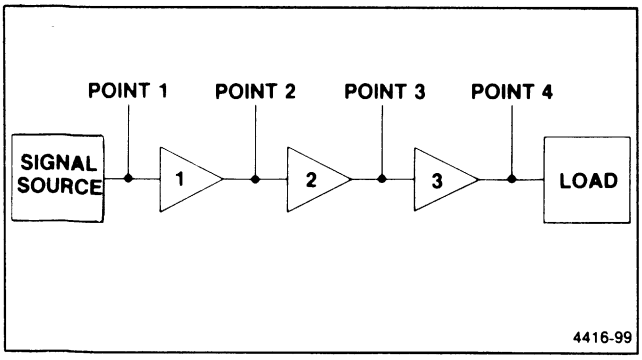


Figure 7-4. Block diagram of a three stage log amplifier.

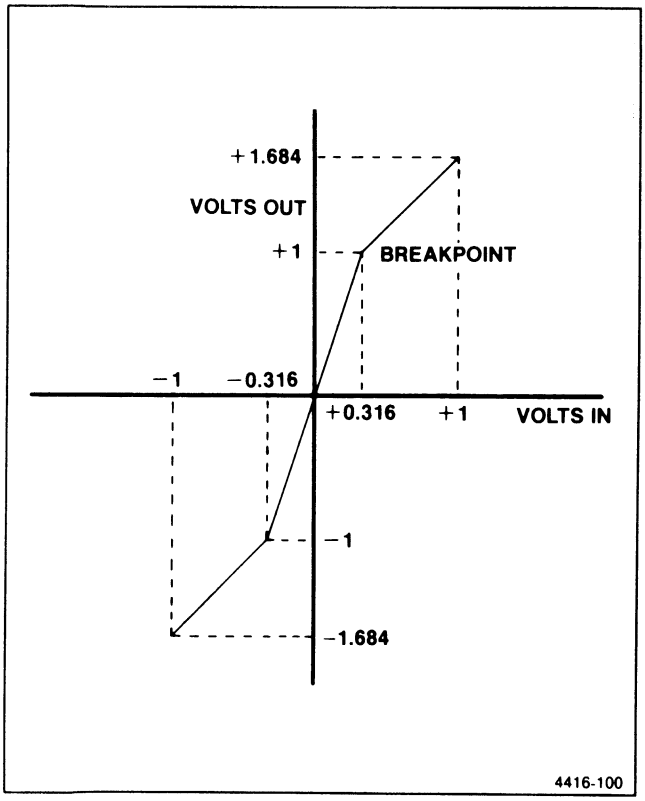


Figure 7-5. Log amplifier gain curve showing break points.

The signal is applied from the VR circuits to input preamplifier Q3105, in the Log Amplifier circuits, through coaxial connector P621. The input preamplifier provides transfer from 50 ohms to the high- impedance input of the first amplifier stage. The input signal is also applied to transistor Q2105, a common-base amplifier that acts as a buffer to supply the 10 MHz IF signal to the rear panel connector.

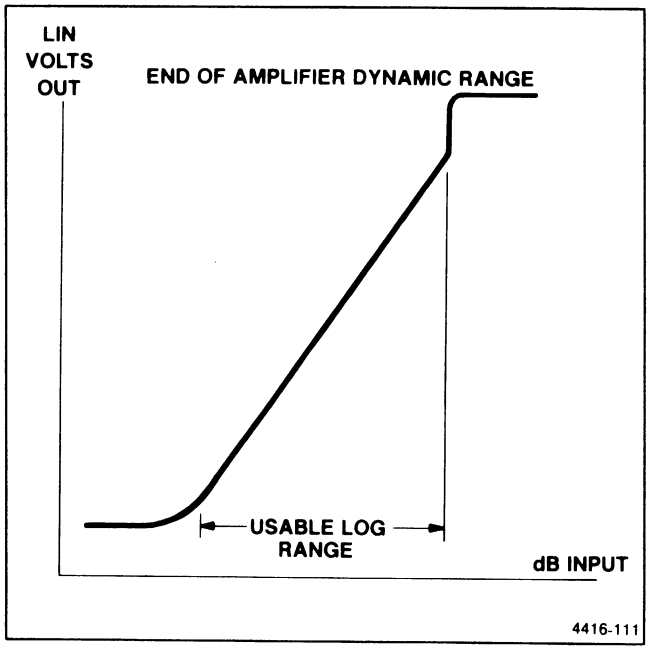


Figure 7-6. Curve showing end-of-range for a log amplifier.

From the input preamplifier, the signal is applied to the first of seven cascaded amplifiers that consist of Q3100-Q1095, Q3090-Q1080, Q3075-Q1070, Q3055-Q1050, Q3045-Q1035, Q3030-Q1025, and Q3015-Q6010, plus the associated circuitry. These stages are similar, except that the first three stages contain an extra set of diodes for a second gain step.

Typically, when the input level to transistor Q3015 is less than approximately 60 mV peak-to-peak, the transistor conducts enough to maintain forward bias on series limiting diodes CR4015 and CR4012. The RF signal path at that level is through both diodes, capacitor C5014, and resistors R4010H, R4010B, R4015, and R4010D, to common-base amplifier Q6010. The gain of the stage, under these conditions, is approximately 10 dB. As the input signal voltage increases, more current flows through CR4015 to increase the reverse bias of CR4012. This sharply reduces the stage gain to unity. The signal current then flows only in R4010B, R4015, and R4010D. This change takes place during the positive-going portion of each cycle. The opposite occurs during the negative-going portion of the signal above the minimum input level. As the input signal increases beyond the point at which the gain of the final stage decreases to unity, the same sequence occurs in the preceding stage, Q3030-Q1025, and in succession, back to the first stage, Q3100-Q1095.

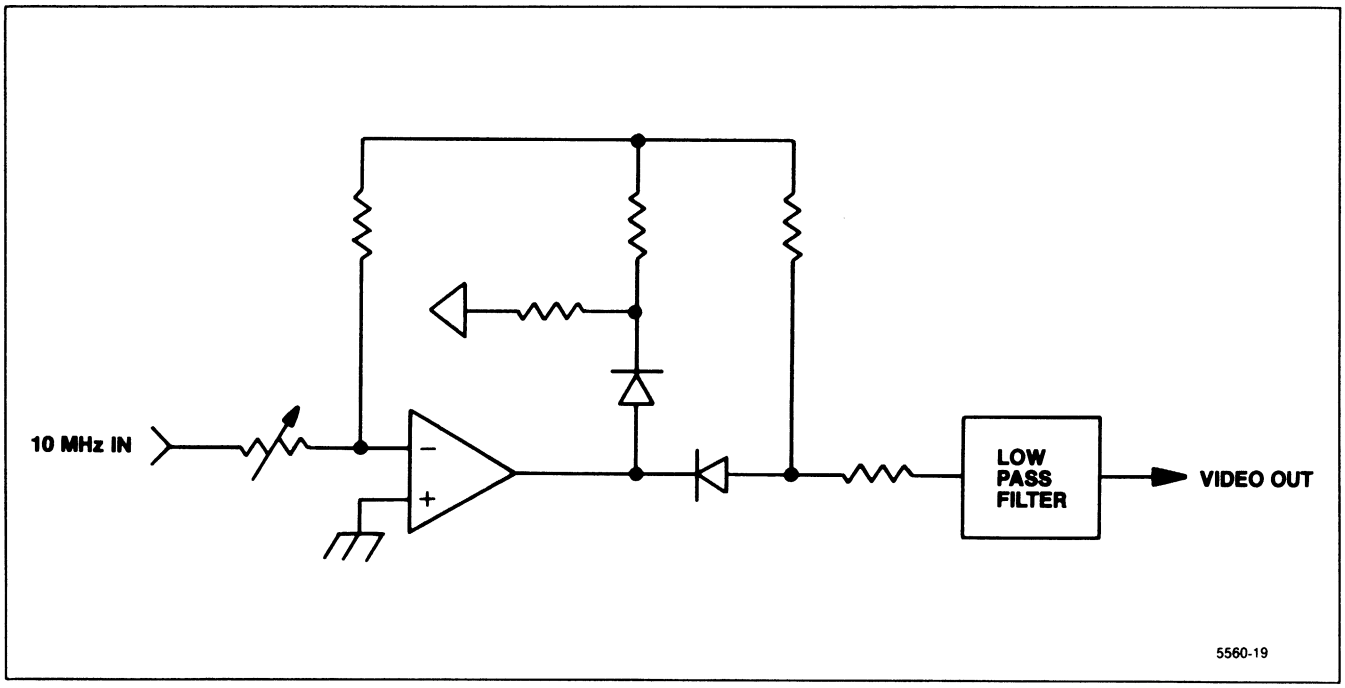


Figure 7-7. Simplified detector circuit.

Signal levels above this point activate the second tier of gain reduction in the first three stages. Each stage incorporates a second set of diodes that reduces the gain by another 7 dB. In the first tier of gain reduction, reduction started at the last stage and proceeded to the first; in the second tier, the reduction starts at the first stage and proceeds to the third.

In the first stage, diodes CR3089 and CR2087 are forward biased when the stage is in the unity gain mode. Limiting occurs in the same manner as previously described, with a further increase in input signal level, and results in less than unity gain through the stage (approximately 1/3). The one-two-three reduction sequence is established by the values of pull-down resistors R3082, R2076, and R2066.

Detector Circuit

This circuit detects and filters the output of the Log Amplifier circuit, and produces the VIDEO signal that is transmitted to the Video Amplifier circuits. The circuit consists of an operational amplifier with a diode detector in the feedback path and a low-pass filter at the output.

Although the circuit is called an operational amplifier, it is not easily recognized as such. It is made up of grounded emitter amplifier Q4025 and a differential amplifier that consists of Q4030 and Q4035. The summing node for the negative input is the base of Q4025 (the positive input is at the grounded emitter of Q4025). Also, the differential amplifier is designed for high impedance output to allow the current that is available from Q4025 to drive the operational amplifier very rapidly during the period when both detector diodes, CR5033 and CR5027, are effectively open circuited; that is, when the output is near 0 V. When neither diode is conducting, it is necessary that the output change rapidly through that zone. Note that the network consisting of resistors R5032, R5029, R5020, and capacitor C5029 is included to stabilize the point of dc operation.

Figure 7-7 shows a simplified schematic diagram of the detector circuit. As shown in this diagram, detector diodes CR5033 and CR5027 are used, but only the negative half cycle is taken as the output (from CR5027). The output from the collector of transistor Q4035 is applied to the diodes through capacitor C5035. Ac coupling is used on both sides of the detector to prevent temperature coefficient effects of the operational amplifier from affecting the detector output. This isolation occurs when the detector charges and discharges capacitors C5035 and C5024, by the current induced in each half cycle of the signal without a change to voltage level.

The positive-going output signal from the detector is applied to the Video Amplifier through a low-pass filter that consists of capacitors C7024, C7014, C7021, C7011, C6021, and inductors L6011, L8021.

DISPLAY SECTION (Diagram 5)

FUNCTIONAL DESCRIPTION

The display section consists of the following major blocks:

- Video Amplifier
- Video Processor
- Digital Storage
- Deflection Amplifiers
- Z-Axis
- CRT Readout

The Video Amplifier amplifies the detected IF signal, performs a log-linear conversion for linear displays, and provides pulse stretching if selected for narrow pulsed signals.

The Video Processor provides leveling to correct front-end unflatness, video filtering for noise averaging, out-of-band blanking to clamp the display to the baseline when the sweep is outside the frequency range, and video marker capability for use with a TV sideband adapter.

The Digital Storage digitizes the video and sweep signals and stores the data in memory. Stored data is then converted to analog signals for the Deflection Amplifier and Z-Axis circuits.

The Deflection Amplifier provides the drive voltages for the CRT. This includes vertical and horizontal deflection signals as well as readout characters from the CRT Readout board.

The Z-Axis circuits receive and decode data from the microcomputer; accept control levels from the front-panel beam controls and generate unblanking signals to control the display appearance, brightness, and focus; detect power failure; monitor the instrument voltage supplies; and record the elapsed operating time.

The CRT Readout circuits generate the alphanumeric characters (letters and numbers) for the display.

VIDEO AMPLIFIER (Diagram 20)

Video (detected) signals, from the detector and log amplifier in the IF section, are received by the Video Amplifier. In the logarithmic mode, the signals are amplified linearly and applied to the Video Processor. In the linear mode, exponential amplification converts the logarithmic gain characteristic to linear function. In either mode, baseline compensation from the Video Processor is applied to the video signal to compensate for any unflatness in the front-end response. The pulse stretch circuit at the output of the Video Amplifier alters narrow pulses so data can be acquired and displayed by the Digital Storage logic. Signal amplitude offset circuits provide display offset for the "Identify" mode operation.

Log Mode Circuits

The log mode circuits process VIDEO signals from the Log Amplifier, and add offset for selecting that segment of the log amplifier gain curve to be displayed. The circuits also select screen display gain steps from 1 dB/div to 15 dB/div.

The VIDEO and the VIDEO 1 signals are summed at the input to operational amplifier U4090A. Front-end unflatness is compensated by the VIDEO 1 signals, which are equal and opposite in amplitude to the unflatness. The two signals are also summed with the reference level, set by R4071, and the output of the digital-to-analog converter (DAC) U5041.

The DAC converts the microcomputer commands to an offset signal that selects the location on the log amplifier curve for the display (see Figure 7-8). In dB/div or log display, a change in the Vertical POSITION control produces an effect, after the log amplifier, that is the same as a signal level or gain change before the log amplifier. Instead of using a large amount of linear gain before the log amplifier, the output of the DAC (U5041) effectively moves the display up or down along the log curve. This process is called offset. Offset produces the same effect as varying the POSITION control except the display position does not change, only the signal level required to reach the reference level changes. Nominally, the log amplifier operates with +6 dBm at the top of the screen.

The output of U4090A is equivalent to 20 mV/dB. Full screen is 2.2 V. At 2.2 V, the output of variable log gain amplifier U4090B is 0 V. This is the only voltage at which the feedback circuit switching network resistors of preamplifier U4090B can be switched without changing the output voltage. (The switching network is described later in this discussion.) The 2.2 V output of U4090A is adjusted to full screen by Input Ref Lvl potentiometer R4071.

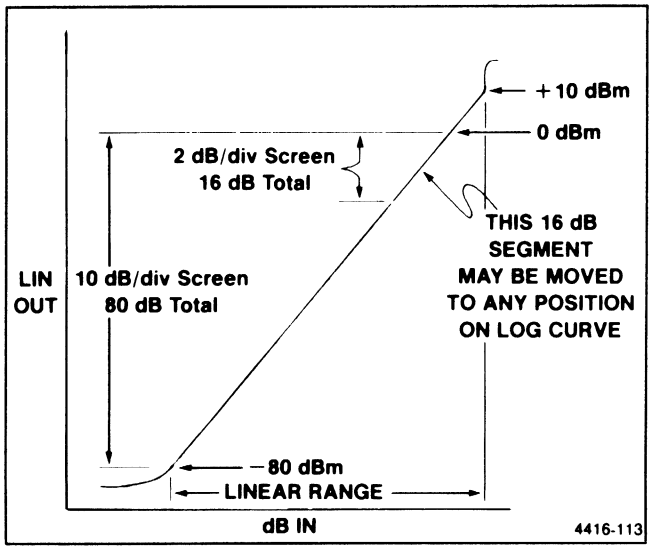


Figure 7-8. Selection of display position on the log scale.

From U4090B, the output signal is applied through FET Q5090 (if that transistor has been turned on by data bit 5 when it is high) to operational amplifier U4090C, pin 10. The signal then travels through emitter follower Q4100 to the Video Processor via the LOG CAL adjustment on the front panel. Output Ref Lvl (output reference level) potentiometer R4081, in the input circuit to U4090C, is adjusted so the output level is a full screen display after the Input Ref Lvl potentiometer R4071 is set for no change in the output of U4090B when switching between the 10 dB/div and 2 dB/div modes.

The gain switching network provides for 15 resistance values to be switched into the feedback path of variable log gain amplifier U4090B. The network consists of FET switches Q4075, Q4070, Q5070, and Q5075, and resistors R6080, R6074, R6073, and R6082. The FET switches, controlled by data bits 0, 1, 2, and 3 from the instrument data bus, switch in feedback resistors for U4090B in 15 value combinations determined by the binary content of the four data bits.

Linear Mode Circuits

The linear mode circuits accept the log preamplifier U4090A output and rescale the signal level to linear values. Since no switching is provided by the Log Amplifier circuits (i.e., all signals are logarithmically scaled), the signal level must be re-exponentiated to operate the system in the linear mode. High gain is required at the top of the screen and low gain is required at the bottom of the screen to offset the characteristics of the Log Amplifier circuits.

In addition to the signal path described for the log mode circuits, the output from preamplifier U4090A is also applied to linear mode operational amplifier U4090D, with a successive resistor network in the feedback path. From this amplifier, the output signal is applied through FET Q5095 (when enabled by instrument bus data bit 4) to the summing node at the input of output amplifier U4090C. After this point, the signal path is identical to that of the log mode description.

Starting at the signal level that represents the top of the screen (0 V) at the output of linear mode amplifier U4090D, the operation of the network is as follows.

With a +6 dBm input from the Log Amplifier to the Video Amplifier, the output of U4090D is 0 V. At that level, the feedback path is only through resistor R4097. The other feedback resistors (R4096, R5103, R5105, and R5107) are not in the path, because the switch transistors are biased off by the bias network consisting of resistors R5111, R4109, R4107, R4105, and R4103, plus diode CR4103. (The diode is included for temperature compensation purposes.) As the display moves away from full screen, the output voltage of U4090D increases and turns transistor Q6115 on. This places R4096 in parallel with R4097 to reduce the gain. As the voltage output increases, transistors Q6110, Q6090, and Q6095 start to conduct in sequence, adding resistors R5103, R5105, and R5107, respectively, across the feedback path. This effectively reduces the gain of U4090D exponentially. The transistor characteristics smooth the step transitions, producing a smooth exponential gain curve.

Pulse Stretch Circuit

The pulse stretch circuit consists of FET switch Q7110 and the associated components in the feedback path of output operational amplifier U4090C. When the pulse stretch mode is not selected (data bit 7 on the instrument data bus is low), pin 13 of U6060 pulls down to −15 V, and Q7110 is biased off. This removes C8104 from the circuit and also supplies sufficient negative bias though R7105 to keep CR8107 forward biased. With CR8107 on, the feedback loop for U4090C, through Q4100 and R7094 is closed so the signal output will fall as fast as it rises.

When the pulse stretch mode is selected (data bit 7 high), the open collector output of U6060 (pin 13) is allowed to float. This turns Q7110 on which completes the path for C8104 to ground. During signal rise time, C8104 now charges through the low impedance of CR8107. The feedback path for U4090C is still closed which provides a fast rise time. When the output of U4090C begins to fall, CR8107 turn off and the signal fall time is now a function of the RC time constant of R8106 and C8104, since the feedback loop for U4090C is now open. Diode CR7103 turns on to prevent

U4090C from slewing too far negative.

The identify offset circuit vertically shifts the display when the identify feature is in operation so that true and false signals can be identified. This feature is implemented elsewhere in the analyzer, except for the offset. When the "Identify" feature is in operation, it allows the operator to distinguish between responses which result from signals for which the analyzer is calibrated (true signals) and those that are produced by other spurious or harmonic conversions (false signals).

This is accomplished by moving the 1st and 2nd LO frequency an equal and opposite amount on every other sweep. The result is that false signals will shift a significant amount horizontally on the display while true signals will remain within close approximation to each other. The offset circuit shifts the alternate or "Identify" sweep vertically (down approximately 2 divisions). This offset is accomplished by the microcomputer setting DB 6 high, during "Identify" sweep, so the open collector output of U6060 (pin 14) goes from −15 V to open. This removes the current normally flowing in R7097 from the summing node of U4090C and causes a −1.2 V or 2 division shift in the VIDEO 2 output level of Q4100.

Digital Control Circuit

The digital control circuit provides the control signals that select the various Video Amplifier functions. Addresses 78 and 79 are decoded by U6070 and sent through inverter U5070 as clock or enabling signals for gain latch U6040 and mode latch U6050.

Gain latch IC U6040 is an 8-bit latch that supplies command data to the 8-bit DAC, U5041, to offset the Log Amplifier output signal. Mode latch U6050 is an 8-bit latch that supplies command data through buffer U5060 and U6060 to select the resistors in the dB/div switching circuit and to select identify, pulse stretch, and log or linear mode.

VIDEO PROCESSOR (DIAGRAM 21)

The Video Processor performs four functions. The first is compensation for flatness variations in front-end response. The second is video filtering, which provides the selection of six video bandwidths (30 kHz, 3 kHz, 300 Hz, 30 Hz, 3 Hz, and 0.3 Hz) under control of the instrument microcomputer. The third function is out-of-band blanking, which blanks the upper and lower ends of the local oscillator swept frequency range to provide a selected window for the display. This function is also controlled by the microcomputer. The fourth is the capability to generate a negative-going ditch marker on the video display for interfacing with a 1405 TV Sideband Adapter.

Interface with 1405 TV Sideband Adapter

The TEKTRONIX 1405 TV Sideband Adapter is a specialized tracking generator that is used with the Spectrum Analyzer to analyze the response of a television transmission system. The Spectrum Analyzer monitors the RF output of the transmitter while the sideband adapter drives the video input of the system. The video input may be at the transmitter site, the head end of the studio-transmitter link, or the video switcher in the studio. The sideband adapter must be connected to the 1st LO of the Spectrum Analyzer by a short length of coaxial cable.

The system in Figure 7-9 shows a TV transmitter operating on Channel 10 with a video carrier at 193.25 MHz. The sideband adapter is tuned to Channel 10. The Spectrum Analyzer is tuned to 195.25 MHz with a span setting of 1 MHz/Div (for purposes of illustration, the sweep is assumed to be halted at the center frequency of the analyzer).

The sideband adapter applies a 2 MHz signal to the AM modulator of the video transmitter. The modulator produces a lower sideband at 191.25 MHz, a carrier at 193.25 MHz, and an upper sideband at 195.25 MHz. This signal is amplified, filtered, and combined with the FM aural signal. The composite signal is sensed by a RF pickup and applied to the RF Input of the Spectrum Analyzer.

The 1st Converter applies the composite signal to the 1st mixer. The composite signal is mixed with a 2.26725 GHz signal from the 1st LO, forming three products. The subsequent stages of the analyzer accept only the 2.072 GHz product and reject the rest. For frequencies used in this example, the accepted product is the difference between the 1st LO and the upper sideband of the TV signal.

The product is converted twice more, amplified, filtered, log amplified, and detected. This detected signal is applied either directly to the video amplifiers of the crt or to digital storage.

The Spectrum Analyzer 1st LO signal is applied to the RF mixer of the sideband adapter. The 2.26525 GHz signal from the tunable LO is subtracted from the 2.26725 GHz signal from the Spectrum Analyzer LO, yielding a 2 MHz product. This video frequency signal is conditioned with sync and blanking signals and applied to the video input of the TV transmitter.

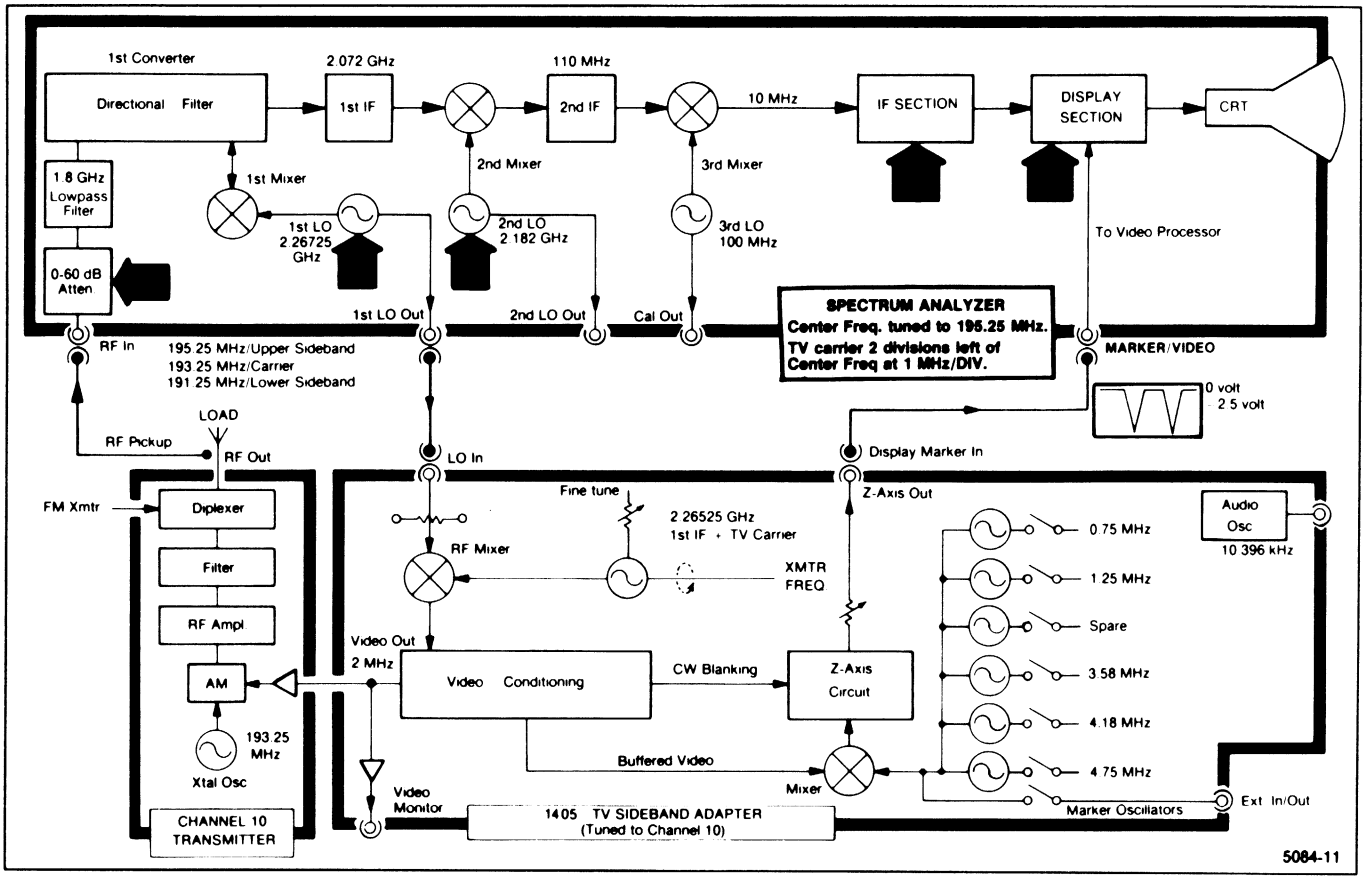


Figure 7-9. Functional diagram showing the Spectrum Analyzer and 1405 TV Sideband Adapter System.

When the Spectrum Analyzer is sweeping, the video signal starts at 3 MHz, falls to 0 Hz, and rises up to 7 MHz. During this interval, the analyzer displays the lower sideband as it moves toward the carrier, displays the carrier, and then displays the upper sideband moving away from the carrier. Since the Spectrum Analyzer and 1405 TV Sideband Adapter system is similar to a tracking generator system, it rejects noise and uncorrelated signal. This allows normal in-service use of the transmitter by adding a low level (1 to 3 IRE units) cw signal to the video or by using full levels with a VITS inserter.

The sideband adapter can insert frequency markers at preselected deviations from the carrier frequency. Six selectable crystal oscillators have their outputs mixed with video signal and applied to a Z-Axis circuit. This circuit produces two negative pulses as the video signal sweeps through the crystal oscillator frequency. These pulses are applied to the spectrum analyzer marker input, where they appear on the crt as two notches on either side of the marker frequency. The sideband adapter allows the width and depth of the notches to be adjusted with the Width and Intensity controls.

Video Marker

The Z-Axis signal from the 1405 Sideband Adapter connects to the MARKER input on the spectrum analyzer rear panel. This negative-going signal flows through the Accessories and Mother boards to the Video Processor board. Here, the signal drives the emitter of Q4060 and turns the transistor on, pulling the VIDEO OUT line down. This produces a notch in the video signal of the display to signify the location of the marker on the display.

Video Leveler Circuits

Video leveling compensates for analyzer front-end circuit characteristics that cause unflat response. Leveling is accomplished through programmable perturbation of the display baseline that is opposite in direction to the flatness error. As the signal power output decreases, the baseline rises an equal amount to compensate, and as power output increases, the baseline falls an equal amount. The perturbation is produced by a normalizer integrated circuit that produces 19 evenly spaced values of the input voltage, with each value corrected to compensate for unflatness.

The Osc Freq signal from the 1st LO driver circuits is applied to a translation circuit that consists of two current drivers (U3045A and half of Q3038, plus U3045B and the other half of Q3038). The Osc Freq signal is directly related in amplitude to displayed analyzer frequency. The nominal +10 V to −10 V excursion voltage versus frequency curve, in maximum span, relates to the full band. This 20 V maximum excursion is scaled to a precise current (from 1 mA at +10 V to 0 current at −10 V) that is applied to the normalizer IC to generate the baseline perturbation. Actual signal scaling is done by current driver U3045A/Q3038. The output signal is applied to the normalizer SWP IN input, pin 5 of U2039. The second current driver, U3045B/Q3038, generates a 2 mA reference current for the normalizer. Horizontal Freq adjustment R1069, in the input translation circuits, shifts the 19 evenly spaced points up or down in frequency to compensate for unflatness.

Normalizer IC U2039 operates as a shaper and contains 19 transistors that turn on and off in sequence as the current input to pin 5 decreases from 1 mA to 0. Each collector is connected to a potentiometer that allows output trimming. Potentiometer R1061 is active with no current, and R1013 is active at 1 mA. The trimming operation is described later.

From the normalizer, the output is applied through a jumper switch to buffer amplifier U2055B, which has a gain of five, then to offset amplifier U2055A. This amplifier has a gain of two, but its primary purpose is to offset the 0 to +5 V (normal), 0 to −5 V (invert), buffer output to the levels required by the Log Amplifier circuits. The range required by the Log Amplifier is 0 to −10 V. The output voltage is a series of linear interpolations of the voltage between adjacent trimming resistors at the outputs of the normalizer. Compensation adjustment R1065 sets correct interpolation.

Jumper plug P2060 selects the input side of buffer amplifier U2055B and proper offset voltage for U2055A. This provides the means to invert the buffer output during the instrument adjustment procedure. The adjustment procedure is described in that section of this manual.

DB0 is always a 1, pins 3 and 2 of switch U2015 are connected, and the output from offset amplifier U2055A is supplied out as the VIDEO 1 signal.

Video Filter Circuits

The video filter circuits provide additional bandwidths than those available with the Variable Resolution filters. Either wide or narrow-band video filtering is selected at the front panel. The microcomputer determines the actual bandwidth selected, based on such factors as sweep rate and total dispersion. Either internal or external signals can be applied to the video filter circuits. A simplified schematic diagram is shown in Figure 7-10.

The EXT VIDEO signal, from the rear-panel MARKER| VIDEO connector, is applied to pin 15 of switch U3063A through edge connector pin 53. The INTERNAL VIDEO signal, from the Video Amplifier circuits (via the front-panel LOG CAL control), is applied to pin 2 of U3063A through edge connector pin 51. The internal video section of switch U3063A is normally held energized (pins 2 and 3 connected, pins 15 and 14 disconnected) by the +5 V supply through R3064. If the EXT VIDEO SELECT line (from the rear-panel ACCESSORIES INTERFACE connector, through edge connector pin 55) is grounded, the external video sections of U3063A are energized. When this occurs, the EXT VIDEO signal is applied through, or around, the filter to become the VIDEO FILTER OUT signal at edge connector pin 57.

Data bit 1 turns the video filter on. Data bits 2 through 4 select any of six bandwidths: 30 kHz, 3 kHz, 300 Hz, 30 Hz, 3 Hz, and 0.3 Hz. With no video filtering (data bit 1 low), the video system bandwidth is 500 kHz.

When the Video Filter is off, the signal is routed through U3062 and around the filter because the two sections of U3063B are selected by DB1. When DB1 is high, the video is routed through the filter.

The filter consists of resistors R2023, R2021, R2022 and capacitors C3026 and C2016, connected between U3062 and U2066. Table 7-4 lists the filter components in the circuit for each of the six video bandwidths. (An X indicates that component is used.) Data bits 2, 3, and 4 control switches in U2015 that select the filter components. From U2066, the signal is routed through contacts 7 and 6 of switch U3063B to edge connector pin 57 as the VIDEO FILTER OUT signal.

Video Blanking

The video blanking circuits blank the lower and upper ends of the local oscillator range. Selective blanking is required because the local oscillator sweeps the full span regardless of the band limits. The video system is designed to effectively open a display window only during the time for display. Data bits 5, 6, and 7, under control of the microcomputer, select the appropriate amount of display for each end.

Video blanking and the Osc Freq signal (which provides frequency information, in voltage form) are located on the Video Processor board. Switch U3063 incorporates a disable function that, when provided a low input, opens all switch sections regardless of individual section input. This feature allows the VIDEO FILTER OUT signal to be easily blanked at will.

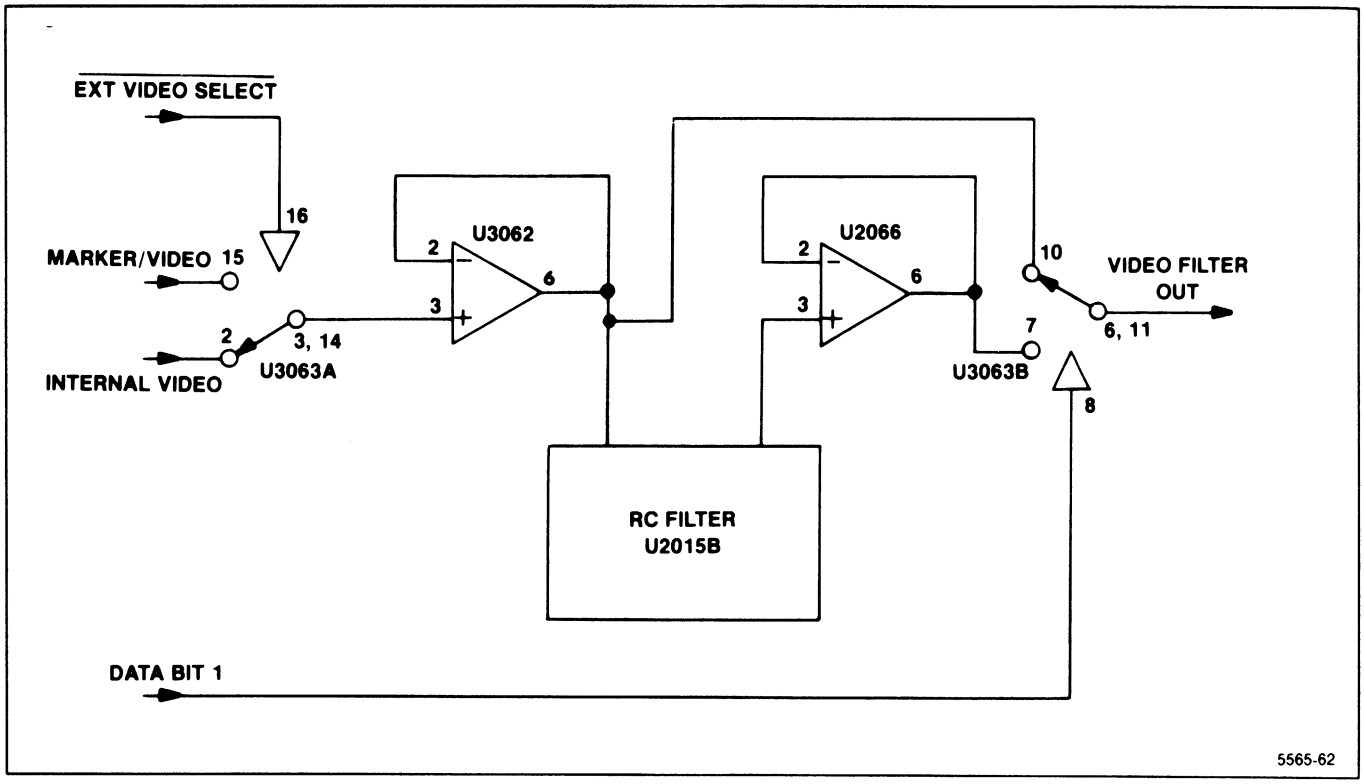


Figure 7-10. Simplified diagram of a video filter.

Table 7-4
FILTER COMPONENT COMBINATIONS

Bandwidth	DB2	DB3	DB4	R2023	C3026	R2021	R2022	C2016
30 kHz	0	0	0	X	X	X	X	
3 kHz	0	0	1	X	X	X		
300 Hz	0	1	1	X	X			
30 Hz	1	0	0	X	X	X	X	X
3 Hz	1	0	1	X	X	X	X	X
0.3 Hz	1	1	1	X	X	X		X

The disable function is controlled by a combination of outputs from comparators U3015A and U3015B. Inputs to these comparators are from the Osc Freq signal and a combination of voltage dividers that are switch selected under control of data bits 5, 6, and 7. The Osc Freq signal is applied from edge connector pin 54 through divider resistors R4013 and R4012 to the inverting input of U3015A, and through divider resistors R4014 and R4011 to the non-inverting input of U3015B. These dividers reduce the excursion of the drive signal from (+10 V to −10 V) to (2.5 V to −2.5 V), which is the maximum input level to the comparators. The non-inverting input to U3015A (pin 3) is from divider resistors R3011, R3012, and R3020.

Input to the inverting input of U3015B (pin 9) is from divider resistors R4018, R4017, and when selected, R3028. Data bit 6 selects R3028 through pins 10 and 11 of U3025. The junction of R3011 and R3012 is connected to +5V through R3028 when it is selected. This switching arrangement of negative and positive levels for comparison with the reduced Osc Freq signal enables the top and bottom extremes of the frequency excursion to be blanked. The blanking signal controls the disable input (pin 13) of switch U3063B. When the blanking signal is low, U3063B has no output. When high, the output is normal.

DIGITAL STORAGE (Diagrams 22 and 23)

The Digital Storage circuits provide the ability to store and process a signal before displaying it. This allows flicker-free displays, even at the slow sweep rates required for narrow resolution bandwidth measurements. Digitizing the signal also allows signal processing and marker generation.

The processing includes detecting peak amplitudes (Max Hold), storing a signal (Save A), subtracting one signal from another (B−Save A), signal averaging (Averaging), and signal comparison (View A and View B). These operations use two memory banks to independently store two complete signals that are each digitized at 500 points across the sweep. Therefore, two signals may be observed simultaneously or processed in separate ways.

The markers are used in a variety of ways. There are two waveform markers that the user sets for various measurements. In addition, an update marker shows where the actual sweep is with reference to the refreshed display.[1]

Four instrument bus addresses are associated with Digital Storage. Addresses 7A and 7B are write addresses. FA and FB are read. These addresses are shared by both the Horizontal and Vertical Digital Storage circuits. Logic on the Horizontal Digital Storage board controls which set is active. 7A on the Horizontal Digital Storage board is further subdivided into 8 subaddresses by 3 bits in address 7B on that board. Address tables in the circuit descriptions for the appropriate boards show details of the Digital Storage addresses

In the Max Hold mode, the highest amplitude at each of the 1000 points in successive sweeps is stored and displayed. In the Save A mode, a signal is stored in one memory for later examination, and is not updated. In the B−Save A mode, the A signal is stored and not updated, then arithmetically subtracted from the B signal, which is stored, but continually updated. In the averaging mode, the display area is divided by a horizontal cursor. Signals above the cursor are peak detected and displayed, and signals below the cursor are averaged. In the View A and View B modes, the contents of the selected memory or memories are displayed.

Graphical presentation of mathematic functions or experimental data is common. One such graph has a single Y value for each X value. An alternate presentation of the data in this graph would be a table simply listing the X coordinate values along with a corresponding Y value for each X value. To further simplify the graph, if the first X value and the spacing between X values were known (all spaces assumed equal), the two-column table could be reduced to a single column with the X value implied by the position of the Y value in the column. This is the essence of digital storage — to convert a vertical analog voltage (Y coordinate value) to a binary number and insert that number in a stored table. The location of the Y value in the table is determined by the analog sweep voltage (X coordinate value) binary conversion. Once a set of binary numbers that represent values across a waveform is stored to create a table, the waveform can be recreated at any time by conversion of the table values (Y) and positions (X) back to analog voltages that represent amplitude and sweep positions.

The digital storage system uses a Table A and a Table B. Table B is updated every sweep. Table A is also changed unless the Save A mode is selected. There are 500 A values and 500 B values. The spacing between values is the same throughout both tables, but the starting point for Table B is shifted slightly so that when both tables are read, the readout values are interlaced.

When the signals are recreated, the contents of either Table A or Table B can be displayed, or both tables A and B can be displayed. If both Tables A and B are to be displayed, and the Save A mode is selected, the contents of both Table A and Table B are drawn, each display in its own trace. If the Save A mode is not selected, the contents of both Table A and Table B are displayed on one trace, with 1000 value positions across the screen. A third trace option is also available. In the B−Save A mode, the displayed values are those that result from an arithmetic operation and are the difference between the contents of Table A and Table B for each X value of analog sweep voltage.

Since a signal waveform is continuous and a table has discrete X values, an algorithm determines the Y value to be stored for a particular X value. This allows the operator to select one of two methods to determine Y values; peak or average. The Y analog voltage is continuously sampled, with the sampling rate dependent upon sweep speed. For each X value, there are always at least two samples, and there may be as many as 2^{17} samples. From this set of samples, either the largest sample value (peak value) or the mean of all the samples (average value) can be selected. Selection between peak and average is controlled by the front-panel PEAK/AVERAGE control, which sets a dc level that is compared with the analog vertical input to produce the PEAK/AVG logic signal. When the input signal is below the level selected by the front-panel control, the signal is averaged; when the input is above that level, the peak signal is displayed. The dc level appears on the display as a positionable horizontal line. This line is created when the dc level is switched to the analog output line

[1]There are also video markers that may be fed to the rear-panel MARKER| VIDEO input. These video markers are from an external source, and are not part of the digital storage system. See the Video Processor description for more information about the video markers.

during the cursor cycle by the CURSOR logic control signal.

Superimposed on the cursor line is an intensified spot called the update marker, which indicates the X value at which new Y values are being computed for display update. The update marker is formed when the analog sweep input is compared to the display analog X output. When the two are the same value, the sweep is forced to pause, which increases the marker intensity at that point.

Two custom integrated circuits are the heart of the digital storage circuits. The vertical control IC contains the vertical acquisition and display logic, peak detection, signal averaging, Z-Axis blanking, and special Y-value processing circuits. The horizontal control IC contains the horizontal acquisition address counter, horizontal display counter, 10-bit RAM address multiplexer, and a system control matrix. The other digital storage control circuits consist of two 8-bit digital-to-analog converters, two 10-bit digital-to-analog converters, one 10-bit latch, 8K bits of random access memory, and various auxiliary circuits. Timing is controlled by $\phi 2$ clock pulses (at 1 MHz) from the Processor board to the Horizontal Digital Storage board.

Vertical Section (Diagram 22)

The Vertical Control IC block diagram is shown in Figure 7-11. The vertical analog voltage is converted to a Y binary value by an 8-bit successive approximation register. Nine clock cycles are required for each Y conversion. After the conversion has taken place, the successive approximation register produces the negative-going SYNC signal. Most functions on both the vertical and horizontal control ICs are synchronized by this signal. On the negative-going transition of SYNC, the successive approximation register is reset to 10 00 00 00 (binary) and the next conversion cycle begins. Incoming data bits are latched into the register on the negative-going clock transition. From the register, the output data is applied to the peak and the averaging circuits.

The averaging circuit consists of three groups of circuits; those that accumulate all the Y values for a given X value into a grand total (called the numerator), those that count the number of samples that make up the numerator (this total is called the denominator), and those that subtract and shift to perform the division process.

As each new Y value is converted, it is added to the eight least significant bits of the numerator. Each carry from the most significant bit of this addition is counted by a 17-bit ripple counter. The contents of this counter and the 8-bit sum are cascaded to form a 25-bit grand total. Each time a new sample is added to the numerator, another 17-bit ripple counter is incremented to produce the denominator.

A division cycle starts when the horizontal control IC (on the Horizontal Digital Storage board) detects a change in the X value. At that time it generates the ST DIV (start divide) signal. On receiving this signal, and in synchronization with the SYNC signal, vertical control IC U2030 does five things (refer to Figure 7-11):

1. Latches the current numerator in a 25-bit latch (25-to-1 data concentrator) and latches the denominator in a 17-bit latch (17-to-1 data concentrator).

2. Clears the numerator adder circuits (25-bit summation register).

3. Performs a 17-bit priority encode on the denominator and loads a 1 in the appropriate cell of the 25-bit shift register.

4. Loads the latched numerator and denominator serially into the divide circuit (subtractor) using the contents of the 25-bit shift register as a mask.

5. Clears the denominator ripple counter (17-bit counter) to zero.

Ten clock periods are required to load the numerator and denominator into the divide circuit. The cycle starts on a SYNC pulse. The first bit of the quotient is available shortly after the first clock pulse that follows the next SYNC pulse. Division is performed by repeated subtract and shift operations. The quotient is arrived at serially with the most significant bit first. Since only 8-bit accuracy is required, with the priority encoder output used as a mask, the divider circuit is loaded with the 8 most significant bits of the denominator and the 16 most significant bits of the numerator. (Ripple borrow for a 17-bit by 25-bit subtractor would be so long that it would be impractical.)

The peak circuit consists of a peak detector and an 8-bit peak shift register. In operation, the previous peak Y value from the last set of samples is still stored in the peak shift register at the start of a conversion cycle. At that time, the peak detector, which is a serial compare circuit, is set to the state that questions whether the old or new number is larger. Each bit of the new value is then compared with the corresponding bit of the old value, most significant bit first. When one value is found to be larger, a flip-flop is set and the smaller number is gated out of the shift register. The start divide logic signal being true then forces the peak detector to select the new value and ignore the number in the shift register.

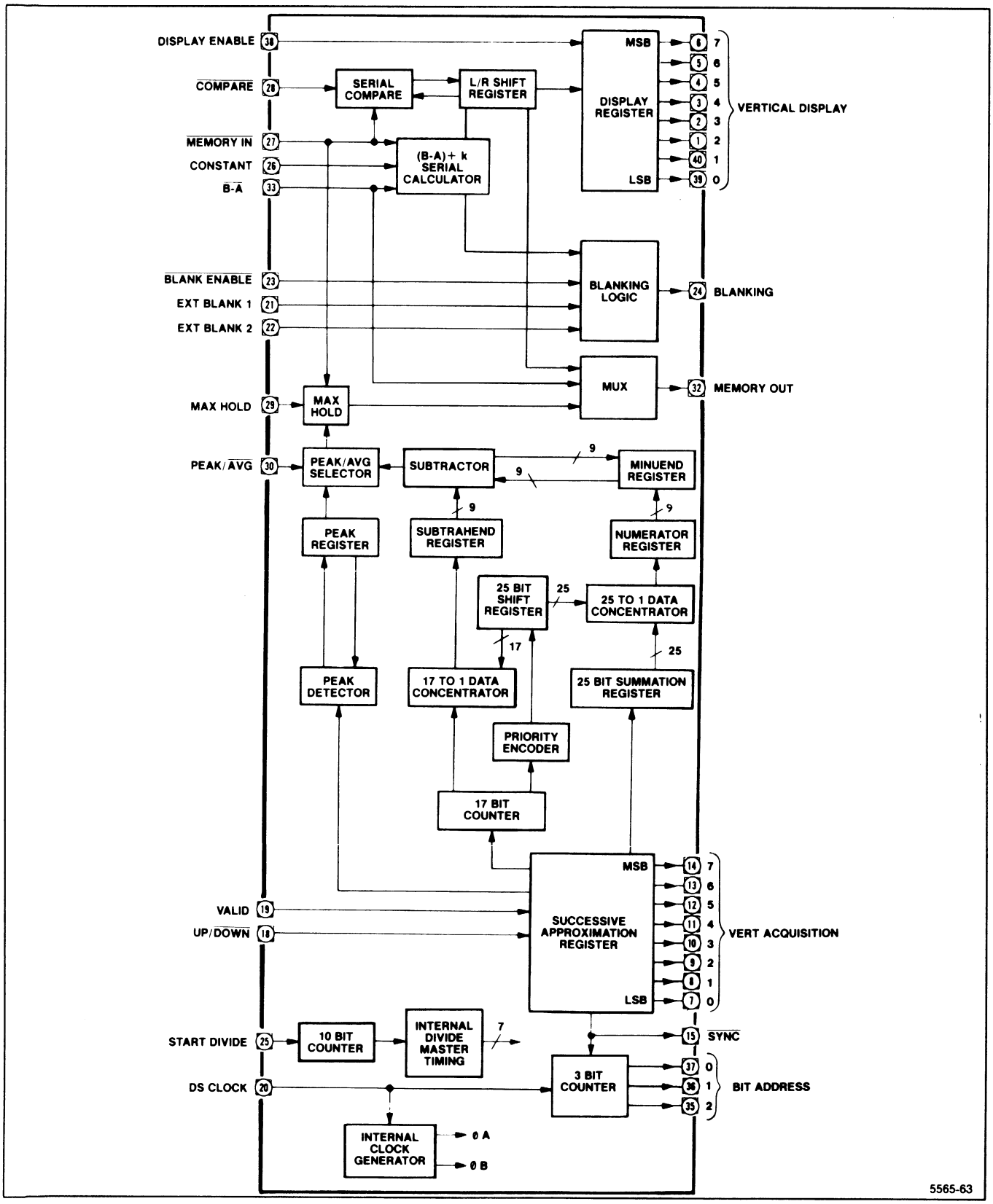


Figure 7-11. Vertical control IC block diagram.

The peak/average selector, a multiplexer, selects either the peak or average value to be routed to the memories under control of the PK/AVG signal. The selector output is routed through the Max Hold circuit, which functions like the peak detector. When the MAX HOLD signal is high, the value that is routed to the output multiplexer is the larger of two values; the current memory value at the subject X coordinate or the previously-selected peak or average value.

Timing to set up the divide operation and clear the numerator, denominator, and peak circuit is controlled by a 10-stage counter. Taps are taken from appropriate stages to develop the necessary clear and latch timing pulses.

All data enters and leaves the memory serially. Data read from memory enters an 8-bit shift register and, timed by the SYNC signal, is transferred to the vertical display output latch (display register). The same shift register is used for other purposes, so the DSPL EN (display enable) signal prevents non-display information from being transferred to the output latches. An example of data moving through this shift register is seen in the B−Save A display mode. The A value is first read from memory and stored in the shift register. As the B value is read, the subtraction is done serially and the answer is applied to the shift register. Since the subtraction must be performed with the least significant bit first, a set of exclusive-OR gates change the order of extracting B from memory. The shift register direction is reversed to present the most significant bit to the proper display latch. The shift register output is also applied to the output multiplexer.

In subtraction, the operation performed by the serial calculator is not merely B minus A. The actual expression implemented is (B−A) + K, where K is a serial input external constant specified by the user. This permits zero to be placed anywhere on the screen. To avoid confusion when (B−A) + K results in an off-screen position, the subtractor blanks the display. (The subtractor examines the carry bit and borrow bit when the most significant bit is calculated. If either bit is a 1, the screen is blanked.)

When the Save A mode is not selected and both A and B are being displayed, maximum resolution is obtained (1000 points across the display). If this display includes a very narrow pulse, it is possible that the top of the pulse is only as wide as a single X coordinate. If this maximum value were in the B Table and the Save A mode was selected and B turned off, there would be an apparent drop in amplitude. So, when the Save A mode is selected, a special set of circuits in U2030 compares all A and B values that have the same X value, and stores the larger in Table A. The B value is read and stored in the display shift register. Then, as the A value is read, it is compared with the B value and the larger of the two is loaded into the display shift register. Finally, the number in the shift register is written into memory. This operation is performed once each time that the Save A mode is selected.

Vertical control IC U2030 contains a 3-bit synchronous counter that identifies the specific bit of an 8-bit vertical value that is to be read from memory or written into memory. This is the only memory addressing that is performed by U2030. All other addressing is performed by the horizontal control IC (on the Horizontal Digital Storage board).

Digitizing Circuits. The input vertical signal, VID FLTR OUT, coupled through edge connector pin 60 is applied through buffer U3040 to sample and hold switch U2040C. U2040C is controlled by flip-flop U1010B. U1010B generates the sample pulse, and is enabled during the clock cycle after the last approximation, as indicated by the least significant bit from the successive approximation register in U2030. The switched sample is then applied through buffer U1045 to a summing junction. At this point the output current from digital-to-analog converter U3025, that is supplied from the successive approximation register in U2030, is subtracted from the sample current. The difference current is then applied through comparator U2035B and synchronizing flip-flop, U2027A, to pin 18 of U2030 as the UP/DOWN signal. The binary equivalent of the input sample is effectively produced by the combination of the successive approximation register, the digital-to-analog converter, and the sample and hold circuit.

Address Decoding. The address decode logic accepts inputs from the address bus and from the address control logic on the Horizontal Digital Storage board, producing the control signals for read and write operations:

CONT W (control write)

DATA W (data write)

DATA R (data read)

The control write signal gates the control word from the data bus into control register U2028 to generate mode control signals. This control word consists of one bit, Q4, that represents the front-panel MAX HOLD function. If output Q5 is low, a peak operation is forced; if output Q5 is high and Q6 is low, an average operation is forced. The data read and data write signals are applied to the interface logic to control memory read and write operations.

Interface Logic. The interface logic, in general, performs control and interface functions between the active data circuits in the vertical and horizontal sections and the rest of the instrument. It allows the microcomputer to control the storage system functions and to access the digital storage memory. It also contains the circuitry for serial-to-parallel and parallel-to-serial conversion. (The microcomputer uses parallel transfer; the digital storage memory uses serial transfer.) Shift register U4020 reads data from memory to the data bus. Register U2025 stores information from the data bus for transfer to memory. Multiplexer U4015 does the parallel-to-serial conversion and applies the data output to gate U3024B, which acts as a buffer to supply either the multiplexer output or the MEM OUT (memory output) signal from U2030 to the memory as the DSDI (digital storage data input) data train.

The interface circuit group on the Vertical Digital Storage board is the handshake logic that works with the horizontal control circuits to access the memory and to determine when to increment the memory address counter. In either a data read or data write operation (when the corresponding signal goes high), flip-flop U3020B is triggered. This releases the BUS REQ (bus request) line to allow that signal to go high and signals the horizontal control circuit that memory access is required. When the horizontal circuits recognize the request, those circuits pull the BUS REQ line low at the same time that SYNC is low. The interface logic detects the BUS REQ and SYNC low condition through U2015A, U2015B, U3010A, and U3015A, and produces the low BUS GRANT signal to indicate memory access. The BUS GRANT signal then enables shift register U4020 to shift data from memory or enable register U1021. BUS GRANT also enables multiplexer U4015 to shift data to memory as indicated by the DATA R and DATA W lines. At the end of a data read cycle, gates U2010B and U4030C produce the INCR ADRS (increment address) signal to increment the address register in the horizontal circuits.

Maximum Hold. As described previously, when the Max Hold mode is selected, the signal from Q4 of control register U2028 causes the circuits in U2030 to compare the binary equivalent of the input signal for a given X value with the information in memory for that same X value. This causes the larger value of the two to be stored in memory. The signal from Q4, in combination with the VALID signal from the horizontal circuits, produces the MAX HOLD command to U2030 through inverter U4030E and gate U4040A.

Constant Circuit. As described previously, in the B minus A operation, a constant is used. This constant is selected internally with switch S1015. This switch, in combination with multiplexer U2020, supplies the CONSTANT data to U2030. Multiplexer U2020 is, in turn, controlled by address bits 0, 1, and 2 to provide the proper constant data bit to U2030.

Output Circuits. From the U2030 vertical display register, the parallel data output is applied to 8-bit digital-to-analog converter U1035. The converter output is then applied to the output storage/cursor switch, U2040B, through a vector generator that consists of an integrator (U1040 and C1035) with an associated feedback loop sample-and-hold circuit. Integrator U1040 has a time constant that provides a ramp to last between the existing sample and the new sample (that is, between sync pulses). Circuits U2040A and U2045 and capacitor C2045 make up a sample-and-hold circuit with U2045 acting as an output buffer. From U2045, the output current through resistor R1036 subtracts from the digital-to-analog converter output current to modify the slope of the output ramp. The output of the vector generator is then applied to switch U2040B. U2040B, controlled by the MKR (marker) signal from the horizontal section, selects between the recreated video signal from U1040 and a dc (Peak/Average) level from buffer U3045, to be sent out as the vertical signal. The dc level is displayed only during retrace as the PEAK/AVERAGE cursor.

Peak/Average Level Circuits. The buffered PEAK/AVG LEVEL signal, from U3045, is compared with the sampled Video Filter Out signal, from U1045, by comparator U2035A. The output of U2035A is a high (1) if the Video Filter Out signal is greater than the PEAK/AVG LEVEL, or low if it is less. This output commands U2030, via U4040C and U4040D, to send peak or average data to the output. U4040B, C, and D are used if the instrument is under GPIB control to select one of three possible modes; Peak, Average, or front panel control knob.

Horizontal Section (Diagram 23)

Figure 7-12 is a block diagram for the Horizontal Control IC U5020. The horizontal analog voltage is converted to a current table value through a 10-bit tracking analog-to-digital converter (adc), which consists of up/down interlock and 10-bit up/down counter in U5020, and external 10-bit digital-to-analog converter (dac) U4040. The horizontal control IC generates a DS blank signal, blanking the display when HD 9-0 indicate that either the left or right-most 8 points are being generated. As the sweep moves right, the counter increments; as the sweep retraces, the counter decrements. Each time the counter increments, it generates a new X coordinate value (the dac input) and a ST DIV (start divide) signal to start the storage cycle.

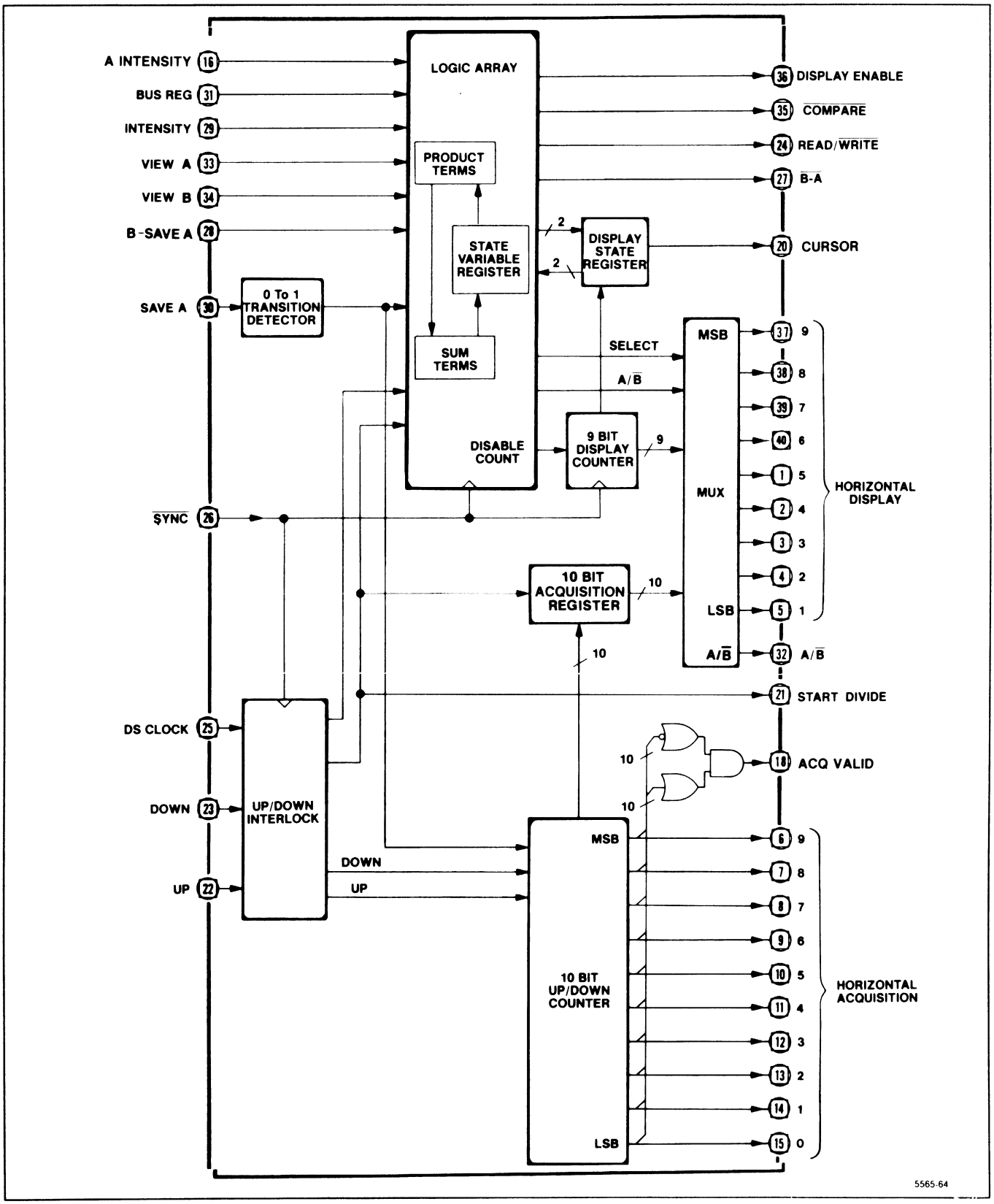


Figure 7-12. Horizontal control IC block diagram.

The increment clock is the SYNC signal, and the decrement clock is the basic digital storage clock divided by two. When the Save A mode is selected, the counter skips every other binary number, so only B coordinates appear as addresses.

A state machine provides the horizontal system intelligence. This circuit determines which trace to write on the screen, determines when to switch from read to write, generates the B–A coordination signals for vertical control IC (on the Vertical Digital Storage board), controls the 9-bit display counter incrementing, and processes requests for the memory bus.

When an external device elects to read from or write to memory, it allows the BUS REQ (bus request) signal to go high to request permission from the state machine. When the time becomes available, the state machine pulls the BUS REQ line low, which signals the start of a request cycle. For the next eight clock cycles, the internal multiplexer output lines are in the high-impedance (open) tri-state mode.

The combination of the up/down interlock, 10-bit up/down register, 9-bit display counter, and horizontal display multiplexer constitute the primary circuits that either write to or read from memory. To generate X values to be written into memory, the circuits convert the sweep voltage to binary form. These circuits also count the sync cycles to cause the external logic to read stored data from memory and produce a vertical signal (Y value) for each corresponding X value.

During acquisition cycles, the 10-bit up/down counter, controlled by the up/down interlock, operates in a loop with the external 10-bit digital-to-analog converter. This allows the counter to acquire the equivalent (X value) of a sample section of the sweep voltage. From the counter, the 10-bit output is applied to the 10-bit up/down register. During display cycles, the 9-bit display counter counts sync pulses to acquire the X value. Either the 10-bit up/down register output or the display register output is applied to the horizontal multiplexer under control of the SELECT signal from the State Machine. From the multiplexer, the output is applied to the memories as an address.

Marker IC. Marker IC U3020 performs several functions on the Horizontal Digital Storage board:

In conjunction with Horizontal Digital Storage IC U5020, it creates the two waveform markers and the update marker.

Controls the processor addresses assigned to digital storage — 7A, 7B, FA, and FB.

Takes control of the address lines to the display RAM when the microprocessor accesses the digital storage data.

To create the waveform marker, it monitors the horizontal display bits, HD0-9, and the CURS and B–A signals. When these lines indicate the display has reached a point that matches on of two points previously stored in the IC by the microprocessor, the IC sets A INTENSITY high, causing U5020 to repeatedly display the same point until A INTENSITY goes low again (which it does after a number of DS ENBL cycles previously stored in the IC by the microprocessor).

The update marker is initiated by a comparator detecting that the analog sweep and the display sweep have crossed as explained elsewhere. U3020 detects this event on the CSLFS line. If the VALID line is high when this occurs, U3020 sets INTENSITY high, causing U5020 to repeatedly display the same point until 15 DS ENBL cycles have passed. Then INTENSITY goes low again.

When the microprocessor wants to read values from or write data to the waveform memory, it first sends a starting address to U3020. Circuitry on the Vertical Digital Storage board (A61A1) controls the BUS GRANT line which indicates when U3020 can actually access the digital storage RAM without disturbing the display. When BUS GRANT goes low, U3020 (instead of U5020) drives HD0-9.

The Vertical Digital Storage board also generates an INCR ADRS (Increment Address) pulse for each BUS GRANT cycle. U3020 increments the address that it will assert on HD0-9 by one for each INCR ADRS pulse. The microprocessor loads an initial address and the address register outputs are applied to tri-state buffers. Then, the 10 bits of address from the counters are buffered. Those signals are multiplexed onto the HD (horizontal display) lines and R/W (read/write) line to the memories. These buffers are enabled only during the bus grant portion of the cycle for display of memory data.

At all other times, horizontal control circuit U5020 outputs control the HD lines to determine the memory address for update of memory data.

U3020 controls and subdivides the addresses assigned to digital storage. The Vertical Digital Storage board responds to addresses 7A, 7B, and FA. The Horizontal Digital Storage board responds to addresses 7A, 7B, FA, and FB. The DV (Data Valid) line (which clocks data to or from the microprocessor from the instrument data bus) goes to U3020, which sends a controlled version of this line, VDV, to the Vertical Digital Storage board. When the addresses on the Vertical Digital Storage board are to be addressed, this line is active and none of the addresses on the Horizontal Digital

Storage board are affected. When the addresses on the Horizontal board are to be accessed, VDV is held low by U3020 regardless of DV.

Address 7A on the Horizontal board is further subdivided into 7A.0 through 7A.7 by three bits of 7B on the Horizontal Digital Storage board. Access to these addresses is passed between the two boards by U3020. Reading from address FB will give access to the Horizontal board regardless of which previously had access. Sending the bits to 7B on the Horizontal board to access 7A.6 (DB6–4= 110) will pass access to the Vertical board. Sending DB6,5=11 to 7A.5 of the Horizontal board will also pass access to the Vertical board. Sending DB6,5=10 to 7A.5 of the Horizontal board will pass access to the Vertical board, but only for one DV cycle.

Tracking Digital-to-Analog Converter. The 10-bit digital-to-analog converter operates as part of the loop that acquires a binary equivalent of the SWP (sweep) input signal from the Sweep board. Converter U4040 accepts the output from the 10-bit up/down counter of U5020 and converts that output to an analog current. The analog current is then subtracted from the SWP signal (which is applied at edge connector pin 60 through buffer U6060B). The result of this subtraction is supplied to up and down comparators in U3050. This creates the UP or DOWN signal, as appropriate, to control the count direction of the 10-bit up/down counter in U5020. The counter then counts in the appropriate direction, which changes the digital-to-analog converter output to reflect the proper value.

Update Marker Circuits. These circuits create a cursor to show the present update location while a digital storage display refreshes. The cursor is made by stopping the sweep for a short period, allowing the crt phosphors to brighten at that spot. This occurs at each of the 500 digital storage sweep positions. The resulting display appears as a bright dot sweeping across the crt, rising and falling with the signal.

The basic circuits consist of a set of latches, a digital-to-analog converter, a comparator, a pulse generator, and control circuitry. The Horizontal Display (HD) data represents the digital equivalent of the present update position. The latches capture the data, and the digital-to-analog converter (dac) converts it, creating the analog horizontal deflection signal. When the sweep voltage reaches the dac level, the sweep stops for a longer period of time, and therefore the crt is brighter, than at other sweep positions. On the next sweep, the HD data increments to the next position, moving the cursor along the sweep.

The DSPL EN (Display Enable) signal clocks the HD (Horizontal Data) signals into latches U1020 and U2030. The latch outputs drive U2020, a 10-bit digital-to-analog converter. The converter's output current drives operational amplifier U6060A, producing a voltage called HORIZ SIG. When a digital storage signal is displayed, HORIZ SIG drives the horizontal Deflection Amplifier.

Also, U4060 compares HORIZ SIG to the sweep voltage from U6060B. The comparator output drives the "Update Intensity" input on the Marker IC, U3020. The Marker IC generates a 16-unit pulse, clocked by DSPL EN. The rising edge of U3020's output pulse produces the INTENSITY signal that temporarily prevents counting by the 9-bit display counter in U5020. This effectively stops the beam for a short time and causes a bright spot (cursor) on the trace to indicate the horizontal point being updated.

Memories. Integrated circuits U4010 and U5010 provide 8K bits of random access memory for storage of the 1000 data points used in the digital storage system. Addressing during bus transfer of memory data is controlled by address tri-state buffers on HD 9-0 pins of U3020 and by horizontal control IC U2035 during memory update.

DEFLECTION AMPLIFIERS (Diagram 24)

The Deflection Amplifier receives vertical signal information from the vertical section of Digital Storage or the Video Processor, and horizontal or sweep voltage from the horizontal section of Digital Storage or the Sweep board. Readout data for the display comes from the Crt Readout circuits. The output of the Deflection Amplifier drives the crt deflection plates. The amplifiers contain the switching circuits necessary to perform the selection functions and they also contain the amplifier stages needed to produce the deflection plate drive signals.

Horizontal Section

Signal lines HORIZONTAL SIGNAL (from the digital storage circuits through edge connector pin 49) and SWEEP (from the Sweep circuit through edge connector pin 51) are applied to switch IC U7055A. U7055, under control of the STORAGE OFF signal (from the digital storage circuits through edge connector pin 7), selects either the HORIZONTAL SIGNAL or SWEEP input. The SWEEP signal is selected when the STORAGE OFF line

is floating or pulled high. The HORIZONTAL SIGNAL is selected when the line is pulled low. Resistive divider R7051 and R7081 reduces the selected signal from 1 V/div to 0.5 V/div. U7073 buffers the selected signal. It goes out to the HORIZ OUT rear-panel connector via edge connector pin 48. U7073 applies the signal to switch U7055B. The HORIZ R/O signal, from the Crt Readout circuits, is also applied to U7055B. The R/O OFF signal, from the Crt Readout circuits selects between these two signals. When R/O OFF is floating or pulled high, the switch transmits the signal from buffer U7073 to the shaper. When the line is pulled low, it selects the HORIZONTAL R/O signal.

U7055B applies the signal to a shaper network to compensate for non-linearity in the crt deflection characteristics. This network consists of resistors R5059, R5058, R5057, R5062, R4061, and R4059, plus diodes CR1012, CR4051, CR4058, and CR4056. The HORIZONTAL POSITION voltage, from the front panel via edge connector pin 47, through resistor R6032, is applied to the shaper circuit so the shape correction factor relates to the crt deflection.

The shaped signal is then applied through preamplifier U2060 to the deflection amplifier circuits. Horiz Gain adjustment R1055, calibrates the amount of gain compensation required for proper deflection sensitivity.

The horizontal deflection amplifier consists of two circuits similar to each other, one for each horizontal deflection plate. One circuit is an inverting amplifier, the other operates in-phase. Inputs to Q4038A of the inverting side are through the parallel combination of resistors R4049 and R4048 and capacitor C4057. The series connection of resistor R4048 and variable capacitor C4057 provides high-frequency response compensation. Capacitor C2047 controls high-frequency feedback.

Input to the non-inverting side is through resistor R5029 to the base of Q4025A. R4019 and R5035 set the dc level for the feedback loop to the base of Q4025B. Variable capacitor C5021 provides adjustment to set transient gain. High-frequency feedback is controlled by capacitor C3021.

Gain of each amplifier section is approximately 20. (Horizontal deflection sensitivity of the crt is approximately 21.3 V/div per side.) Each section is single-ended and incorporates a gain- degenerated dual PNP transistor at the input side (for temperature compensation) connected as a differential amplifier. For example, Q4038B of the right deflection amplifier drives emitter follower Q4047.

Signals with a low rate of change drive the output transistor through R5037 and P3033. As the rate of rise increases, the drop across R5037 increases and when it reaches 0.6 V, either Q4035 or Q4042 are biased on. These transistors provide the high current drive for the output transistors. When the signal rate of change is low, Q1043 drives the crt deflection plate and Q1049 provides bias current for the amplifier. As the rate of rise increases, C3039 couples the signal to the base of Q1049. Q1049 provides the positive drive to the deflection plate, and Q1043 provides the negative drive. Each output transistor can provide a 200 V excursion in approximately 1 μs.

The horizontal amplifiers operate with approximately 1 mA of bias current in the output stage, as set by the current through resistor R3031, R1052, and R1049 at the base and emitter of Q1049. Current through resistor R3031 also provides the current for the input stage, Q4038A/Q4038B. Emitter follower Q4047, operates at approximately 2.5 mA. Resistors R1045 and R1034, in the emitter circuit of Q1049 and Q1043, degenerate the output stage for fast steps. Current from the −15 V source through resistor R4033, sets the output operating level. Feedback resistor R3045 sets this output level at approximately 142 V.

Operation of the right-hand (inverting) section is basically the same as the left-hand (non-inverting) section.

Vertical Section

VIDEO FILTER OUT, from the Video Processor, and VERTICAL SIGNAL, from the Digital Storage, are routed through switch IC U6055A, under control of the STORAGE OFF signal from the Digital Storage board. Note that the VIDEO FILTER OUT signal is buffered by IC U7065 to prevent a change in load transients from affecting the signal level. A high on the STORAGE OFF line selects the buffered VIDEO FILTER OUT signal, and a low selects the VERTICAL SIGNAL. U6065 inverts the selected signal and clamps it to ground. Both the VIDEO FILTER OUT and the VERTICAL SIGNAL are specified at 0.5 V/div with 0 V for the baseline and positive voltages above the baseline.

The signal is re-inverted and offset by buffer U6073 so center screen represents 0 V. Buffer U6073 supplies a sample of this centered signal to the rear-panel VERT OUT connector via edge connector pin 46. The output of U6073 is also applied through switch U6055B, when the R/O OFF line is high, to the vertical shaper circuit. When R/O OFF line is low, the VERTICAL R/O signal is applied to the shaper.

The vertical section shaper (R4062, R4065, R4067, R4069, R4064, and CR4063, CR4064, plus the preamplifier U2062) operates the same as the horizontal section. Q4078 limits positive excursions to approximately one division above the top of the screen to protect the output stages from being overdriven.

The vertical output stages are similar to the horizontal stages, with the exception of higher bias current. Current flow of approximately 1 mA, through resistors R3089 and R3098, produces approximately 5 mA in the output stages. To correct for the increased current in the dual input stage transistors, Q4083 and Q4101, resistors R5081 and R5099 are lower value than their counterparts R5041 and R5027 in the horizontal amplifier.

U6024 compares the signal level from the baseline clamp, U6065, with a reference level set by divider R7032/R7034. This produces the CLIP signal for the Z-Axis interface circuits. When the VIDEO FILTER OUT signal is more negative than the reference level (approximately 1 division above baseline), it pulls the CLIP line low. R7021 pulls the CLIP line high if the signal is more positive than the reference level.

Z-AXIS AND RF INTERFACE (DIAGRAM 25)

The Z-Axis and RF Interface board contains the RF interface circuits, crt Z-axis drive circuits, power monitor circuits, and a timer that measures operational hours. This board provides beam intensity (nominally from the front panel), baseline clipping, and unblanking logic for the signals or readout data. Unblanking logic comes from the Sweep board, the Crt Readout, the Deflection Amplifiers, and the Digital Storage. The RF Interface circuits receive data from the microcomputer that controls the RF Attenuation, transfer switch, and IF selection. A power fail circuit on the board detects any change in input power frequency or power supply voltage and notifies the microcomputer. An elapsed time meter is also located on the board to give a indication of total instrument operating time.

RF Interface Circuits

The RF interface includes the digital control circuits that receive the address and instruction data from the microcomputer and decode it to control the RF Attenuator, Transfer Switch, and IF selection. The power supplies that are required to drive the attenuator and switches are also included.

Digital Control. Address decoder U2045 latches the data at the input of U3046 whenever the microcomputer selects address 4F. Table 7-5 lists the purpose of each data line from the buffer.

When Q4 of U3046 goes low, Q2025 and Q3028 conduct. This raises the Vcc of attenuator drivers U3034, U3029, and U3038 to +16 V for approximately 100 ms to energize the attenuator solenoids. A diode protects each attenuator driver output line from the inductive voltage surge that occurs when the solenoids change state.

Table 7-5
RF INTERFACE LINES

Line	Purpose
Q1	Enables 10 dB attenuator
Q2	No connection
Q3	Enables 30 dB attenuator
Q4	Enables current drivers Q2025 and Q3028
Q5	Enables transfer switch driver
Q6	Selects 829 MHz IF (high state) or 2072 MHz IF (low state)
Q7	Enables 20 dB attenuator
Q8	Enables baseline clipping

Transfer Switch. Operation of the Transfer Switch is dependent on the output of Q3025/Q3024. The Q5 output of U3046 is applied to the input of operational amplifier U4023, which drives differential amplifier Q2025/Q3024. When Q5 goes high, Q3025 is biased on and the Transfer Switch selects the external mixer. When Q5 goes low, Q3024 is biased on, and the internal mixer is selected. Diodes CR3018 and CR3017 protect the transistors from voltage spikes induced when the Transfer Switch changes state.

Z-Axis Circuits

The Z-Axis circuits provide the drive currents and bias voltage to operate the crt. They consist of the intensity control logic circuits, which control the crt beam current for normal signal display operations, and the unblanking gates, which furnish current to the Z-Axis drive amplifier to drive the crt control grid.

Z-Axis Drive Amplifier. The Z-Axis Drive Amplifier is an operational amplifier that consists of transistors Q3047, Q4058, and Q4059, and related components. R1050 is the input resistance for the amplifier, and R2066 is the feedback resistor. The output is clamped by diodes CR3059 and CR3066 to protect the amplifier from transient surges in case of crt arcing. The amplifier is driven by two sources, exclusive of each other; U2038B/Q2042 drives the amplifier during readout display periods, and U2038A/Q2044 drives the amplifier during sweep display periods. U2039 is an AND-NOR gate that provides the logic to one input of NAND gate U2038A to turn Q2044 on or off. The R/O OFF line and the output of U2039 must both be high for U2038A to furnish current to Q2044. Table 7-6 lists the conditions under which U2039 will output a high to U2038A.

Table 7-6
U2039 TRUTH TABLE

Signal	Condition
U3046 output (line Q8)	0 0 0 1 1 1 0 0 0
CLIP	0 0 0 0 0 0 1 1 1
Z-Axis Blank	1 1 1 1 1 1 1 1 1
Storage Off	0 0 1 0 0 1 0 0 1
SWP GATE	1 0 1 1 0 1 1 0 1
U2034, pin 10	0 0 0 0 0 0 0 0 0

Only the combinations shown in Table 7-6 plus a high on the R/O OFF line will gate a low out of U2038A. When the U2038A output is low, emitter current is furnished to Q2044, which in turn furnishes current through R1050 (the input resistance of the Z-Axis drive amplifier) to Q3047. U2034B is a single-shot multivibrator that produces a 3 μs pulse to blank the crt beam during trace return, between readout and signal display.

The other source of input current to the Z-Axis drive amplifier is Q2042. This transistor is turned on by U2038B when R/O UNBLANK is high and R/O OFF is low.

Q1028 is the current source for divider R1030/R1025 that establishes the operating point for Q2042 and Q2044, which sets the intensity level. Diodes CR1045 and CR1043, connected from the base of Q2042 and Q2044 to the emitter of Q2022, limit the display intensity. These diodes prevent the bases from going more positive than approximately 0.6 V above the emitter voltage of Q2022. This circuit, which includes Int Limit adjustment R1027, sets the maximum current for both Q2042 and Q2044.

Transistors Q1017 and Q1015 provide current for the trace rotation coil. Trace Rotation adjustment R1021 sets the current so the displayed trace is aligned with the graticule.

Power-Fail Detector

This circuit detects an instrument power failure and transmits the information to the Processor and Memory boards. The LINE TRIGGER signal from the Power Supply board through edge connector pin 60 is supplied to Q2011. Q2011 buffers the signal and applies it to the input of retriggerable one-shot U2034A. U2034A performs as a missing- pulse detector to generate a power-fail signal through Q3011 to notify the Processor and Memory boards if more than two 60 Hz cycles are dropped. To avoid an undefined state, the output from U2034A is latched low by U2051. Under normal operating conditions, the POWER-FAIL signal from Q3011 is high.

Power-Supply Monitor

This circuit detects if one or more of the instrument power supplies have failed. Each voltage supply in the instrument is fed into thick film resistor network R3051, which balances the currents to provide a null output (approximately 1 Vdc). Any line change of more than ±25% drives the input to window comparator U3051 beyond its ±200 mV threshold and generates a low output. Q2059 and Q2067 drive the dual light emitting diode DS1062 to provide visual indication of power-supply status (green indicates normal operation and red indicates a fault condition). The output of U3051 is also fed to tri-state buffer U3052. After instrument power up or if a failure is detected, the microprocessor will poll address CF to determine power- supply status over the data bus.

Timer

An electromechanical timer, M1019, is calibrated for a duration of 5000 operating hours. The current through R1015 and the timer causes the copper band to progress along the scale.

HIGH-VOLTAGE SUPPLY (DIAGRAM 26)

The High-Voltage Supply furnishes the -3860 V crt bias and 6.3Vac filament voltage to the crt cathode, and provides dc restoration for the Z-AXIS DRIVE signal. The supply consists of the following four main circuits:

- High-Voltage Oscillator
- Voltage Doubler
- High-Voltage Regulator
- Z-Axis Clipper

High-Voltage Oscillator

This circuit consists of transistor Q1073, transformer T2065, and associated components. The approximately 200 Vac, oscillator output is coupled across T2065, where it is stepped up for application to the voltage doubler, and stepped down for application to the crt filament.

Voltage Doubler

The voltage doubler consists of CR4041, CR4035, C4027, C5021, C4024, R3038, and R1039. The output of the doubler is taken off the anode of CR4035 and applied to the crt cathode through the filter consisting of R3038, R1039, and C4024. Reference voltage for the

regulator is also taken off the end of R1039. R1039 keeps the filament at the same potential as the cathode.

High-Voltage Regulator

This circuit consists of amplifier U4083 and surrounding components. The high voltage is applied through a voltage divider that consists of R1017B and R1017C. This voltage divider is connected through R1042 to +15 V. The sample of the high voltage at pin U is applied through R4075 to the input of comparator U4083. The correction signal, in the form of dc drive, is applied as bias to Q1073 to set the oscillator current.

CR4078 and CR4077 at the input to U4083, protect the input against excessive voltage excursions. The high-voltage oscillator is protected by CR4071, R3079, and R4074 in case the +100 V supply should fail. Normally, CR4071 is back biased. If the +100 V is not present, CR4071 conducts and clamps the input negative; the output of U4083 swings negative and Q1073 remains cut off. This circuit ensures that Q1073 will begin to oscillate only after the 100 V supply reaches a voltage sufficient to sustain oscillation. CR3077 (in the regulator output circuit) protects the base of Q1073 from excessive negative voltage.

Z-Axis Clipper

This circuit consists of diodes CR1056 and CR1046, plus associated components. The 225 Vac from pin 8 of T2065 is coupled through C1058 and R1048 to the junction of CR1046 and CR1056. The regulator circuit, that consists of VR1041, R2050, R2040, and Q2048 holds holds the cathode of CR1046 at approximately +100 V to 143 V, depending on the setting of R2040. CR1046 and CR1056 clip the incoming 225 Vac to a total excursion of [$V_{CR1046\ cathode} - V_{Z\ AXIS\ DRIVE}$ +1.2V). R2040 is adjusted to completely cut-off the crt with Z-Axis DRIVE at minimum. The voltage that passes the clipper circuit is coupled through C1031 to the Z-Axis rectifier.

The clipped Z-AXIS DRIVE signal is rectified by CR2044 and CR2046, which are the principle components of the second section of the Z-Axis circuit. The rectified voltage is then fed to the grid of the crt. C1041 couples the fast changes of drive voltage to the crt grid to speed up the response of the grid circuit. The crt grid is protected from high-voltage arcs by neons DS2052, DS2054, and DS2057. R1043 protects CR2046 and CR2044, respectively, from high-voltage surges if the crt should arc.

CRT READOUT (DIAGRAM 27)

The Crt Readout assembly stores readout characters and generates deflection and Z-Axis signals to display those characters. It also handles the frequency dot marker display. Both characters and frequency dot displays are time-shared with the spectrum trace.

Generating Readout

Crt readout is handled by sequential logic, clocked at 3.41MHz, supplied by the Processor board. The readout circuitry (Figure 7-13) is composed of the following elements.

- Readout On Timing — RAM for character storage.
- Character Counter — to access the RAM and control the scan.
- Character Generator — to unblank the crt beam.
- D/A Converters — to deflect the crt beam.
- Instrument Bus Interface — to store characters and control the display.

Forty characters can be displayed per line, with up to sixteen lines selected. Normally, up to three lines are displayed while simultaneously displaying the spectrum. When over three lines are to be displayed, the spectrum display is disabled to keep the readout refresh rate above 60 Hz.

Readout-On/Off Timing. Characters are written one at a time. This allows a portion of the spectrum to be drawn between each character. The character duty cycle is between 10% and 25% because it varies with the character drawn. The time sharing between character writing and spectrum display is pseudorandom to reduce the effect of gaps in the spectrum display by moving them on the trace.

The readout-off time is set to 140 μs by one-shot multivibrator U1055 (Figure 7-14). Flip-flop U1041B asserts GEN RUNNING after U1055 times out, allowing a character to be drawn. After a character is written, ROW 0 COL 0 resets the flip-flop, which clocks off time one-shot U1055. The ON control bit must have been asserted by the microcomputer to get readout (as described under Instrument Bus Interface later in this section).

If BLANK (MSB of the character data) is not set, the GEN RUNNING flip-flop unasserts R/O OFF through OR gate U2044B; this switches the readout deflection signals for the deflection amplifier inputs.

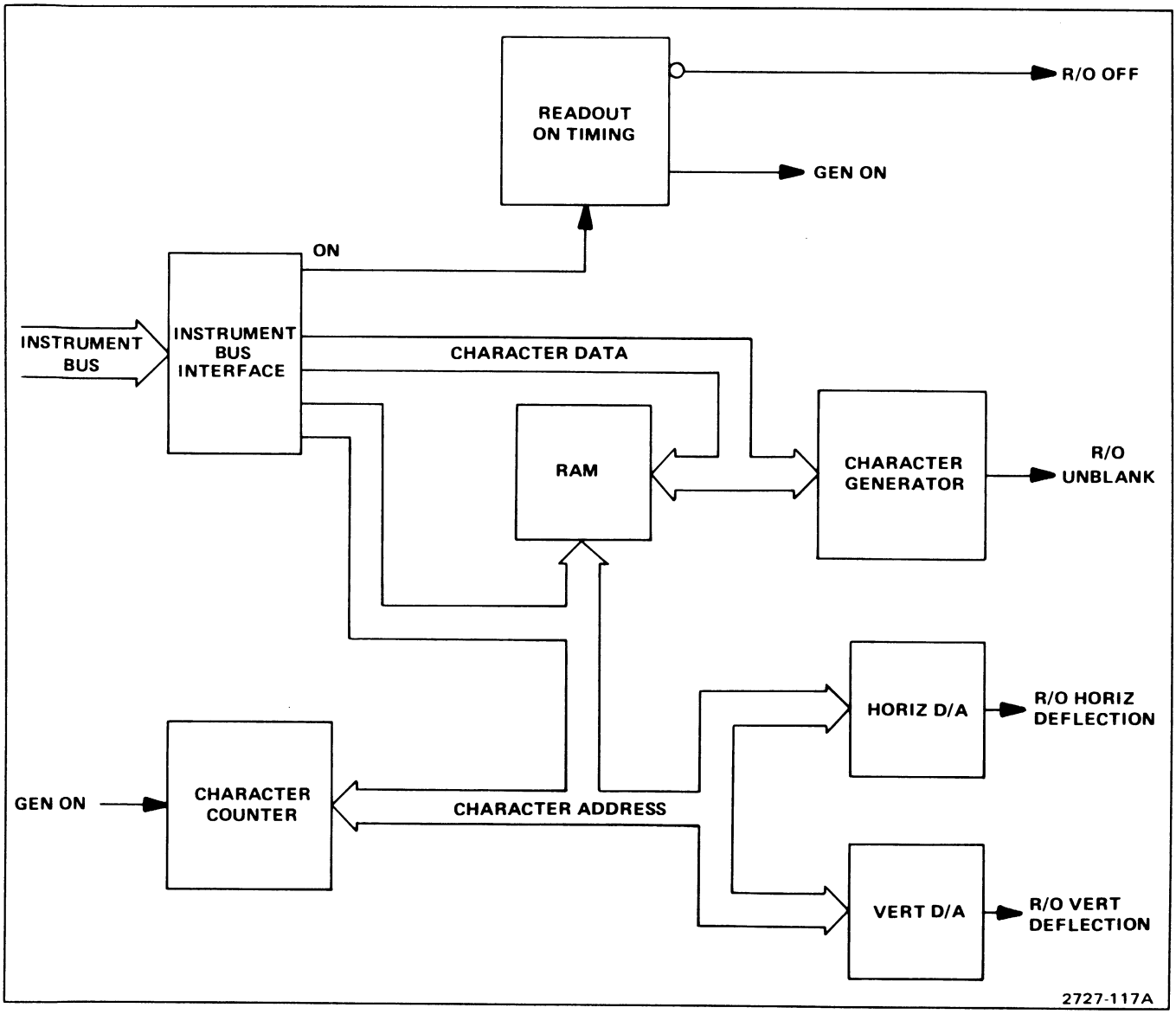


Figure 7-13. Block diagram of crt readout.

BLANK can be set by the microcomputer to load a space into the character RAM so the readout does not use time for the spectrum trace to scan a blank character.

Character Scan. Although the 8678 character generator IC, U2048, is often used in raster scans, in this application it is used to write complete characters, as shown in Figure 7-15. A character is drawn as a pattern of dots in an 8 x 8 matrix where the top row and first three columns are blank. These blank dots allow for beam retrace and spacing. The idle position between characters is indicated on the figure.

Character counters synchronize the horizontal and vertical scan with the Z-Axis signal from the character generator IC to draw the character. These counters, U2022, U2018, U2026, and U2014, divide by 8 for the columns within a character (columns A, B, C), divide by 8 for the rows within a character (rows A, B, C), divide by 40 for the characters within a line (characters A, B, C, D, E, F), and divide by 16 for the lines within a display. The counters are enabled only when the generator has control of the crt beam (GEN RUNNING line asserted) and INCR (increment) is high (when INCR is low, the crt beam is stopped to write a dot on the crt).

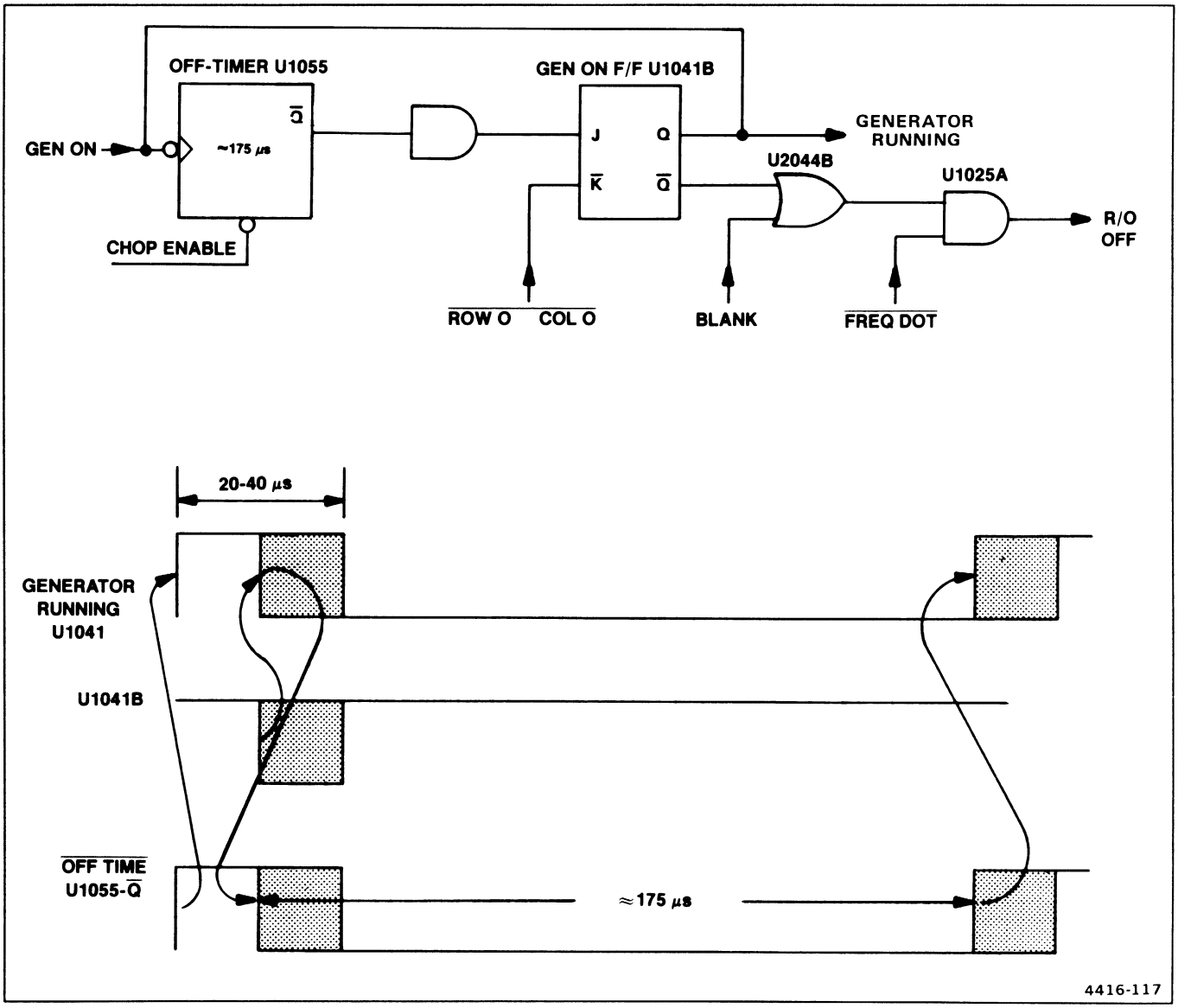


Figure 7-14. Character on/off timing.

The SKIP line from U2052 permits software control of the allowable states of line counter U2014. By placing a one in this bit of a character, the line counter is allowed to count up to the next state. This will continue until a character is encountered with the skip bit set to zero. This allows the addition of a third line to the normal two-line readout for status messages, by operating with the circuit normally in the 16-line mode (all but the bottom and top lines start with a readout character of 40 hex, which has the SKIP line set high). Thus, all but the bottom and top lines are skipped. When large messages are to be displayed, the SKIP line is set low for all characters and 16 lines are displayed.

The counters are wired to force the D/A converters to step through the character horizontally, a row at a time. At the same time, the pattern of dots is accessed under the control of the timing decoder logic, U2039B and U2031. The AND gate and decoder combine to control the character generator, U2048, which generates the correct pattern of blanking to draw the pattern of dots for the character. U2048, the 8678 character generator IC (Figure 7-16) contains a ROM with the correct pattern of 64 bits for each of the 64 characters in its repertoire. The bit patterns are accessed by a decoder that operates on the ASCII code on the character generator inputs. The pattern of bits is multiplexed, one 8-bit line at a time, into a shift register that is clocked out one bit at a time to control the crt Z-axis.

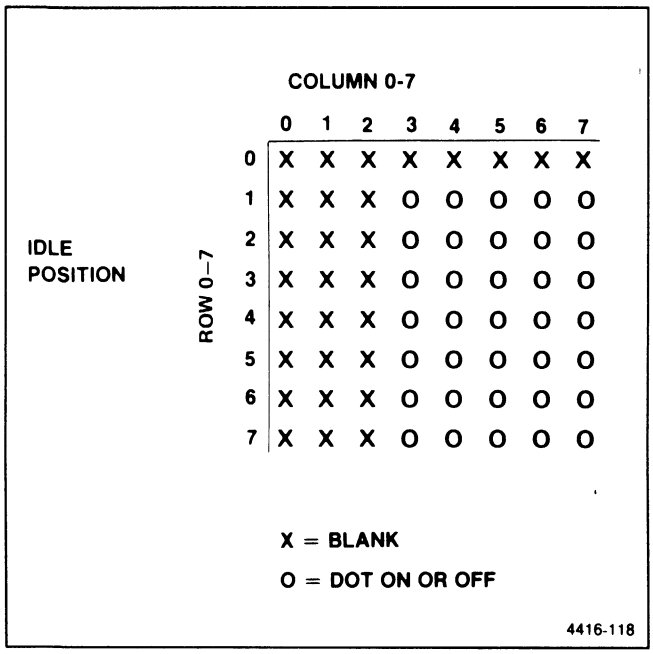


Figure 7-15. Character scan.

Character Generator Timing. The character generator timing lines are called DOT, LINE CLK, LE, and CLR. Each cycle of DOT clocks one dot (bit) out of the shift register. A positive transition on LINE CLK switches the next line (row) of dots onto the shift register inputs; the dots are latched by a negative transition on LE (load enable), setting up the shift register to display another row of dots. CLR resets the line counter to begin drawing another character.

GEN RUNNING, INCR, and CRT CLK are combined through AND gate U1037B to generate DOT to clock the character generator, U2048. Inversion by the gate restores the phase relationship of the DOT input and the inverted LINE CLK. LE is gated by U2039B when the character counter reaches column 2. This loads the shift register with the next row of dots, which is displayed starting at column 3. LINE CLK advances the line (row) counter after the scan of the current row begins to set up the next row of dots on the shift register inputs; this occurs at column count 4. Decoder U2031 outputs a ROW 1 COL 1 when the character counter reaches row 1, column 1 (the first non-blank row of dots scanned in each character). This is asserted once during the scan of each character.

The sequence of events to scan a character is illustrated in the character timing diagram (Figure 7-17). At 1, the character generator finishes a character. Then, when the counter advances, decoder U2031 asserts ROW 0 COL 0, resetting the GEN RUNNING flip-flop, U1041B, on the next clock. This stops the counter at row 0, column 1 (2 on the figure). When readout-off time one-shot U1055 completes the time-out period, it allows the GEN RUNNING flip-flop to be set. Just before the scan enters the actual character clock area (at 6), CLR resets the character generator line counter (at 5). LE (at 5a) loads one row of dots into the output shift register so that the first dot is output at 6. The break (7 on the figure) indicates that the scan continues. After the character is scanned, the scan returns to the idle state; 8 and 9 correspond to 1 and 2 on the timing figure.

Dot Delay. Each bit shifted out of the character generator is the value of a dot in the 5 x 7 character matrix; 0 for a blank and 1 for a dot that is to be written. As the scan progresses at 3.4133 MHz, a faint character display might be expected. To brighten the dots that are written, a shift register is used as a delay element so that dots are displayed and counters disabled for 3 clock cycles.

Assume that no dots have been displayed for several dot clock cycles, so the output of the character generator, pin 11 of U2048, is low. Thus, U1020B output is high, and the outputs of the delay shift register U1025C and U1020B are low. When a dot is displayed, the character generator output (pin 11 of U2048) goes high. This causes INCR to go low and disable the counters. It also causes the input to the delay shift register, pin 11 of U1020B, to go high. On the next clock pulse, U1020A output follows INCR and goes low. The shift register clocks the one in, and the unblank flip-flop, U1016B, goes high, turning the crt beam on. This is the only "1" it will clock in, because the output of U1020A is now low. The circuit is now in a lock-up state with the counters disabled. Two more clock cycles will go by until the "1" in the shift register is clocked out, allowing the output of U1033C to go high. A high on the output of U1033C starts the counters again and resets unblank flip-flop U1041A.

Instrument Bus Interface

The microcomputer controls the crt readout and frequency marker dot over the instrument bus through the following ports.

Port	Hex Address
Control/Address	5F
Address/Data	2F

Decoder U3051 asserts 5F when it sees a value of 5 on the upper four bits of the instrument bus address lines, and 2F when it sees a value of 2. The decoder must be enabled by DATA VALID high on the instrument bus. The false transition of DATA VALID causes the addressed port to latch the data on the instrument bus.

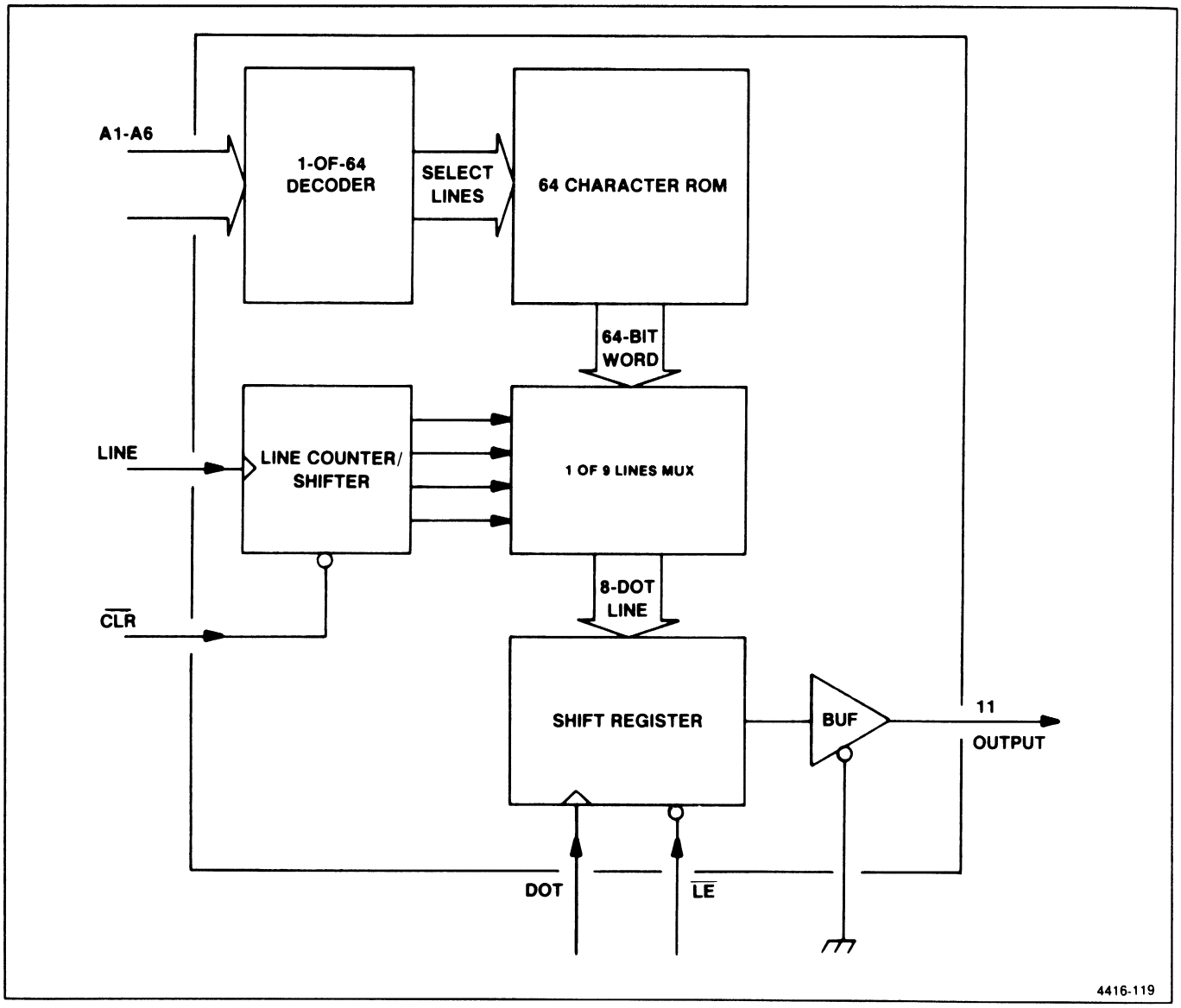


Figure 7-16. Character generator block diagram.

Control Port. Control address port U3034 turns the readout on or off, steers data sent to the address/data port, controls the mode of the frequency marker dot, and contains two bits of the RAM address. The bits are defined in Table 7-7. Bit numbering on the instrument bus starts at zero. However, the D and Q pins of U3034 (and some other ICs) are numbered starting at one, following the manufacturers data.

Table 7-7
CONTROL PORT

Bit	Function
0	Readout on/off
1	Address/data
2	A9 of RAM address
3	Max Span dot
4	A8 of RAM address
5	16 line mode
6	40 characters/line
7	Spectrum display available

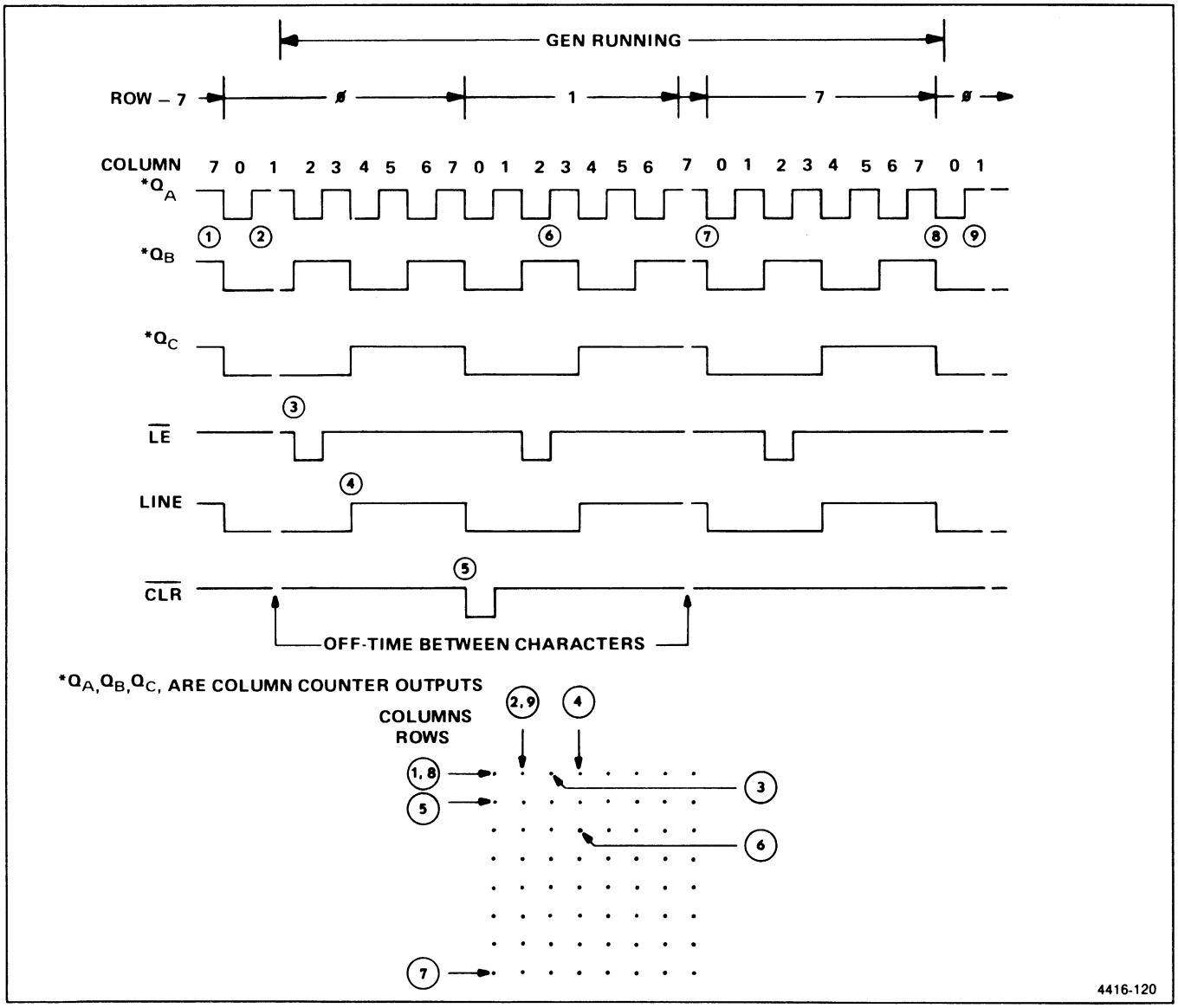


Figure 7-17. Character timing diagram.

Bit 0 turns the crt readout display on (1) or off (0). When set, this bit releases CLEAR from the GEN RUNNING flip-flop and allows the off timer, U1055, to set U1041B. Also, when the ON/OFF line goes high, it enables the INCR gate, U1037C, to steer the position counter onto the character RAM address inputs through line driver U3042 and multiplexers U1050 and U1046. When cleared, this bit places an address, latched in U3038 and U3034, on the character RAM address inputs.

Bit 1 interprets data sent to the address/data port as an address (1) or data (0) for the character RAM. Setting this bit disables the character RAM for input and sets up the clock signal to latch the address.

When this bit is set, Q8 of U3034 gates a high on the output of U2044A. This high prevents input to the character RAMs, U2057 and U2052, by setting its R/W input high. This high also disconnects the instrument bus from the character RAM data inputs by disabling U3047; meanwhile, U2037A is enabled to gate the clock signal that latches the address. The positive clock transition is applied to U3038 when DATA VALID goes false at the end of a write cycle to the address/data port, releasing 2F.

When this bit is cleared and 2F is asserted, U2044A enables the character RAM for input and passes the data through U3047.

Bit 2 is the MSB of the RAM address.

Bit 3 controls the frequency dot marker. This bit is set in the MAX SPAN mode to position the frequency dot with MAX DOT CONTROL from the Sweep board. When cleared, this bit centers the frequency dot on the spectrum display.

Bit 4 is the A8 address line for the character RAMs.

Bit 5 is the select for 16 lines mode.

Bit 6 selects the 40 character/line mode.

Bit 7 enables the clipped display with the spectrum. When high, U1055 is enabled and causes 140 μs periods to occur between characters when the spectrum is disabled. When low, U1055 is disabled, R/O OFF is forced low to disable the spectrum display, and W1028E forces the current boost addition to be disabled. Also, U1016 is disabled so that the marker dot is not displayed.

Address/Data Port. The microcomputer loads characters for crt display through the address/data port. Each character requires the following four write cycles.

1. Bit 2 in the control port is set for an address transfer, and the upper 2 bits of the RAM address (A8, A9) are sent.

2. The lower 8 bits of the address in the character RAM are sent to the address/data port.

3. Bit 2 in the control port is cleared.

4. The data is sent to the address/data port. The bits are defined in Table 7-8. Bits 0-5 are the lower six bits of the character RAM address or are the ASCII code for the character.

Table 7-8
ADDRESS/DATA PORT

Bit	Function
0-5	Address of ASCII code
6	Skip bit
7	Blank character

Bit 6 causes the line counter, U2014, to skip a line, if set.

Bit 7 is used to reduce overhead readout display. It is set when a space is transferred to the character RAM, so the readout does not steal time from the spectrum trace to scan a blank. When set, this bit prevents the GEN RUNNING flip-flop from gating R/O OFF low through U2044B.

Frequency Dot Marker

The frequency dot marker is refreshed immediately after the last character position in the lower readout is scanned. Normally, the marker is centered on the screen just below the upper readout as a pointer for the center frequency readout. When MAX SPAN is selected, however, the dot marker moves to a point on the display that corresponds to the center frequency value.

The negative transition of line D triggers the marker generator. A simplified diagram of the circuit and its timing is shown in Figure 7-18.

U1016A delays the marker dot to allow retrace while gating DOT INV low to set up the display. DOT INV affects the readout deflection outputs in the following ways.

1. The horizontal output is connected either to ground, for a center-screen dot, or MAX DOT CONTROL, for a max span pointer. MAX DOT CONTROL is proportional to the center-frequency readout offset from the center of the frequency range.

2. The U1025B output goes low during the dot interval to cause Q3018 to insert an offset current into the vertical output, to shift the dot position down on the screen.

3. R/O OFF is gated low to switch the deflection amplifier inputs from the Trace Mode to the Readout Mode, using the marker dot horizontal and vertical signals.

When the retrace one-shot times out after about 5.9 μs, it's Q line triggers the unblanking one-shot U1016B, which sets R/O UNBLANK high for 5 μs, via DISPLAY MKR DOT through U1037A. This refreshes the dot. DISPLAY MKR DOT also holds DOT INTVL low through CR1013, until the dot marker is drawn. R1015 and C1011 slow the rise of DOT INTVL to prevent a spurious signal through the "diode AND" gate.

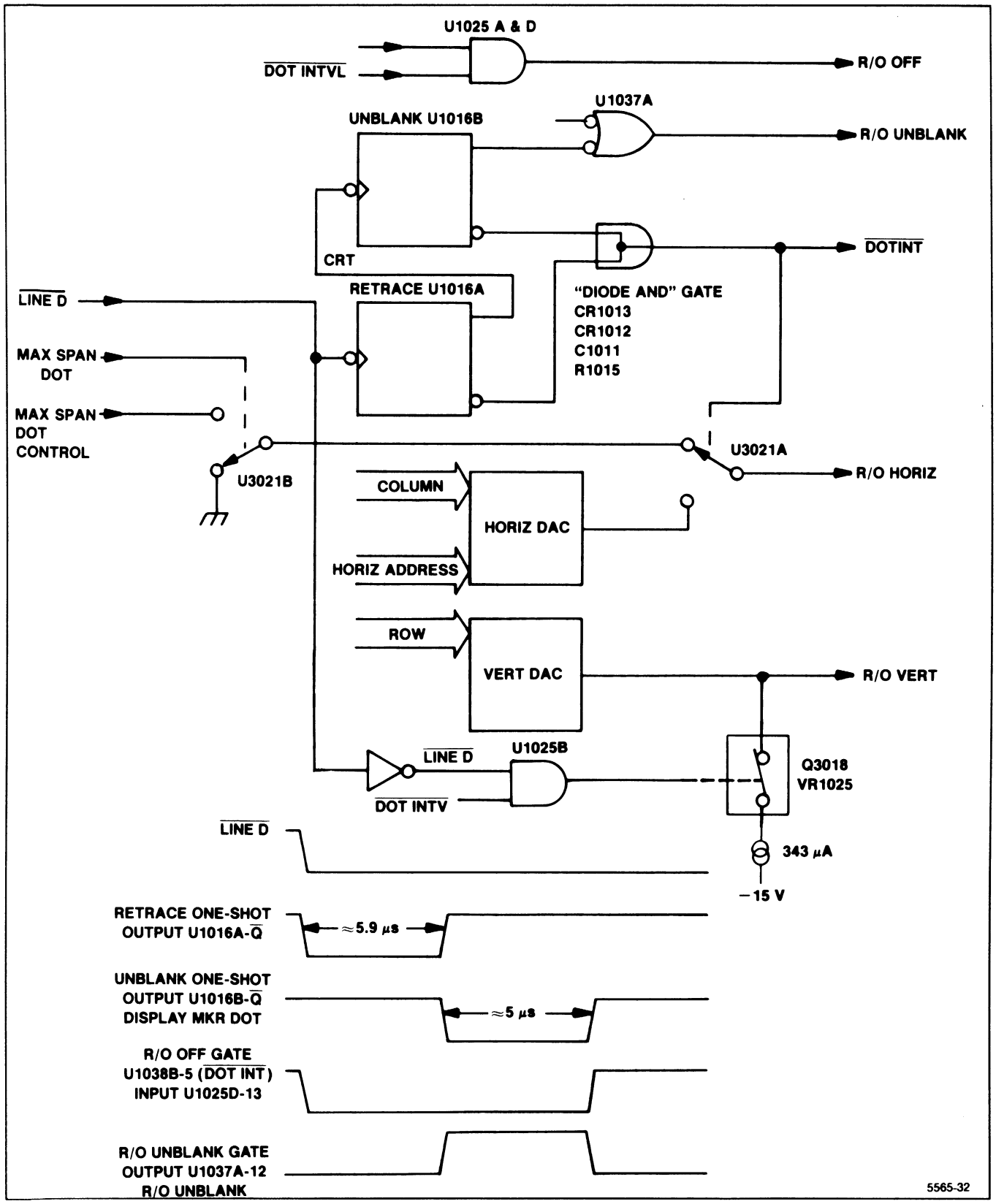


Figure 7-18. Frequency dot marker simplified diagram with timing waveforms.

FREQUENCY CONTROL SECTION (Diagram 6)

The Frequency Control section performs the tuning and scan function for the 1st LO and 2nd LO. It also provides the sweep voltage for the deflection amplifiers in the Display section so the crt display is coincident with the frequency scan and tuning. This section contains the following major circuits:

- Sweep
- Span Attenuator
- Center Frequency Control
- 1st LO Driver

Circuits on the Sweep board accept trigger inputs from line, internal and external sources, and the normal free-run mode of operation. They also receive external horizontal and manual sweep inputs. The circuits produce a PEN LIFT signal for chart recorder applications, a SWEEP GATE signal for crt display blanking, a SWEEP signal to drive the crt beam across the horizontal axis and drive the horizontal portion of the digital storage circuit, plus a ramp (OSC SWEEP) that is fed through the Span Attenuator to the 1st LO Driver and the 2nd LO. This circuit attenuates the ramp signal as required to sweep the frequency of the 1st and 2nd local oscillators.

The Center Frequency Control circuit provides a tuning voltage for the 1st and 2nd Local Oscillator circuits that results in a linear center frequency change as the front panel FREQUENCY control is changed. The circuit is directly controlled by the microcomputer, so remote control of the frequency is possible programmable instruments by way of the GPIB rear-panel connector. The COARSE TUNE VOLTS signal from this circuit is applied to the 1st LO Driver circuits for summing with the SPAN signal to drive the 1st LO. The FINE TUNE VOLTS signal is applied to the 2182 MHz Phase Locked 2nd LO circuit for summing with the 2nd LO SWEEP signal.

The 1st LO Driver combines the COARSE TUNE VOLTS signal with the SPAN signal and outputs a current to drive the 1st LO. This assembly also produces reference and supply voltages.

SWEEP (Diagram 28)

The circuits on the Sweep board (A72) provide the ramp voltage that drives the horizontal deflection amplifier, the 1st LO Driver, the 2nd LO, and a voltage used to align the frequency control system with the digital storage marker positions. The sweep board also provides signals for the Z-Axis circuitry, an external plotter pen, and digital storage.

The major circuits on the Sweep board are:

- Sweep Generator
- Trigger Circuits
- Sweep Control
- Digital Control
- Marker DAC

The sweep generator generates the voltage ramp that drives the Deflection Amplifiers, Digital Storage and the swept oscillators.

The trigger circuits process and multiplex the three trigger signals.

The sweep control circuit generates the SWEEP GATE and PEN LIFT signals and determines the holdoff time for the sweep generator.

The digital control circuits receive and decode the address and instructions from the microcomputer, select the sweep rate, holdoff time, trigger source, sweep mode, control marker dac, and control interrupts to the microcomputer.

The Marker DAC provides a dc level corresponding to the marker sweep position.

The Sweep board analog section consists of the ramp or sweep generator plus its output buffers that drive the deflection amplifiers, the oscillators, digital storage, Z axis, and the trigger circuits. The sweep and trigger circuits are digitally controlled.

Digital Control

Three instrument bus addresses are associated with the sweep board. Addresses 0F and 1F are write addresses and 9F is a read address. Two bits at address 1F subdivide address 0F into four subaddresses.

Bus decoder U4030 outputs lows for addresses 0F, 1F, and 9F. U4020 buffers the instrument bus data bits. U1027 is used as a 6-bit register to hold data at address 1F. Data bits 6 and 7 go to U1030 which decodes which of U1035, U2030, U1045, and U1040 are activated at address 0F by U4030. These registers store the microcomputers latest commands (except for the trigger single sweep and the abort sweep com-

mands, which are not stored) and they control most of the operation of the sweep board.

Commands that can be written are:

- Sweep start for single sweep mode (bit 3 of 1F high).
- Single sweep operation (bit 0 of 0F.0 high).
- Sweep rate selection (bits 0-4 of 0F.1, see Table 7-9).
- Internal frequency reference on or off (bit 4 of 1F low for on and high for off).

TABLE 7-9
SWEEP RATE SELECTION CODES

Sweep Rate	D4	D3	D2	D1	D0
20 μs/div	1	1	0	1	1
50	1	0	1	1	1
100	1	0	0	1	1
200	0	1	0	1	1
500	0	0	1	1	1
1 ms/div	0	0	0	1	1
2	1	1	0	0	1
5	1	0	1	0	1
10	1	0	0	0	1
20	0	1	0	0	1
50	0	0	1	0	1
100	0	0	0	0	1
200	1	1	0	0	0
500	1	0	1	0	0
1 s/div	1	0	0	0	0
2	0	1	0	0	0
5	0	0	1	0	0
10	0	0	0	0	0
Manual	1	1	1	1	1
External	0	1	1	1	1

Commands written to address 1F control the triggers and sweep holdoff time. These commands are as follows:

- Abort sweep (bit 0 of 1F goes high).
- Ignore input trigger signals (bit 1 of 1F high).
- Disable sweep gate and blank non-store display (bit 2 of 1F high).
- Trigger mode (controlled by bits 3 & 4 of 0F.0, see Table 7-10).
- Sweep holdoff time (bits 5 & 6 of 0F.0, see Table 7-11).
- Interrupt at end of sweep (Data Bus bit 4 goes low when the microprocessor does a POLL after it detects the interrupt, bit 1 of 0F.0 enables the end of sweep interrupt).

Table 7-10
TRIGGER SELECTION MODES

Trigger Mode	D4	D3
Free run	0	0
Internal	0	1
External	1	0
Line	1	1

Table 7-11
SWEEP HOLDOFF SELECTION

Sweep Holdoff	D4	D3
Short	0	0
Medium	0	1
Long	1	0

Sweep Generator

The sweep generator is an integrator circuit consisting of operational amplifier U1055 with one fixed and two switchable capacitors in the feedback circuit. Fixed capacitor C1061 is used for the faster sweep rates. The other two capacitors, C1065 or C1062, are added to change the time constant when either Q2068 or Q2064 are switched on by comparators U1060A or U2050A. These comparators are driven by register U2030, which interfaces to the instrument bus. For manual sweep operation, Q2060 is turned on and the integrator becomes an amplifier.

Multiplexer U3060 connects timing resistors between a −12 volt reference, out of U3050B, and the input to integrator U2060. Data bits D2, D3, and D4 of address 0F.1 drive the select inputs of the multiplexer. The voltage reference of −10 volts out of U4055 is boosted to −12 volts by U3050B. A voltage divider sets the non-inverting input of U1055 to −8 volts. Therefore, there is about 4 volts difference across the timing resistors. The timing current through the resistors varies over two decades such that 1/I is proportional to a 2-5-10 sequence.

Switching in feedback capacitors C1065 and C2060 each changes the sweep rate by a factor of 100 times. Sweep Accuracy adjustment, R1062, compensates for differences in timing voltage or timing circuit values. The timing capacitors are matched so that one adjustment compensates for small variations in each set.

Trigger Circuits

The sweep circuit can be triggered by an externally applied signal, the internal video filter signal, or from the power line. Each trigger signal is converted to TTL level and then applied to trigger multiplexer U2026, part of the trigger control circuit. The trigger control circuit selects the desired triggering signal and triggering mode or rejects the trigger to let the sweep circuit free run, be manually controlled, or let the external sweep mode be used.

An external trigger signal applied to the external HORIZ/TRIG connector is converted to TTL level by Q2030. CR2030 limits any voltage surges that may be on the line. Line trigger signals, from the power supply, are applied through comparator U3025A to the multiplexer. Video Filter Out signals from the Video Processor board are buffered by Q4037 and converted to TTL level by Q3030. Both the external and video trigger signals are applied to multiplexer U2026 through Schmitt trigger inverters in U1015C.

Under control of the data (D2 and D3) from register U1035 (at extended address 0 of address 0F), the multiplexer selects the trigger signal and passes it to flip-flop U1016B. After retrace and holdoff time, U1016B allows a trigger to pass through U2026 and U2020C to reset the Sweep State Control flip-flop U1025. When U1025 is reset the integrator starts a new sweep.

Sweep Output Circuits

The sweep ramp from the integrator is applied through buffer amplifiers, U3045 and U4050, and a bus on the Mother board to the Deflection Amplifiers, Span Attenuator, and Digital Storage board. The sweep out of U3045 is an 11 volt peak-to-peak ramp centered around 0 volt. The sweep out of U4050 is a 22 volt peak-to-peak ramp for the oscillators.

The sweep signal also drives pen-lift comparator U3010A and the end-of-sweep comparator U3010B. The threshold for the pen-lift comparator is +7.4 volts. The threshold for the end-of-sweep comparator is +8 volts. The sweep ramp, from the integrator, starts at −8 volts and rises towards +8 volts. When the signal reaches +7.4 volts, the pen lift comparator toggles. This output is gated through U3015B and the pen lift signal goes high. When the sweep ramp reaches +8 volt, the end-of-sweep comparator, U3010B, toggles. The resultant low output is applied through U1015A to become the EOS (end-of-sweep) signal.

Marker DAC

The Marker DAC circuit provides a dc level corresponding to the marker sweep position. This occurs during retrace, allowing oscillators to operate long enough for the counter to get an accurate reading of the marker position. The processor loads twelve bits to Marker DAC U1047. This dc level replaces the sweep ramp during the during the retrace time when the sweep is inactive. The Marker circuits on the Horizontal Digital Storage board reads the dc voltage and reconverts to digital to feed the processor. The processor compares these bits to the location of the marker in digital storage and adjusts the Marker DAC bits until the digitized voltage matches the marker position.

U1047 is a 12-bit DAC. The 12 bits come from registers U1040 and U1045, the address 0F second and third extended address registers. The DAC produces a current output, which U2040 converts to a voltage. U2045 sums an offset voltage, giving a voltage range of about ±9 volts. This voltage range is greater than the range of the sweep ramp. This fact, and the DAC having twelve bits guarantee that there will be a twelve bit number for the DAC for each of the 1000 digital storage points.

Sweep Control

U1025A is the Sweep State Control flip-flop. When reset, the high at the Q(bar) output turns off FET Q1062 and allows the integrator capacitors to charge. When the Sweep State Control flip-flop is set, by a low on pin 4, its Q(bar) goes low. This switches the output of comparator U1060B so its output turns Q1062 on and discharges the timing capacitors. The Q(bar) output of U1025A connects to pin 5 of U1017A so this low switches the output pin 6 to its high impedance state (its output is open collector). The Q output of U1025A is high. Both U1016A and U1016B where previously set when the Q output was low. This starts the holdoff cycle or retrace time which is described in detail further on.

The Sweep State Control flip-flop U1025A, is set by a low out of NOR gate U2020A when either the EOS (end-of-sweep) or the ABORT SWEEP lines go high. ABORT SWEEP is generated when a 1 is written to D0 at address 1F. The Sweep Control flip-flop is reset by either a trigger signal from multiplexer U2026 or a high on the MNL or EXT SWP line. The microcomputer writes to bits D2 and D3 at subaddress 1 of address 0F for the manual or external sweep mode.

Trigger Control

A sweep is initiated by the microcomputer, in single sweep or manual mode as noted above, or by one of three trigger signals selected by the multiplexer U2026. Data bits D2 and D3 at address 0F.0 select the input trigger signals and route them to the clock input of U1016B. During sweep time the flip-flop U1016B is set by a low on the Q output of U1025A.

The high on the Q(bar) output of U1025A is also applied through an inverter buffer in U1017A. The resultant low out discharges holdoff capacitor C3032 at the input to U3025B. The output of U3025B is low so the output of NAND gate U1020D is high. Flip-flop U1016B requires a high-to-low transition to clock any input through. Since it is high, incoming trigger signals will have no effect on the circuit.

At the end of sweep, the Q(bar) output of U1025A goes low. This switches the output of U1017A to its high impedance state and the holdoff capacitor, C3032, starts to charge towards +15 volts through R3030. When it reaches +5 volts the comparator output switches high. This, along with a high on pin 13 of NAND gate U1020D, causes the output to go low and the high-to-low transition clocks U2026 so the incoming trigger signal can now clock U1016B and produce a high at the Q(bar) output. This is gated through U2026 to the input of U2020C, so the output of the NOR gate will now reset the Sweep State Control flip-flop, U1025A, and start a new sweep.

In the free-run mode the multiplexer U2026, selects the +5 volts on pin 6. This high is clocked through to the Sweep State Control flip-flop immediately after retrace. Incoming trigger signals are ignored and the sweep runs automatically.

In single sweep mode the sweep circuit cannot be re-triggered until it is armed by the microcomputer. Bit D0 is set high at subaddress 0 of address 0F (U1035-6). This appears as a high on pin 2 of U4010A. Since U1016A has been set by the previous sweep, the two highs at the input produce a low at pin 13 of U1020D. Therefore, incoming triggers are disabled. The sweep is now in an idle state and cannot run until the microcomputer arms the trigger circuit again. This is done by setting bit D3 high at address 1F, which produces a high out of U1026 pin 3 and clocks flip-flop U1016A. The resultant low at pin 1 of U4010A forces a high at pin 11 of U1020D, and arms the trigger circuit. Thus a signal can now trigger the sweep circuit and the single sweep cycle repeats.

Sweep Holdoff

During retrace, the sweep must be held off long enough for the timing capacitors in the integrator to discharge and the circuit to stabilize. To prevent flicker, the holdoff period must vary as sweep time changes. U3025B and three timing capacitors (C3027, C3030, and C3032) plus a resistor (R3030) form the holdoff circuit.

During sweep time pin 5 of U1017A is high. This pulls pin 6 low and discharges C3032. During retrace, pin 6 is released and the timing capacitors start to charge. When they reach +5 V, comparator U3025B toggles and its output goes high. This, along with the high on pin 13 of the NAND gate U1020D, provides the clock pulse for U2026 to pass a trigger signal through to the Sweep State Control, U1025.

Interface Circuits

In addition to the sweep circuits, there are circuits that interface between the microcomputer and the Reference Lock module (Option 05 only). These circuits generate an interrupt (SER REQ) when a change of status in the Reference Lock module occurs, respond to the POLL routine, and provide data so the microcomputer can monitor the status of the Reference Lock module.

To determine the status of the Reference Lock module, the microcomputer reads the status of bits 0 and 1 (DB0 & DB1) of the data bus at address 9F. These two bits connect through tri-state buffers in U4015C to the INTL REF and {REF LOCK}(bar) lines from the Reference Lock module. The INTL REF line is high when the internal reference is used and low for external reference. The {REF LOCK}(bar) goes high when the 3rd LO is not locked to the frequency reference and low when it is locked.

When address 9F is read, U2017 is enabled and latches the {INTL REF}(bar) and REF LOCK signals. Thus, the bits on pins 1,2, and 5,6, of the exclusive-nor gates in U2015 match each other. The open-collector outputs are wired together, so when the outputs are high, inverter U1017B applies a low to the clock input of flip-flop U2025A. When a change in status occurs, one of the bits to the exclusive-nor gates (pin 1 or pin 5) changes. There is now a difference between the present status and the previous status, stored in U2017. One output of U2015 now switches low and a low-to-high transition occurs on the clock pin of U2025A. This triggers an interrupt and causes the microcomputer to inquire about the new status. Reading the new status activates the latch and resets the circuit. Transistor Q3015, driven by bit D4 at address 1F, turns the INTL REF (internal reference) on or off.

The Interrupt and Service Request circuit generates the instrument bus interrupts and responds to the subsequent poll routine from the microcomputer. There are two sources of an interrupt from the sweep board, either an EOS (end-of- sweep) has occurred or a

change of status of the reference lock module is detected. When an EOS occurs, and provided the EOS Interrupt Enable bit is high, the flip-flop U1010A is clocked and its Q(bar) goes low. This produces a high out of U1020B which turns Q4032 on to pull the instrument bus line SER REQ (service request) low and forces an interrupt.

The microcomputer response to an interrupt is with a poll routine. It first writes FF to the instrument address bus. The Sweep board address decoders normally respond only to addresses 0F, 1F, and 9F, but the interrupt circuit detects when bit 7 of the address bus (AB7) goes high. The microcomputer raises the POLL line and reads the instrument data bus. The output of U2010A goes low. This, anded with the low out of U1010A, generates a high to turn Q3020 on and pull bit DB4 of the instrument bus low. When the microcomputer reads a low on bit DB4 it lowers the POLL line and writes 7F on the instrument bus. Again, none of the other decoders respond. However, bit 7 (AB7) of the address is pulled low. The microcomputer now writes a word to the data bus with all bits except bit DB4 high. This acknowledges the interrupt. The microcomputer now raises the POLL line again and since both inputs to U2010B are high, the output of the gate goes low. The POLL line is then pulled low and the low-to-high transition clocks the low on the D input of U1010B through to reset U1010A. Its Q output then sets U1010B. Q4032 is cut off, the interrupt is removed, and the circuit is now ready for another EOS.

When a change-of-status occurs, in the reference lock module, a low-to-high transition occurs on the clock input of U2025A to latch the Q (pin 5) output high and the Q(bar) output low. This low is gated through U1020B to turn Q4032 on, and pull SER REQ line low. When the microcomputer responds, by writing FF and raising the POLL line, U2010A output goes low, however, at this time U2020B output goes high, because of the low on pin 6 of U2025A. This turns Q3025 on and bit DB7 on the instrument bus goes low. The microcomputer reads this and pulls the POLL line low. Address 7F is written on the address bus and the POLL line is raised. This forces U2010B to output a low and the POLL line again goes low to toggle U2025B. The low Q output resets U2025A to remove the interrupt or SER REQ. At the same time U2025B is reset and the circuit is ready to repeat the sequence.

SPAN ATTENUATOR (Diagram 29)

The Span Attenuator, under control of the microcomputer, selects the appropriate attenuation factor for the incoming sweep signal, to establish the frequency span. Refer to the block diagram adjacent to Diagram 29 as well as the schematic diagram. The Span Attenuator consists of digital control circuits, which receive and decode the address and instructions from the microcomputer; the input amplifiers, which perform noise reduction and signal inversion on the incoming sweep signal; the digital-to-analog converter, which attenuates the sweep signal to the desired amplitude for driving the 1st LO Driver; and the decade attenuator, which provides three decades of attenuation for the output signals

Digital Control

Decoder U5025 decodes the address information from the address bus and sends a low signal to either of the two latches, U1025 (address 75) or U2015 (address 76), when a latch is addressed and the DATA VALID line moves high. (The data is stored in the latches on the trailing edge of the DATA VALID signal.) Logic buffer U4015 reduces loading of the data bus. Latch U1025 stores data that controls the eight least significant digits of the span attenuation factor. Latch U2015 stores data that controls the two most significant digits of the span attenuation factor, and other functions on the board. When a span attenuation factor is selected, the microcomputer selects an address and places the first byte of the data on the bus. The DATA VALID signal causes the data to be stored in one of the two latches. Then the second address is called and the next byte is stored in the other latch. The block diagram illustrates the significance of each bit in tables near the affected circuit. A logic 1 represents the more positive of two levels or high state, and a logic 0 represents the more negative of two levels or low state.

Input Section

The sweep signal and its ground reference are applied to differential input buffer U3036. Any signals or noise induced in the two signal transmission paths are canceled by this stage.

The following stage consists of amplifier U3032, plus switching transistors Q2025, Q2028, and Q2023. Different mixing modes require the 2nd LO frequency to either increase or decrease to increase the signal frequency. Thus, this circuit is a unity gain amplifier that can be changed from inverting to non-inverting, under bus control. When line Q8 of latch U2015 is low, Q2023 conducts and its collector moves positive to about +5 V. This in turn causes both Q2025 and Q2028 to conduct. Pin 3 of U3032 is effectively grounded, the sweep signal is applied through R3028 to the summing node of the amplifier, and the gain of the stage is −1. If line Q8 is high, Q2023 does not conduct and the voltage at its collector falls to nearly −15 V. Neither Q2025 nor Q2028 are now in conduction, so the sweep signal is applied to pin 3 of U3032, and pin 2 is disconnected. Now, the gain of the stage is +1.

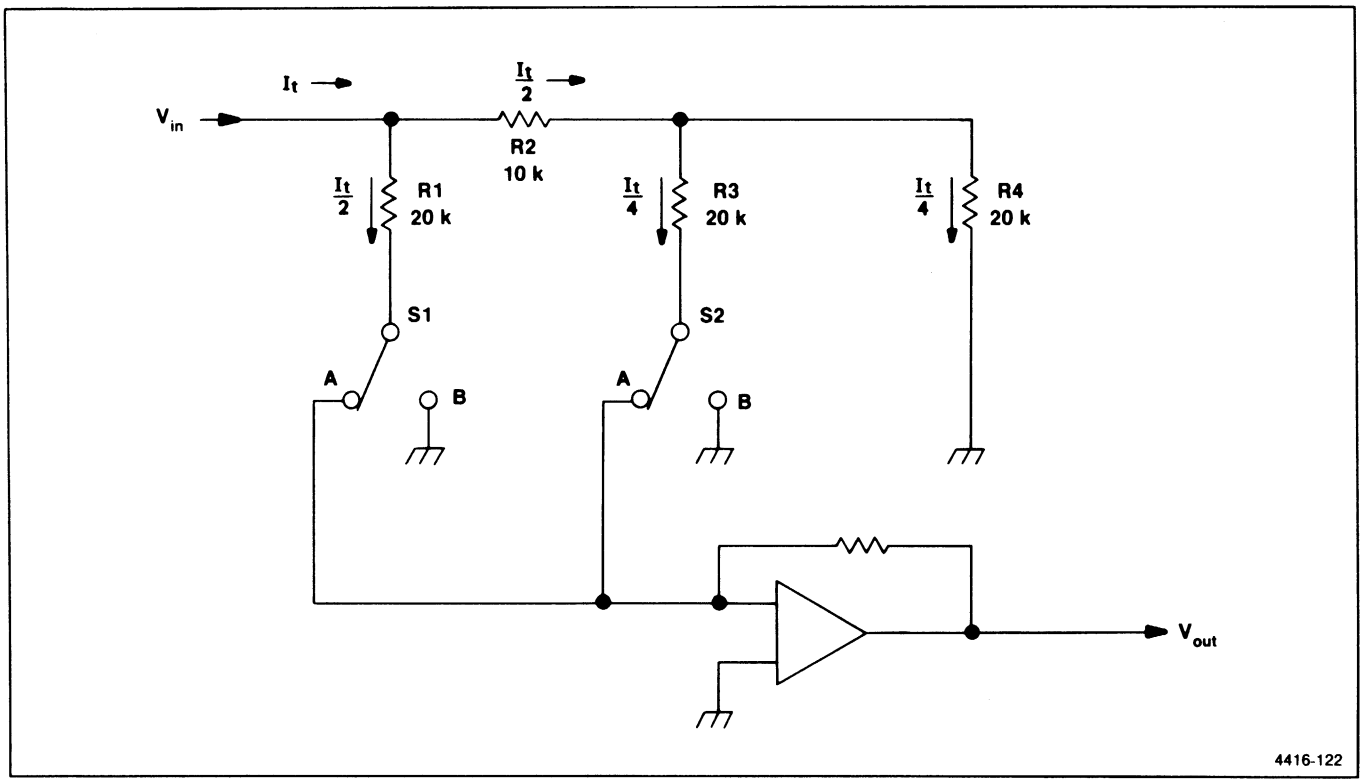


Figure 7-19. Simplified digital-to-analog converter.

Digital-To-Analog Converter

The magnitude of the sweep signal is determined by the desired frequency span, band, and option installed in the instrument. The microcomputer calculates the proper magnitude for each combination, and sends the appropriate codes to the data latches, which in turn control the attenuation factor of the digital-to-analog converter. This stage consists of converter U1042, amplifier U2042, and a complementary pair, Q2062 and Q3056, that form the output current buffer.

Figure 7-19 shows a simplified two-bit digital-to-analog converter. The circuit works by current division. Since the amplifier summing node is at ground potential, the current through a resistor is not affected by the position of the switch that selects that resistor. For example, when switch S1 is at position B, the current is shunted to ground. When S1 is at position A, the current through R1 becomes part of the total output current. Thus, the output current can be 0, 1/4, 1/2, or 3/4 of the total current available. Because of the resistance ratios, the ratio of the output voltage to the input voltage equals the ratio of the output to the total current ($V_{out}/V_{in} = I_{out}/I_{total}$). In this 2-bit converter, there are 2^2 or 4 output values possible. In the actual 10-bit converter, there are 2^{10} or 1024 output values.

In converter U1042, each internal resistance is switched in or out by a CMOS FET (internal to the device). The CMOS inputs are each protected by a series input resistor. Since the sweep signal is applied to the Vref input, U1042 serves as a digitally controlled attenuator for the sweep signal.

The attenuated sweep signal from U1042 is applied to U2042, an operational amplifier. It in turn drives an output current buffer, consisting of complementary pair Q2062 and Q3056. The pair is biased to produce a standing current of about 10 mA in the absence of an applied signal. This eliminates crossover distortion of the output signal. Diodes CR2051, CR2053, CR1051, and CR1049 provide temperature stabilization for the bias current in the stage. When high current is passing through the pair, diodes CR1056 and CR1061 clamp the voltage across the emitter resistors to reduce voltage drop.

Feedback for the output stage is provided by R1056, plus an internal resistor in U1042. The internal feedback resistor ensures better temperature tracking. The internal resistor provides a gain slightly less than unity; R1056 increases the stage gain and permits gain calibration, as described below.

One-of-four decoder, U4025, uses data bits DB3 and DB4 lines from U2015, to control three sections of a quad FET switch, U3025. (RC circuit inputs of each FET control line filter out noise from the digital circuits.) The code is exclusive; i.e., only one FET is switched on at a time. See Table 7-12 for a listing of the codes. When a FET is switched on, it connects a calibration adjustment potentiometer to the summing node of the operational amplifier. Adjustment R1065 sets the 1st LO tune coil sweep, R1071 sets the 1st LO FM coil sweep, and R1067 sets the 2nd LO span.

Table 7-12
CALIBRATION CONTROL SELECTION CODES

U4025		
DB3 (Pin 3)	DB4 (Pin 2)	Selected Adjustment
0	0	R1065 (main coil)
0	1	R1071 (FM coil)
1	0	R1067 (2nd LO)

Decade Attenuator

Since accuracy of the digital-to-analog converter is specified as a percentage of full scale, the accuracy decreases as the attenuation is increased. To maintain accuracy at 1%, it is never used at an attenuation factor of more than ten. If more attenuation is required, the decade attenuator, consisting of K4072, K3075, K3065 and the connected divider network, provides further sweep attenuation of X0.01, X0.1, and X1. See Figure 7-20 for a simplified circuit diagram.

The "2" side of U4025 is controlled by data bits, DB5 and DB6, on the Q6 and Q7 lines from U2015. The "2Y" outputs of U4025 are applied through buffers in U4042 to select the appropriate attenuation factor for the output sweep. Table 7-13 lists the states required to energize the attenuation relays. A diode across each relay coil protects the driving circuit from inductive feedback transients.

Table 7-13
ATTENUATION SELECTION CODES

U2015		
DB5 (Pin 15)	DB6 (Pin 16)	Attenuation Factor
0	0	×1 (K3065)
1	0	×0.1 (K3075)
0	1	×0.01 (K4072)

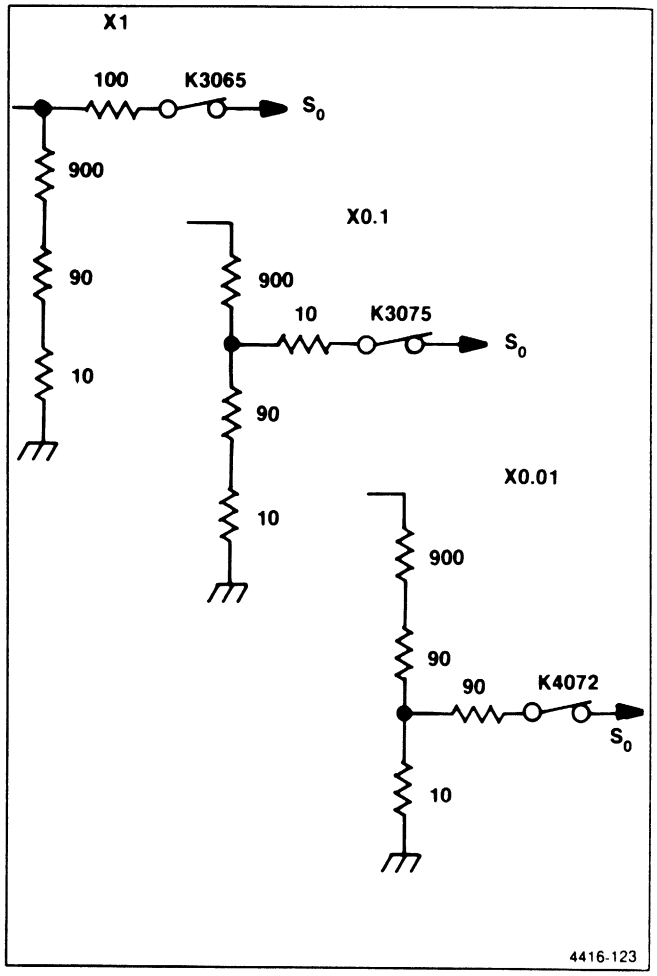


Figure 7-20. Simplified span decade attenuator.

1st LO DRIVER (Diagram 30)

The 1st LO Driver performs the following functions:

- Combines the SPAN VOLTS with the COARSE TUNE VOLTS and outputs the combination to the Oscillator Driver circuits, which drive the 1st Local Oscillator coil.
- Controls the oscillator filter switch.
- Produces a −10 V reference.

The major circuits and their function are:

- The digital control circuits buffer the incoming data from the data bus, decode the address data, connect or disconnect the TUNE VOLTS and SPAN VOLTS signals to the summing amplifier, energize the filter switch in the 1st LO assembly, and control

the oscillator driver stage.

- The oscillator filter switch driver furnishes drive current to the capacitor switching relay in the 1st LO assembly
- The input switching circuit connects or disconnects the SPAN VOLTS and COARSE TUNE VOLTS signals to the input of the summing amplifier.
- The summing amplifier, furnishes the drive signal to the oscillator driver. The summing amplifier sums the SPAN VOLTS ramp signal, from the Span Attenuator, with the COARSE TUNE voltage, from the Center Frequency Control circuit. In less than maximum span, a sweep voltage of ±10 V sweeps the oscillator at a rate of 180 MHz/division. As the TUNE VOLTS signal varies from −10 V to +10 V, the oscillator's center frequency is moved over its full range.
- The oscillator driver, furnishes the current drive for the 1st LO coil.
- The −10 V reference supply, produces a precise −10 V reference for the 1st LO Driver.

Digital Control

The digital control circuit sets the oscillator span volts. Decoder U4034 output Y1 (pin 14) goes low when the input address is 72 and output Y7 goes low for address 7E. When output Y1 goes high, data is clocked or latched into U4017, and when Y7 goes high data is latched into U4024 and U4022.

Data for U4017 consists of control codes for the oscillator drive circuits.

Input Switching

If the main coil of the oscillator is not to be swept, DB6 (line Q7 of U4017) goes low. This cuts Q3028 off, de-energizes K3034 and disconnects the SPAN VOLTS signal to the summing amplifier. Diode CR3031 protects Q3028 from the inductive feedback surges that occur at turn-off.

Oscillator Filter Switch Driver

When relay K3034 is de-energized, DB6 is low, Q2029 is biased on which drives a capacitor switching relay on the 1st LO Interface board. The capacitors are switched across the main coil, when it is not being swept, to filter noise riding on the tuning current. Capacitor C2025 provides a gradual decay of current through the relay after power is turned off.

Summing Amplifier

Amplifier U2032 and the complementary pair of transistors, Q2035 and Q2039, plus related components, form an operational amplifier. The COURSE TUNE VOLTS and the SPAN VOLTS sum at the input to U2032. The operational amplifier feedback resistor is R1038. The input resistance is R2027 for the COARSE TUNE VOLTS signal and R2031 for the SPAN VOLTS signals. (R2030 is switched across R2031, as mentioned previously, to increase stage gain for maximum span operation.) The output of the summing amplifier, which can swing from −10 V to +10 V, is applied to the Video Processor.

Oscillator Driver

The output of the summing amplifier also drives the input to the oscillator driver stage when FET Q2040 is switched on. The oscillator driver stage consists of active components Q2045, U2043, Q3047, and Q352. The input resistance consists of R2041, the 1st LO Sensitivity adjustment R1031, plus R2043. The feedback resistance is R2042. The amplifier converts a voltage input into a current drive for the 1st LO tuning coil by controlling the voltage across current sense resistor R1040, which is in series with the oscillator tune coil. Q3047 assures that Q352 base current remains within the oscillator tuning coil circuit. Q2040 is biased on except when the oscillator is degaussed. The output of the operational amplifier U2032, Q2039 and Q2035, is applied through the 1st LO Sensitivity adjustment R1031, and summed with an offset voltage set by the 1st LO Offset adjustment R1032, at the input to the preamplifier stage Q2045. Adjustments R1031 and R1032 match the oscillator driver stage to the oscillator characteristics. R1032 adds offset to the input of the preamplifier to place the oscillator at center operating frequency when the amplifier input is at 0 V.

Q2045 is a low-noise, matched, dual transistor. The feedback path through R3040 and R2042 sets the voltage across a four-terminal resistor R1040. This voltage sets the current through the resistor which is also emitter current for driver transistor Q352. The 1st LO Sensitivity adjustment R1031, sets the voltage gain of the amplifier. This in turn, changes the current drive to the oscillator coil.

Reference Supply

Preamplifier Q2052 plus amplifier U2052 and emitter follower Q2051, are the active components of the −10 V reference supply. Bias for one side of Q2052 is set by VR1055. The other side is set by the −10 V Adj R1034. Any change in the supply is amplified by Q2052 which changes the drive to the pass transistor Q2051 which compensates for the change. The diode network across the base-emitter junction limits the emitter current to about 30 mA.

CENTER FREQUENCY CONTROL (DIAGRAM 31)

The Center Frequency Control converts digital information, from the front panel FREQUENCY control or on the GPIB bus, via the microcomputer, to analog voltages for the 1st LO Driver. These in turn control the center frequency of the analyzer. The Center Frequency Control board contains the following major circuits:

1. The Digital Control circuit, which buffers and decodes the addresses and other data to control the other circuits.

2. The coarse and fine storage registers (latches), which store the numerical bytes that control the digital-to-analog converter (DAC) stages.

3. The coarse and fine DAC stages, which convert the digital inputs from the storage registers into analog current and voltage equivalent values.

4. The coarse and fine track/hold amplifiers, which store the analog output values during the approximation routine and compare the stored value to the approximated value for the microcomputer.

5. The write-back circuits, which inform the microcomputer when the stored value and the approximated values are equal.

Operating Modes

An explanation of circuit design principles is given before the operation of the circuit is described. Two DAC chips are used in tandem to get the required resolution. However, this method can cause errors and non-monotonic behavior in the overall converter circuit. To circumvent this problem, the outputs of the tandem DAC units are summed together so that the two units are overlapped by three bits. That is, the MSB of the low-order DAC is weighted equally with the third least significant bit, or 2×10^{-10} bit of the high order DAC. The overlap means that the lower DAC will have sufficient range to monotonically tune the output of the converter over the entire range of the analyzer, but only if the proper codes of the lower DAC device can be found. Now, suppose that the tandem DAC is loaded as follows:

Upper order 1 0 0 0 0 0 0 0 0 0 0 0
Lower order 1 1 1 1 1 1 1 1 1 1 1 1

The contents of the devices are shown overlapped to illustrate the bit weighting. Now assume that the low-order device is to be incremented one bit. The MSB of the low-order device must be moved into the high-order device before the low-order device can be incremented. Thus, the two must appear as follows:

Upper order 1 0 0 0 0 0 0 0 0 1 0 0
Lower order 0 1 1 1 1 1 1 1 1 1 1 1

If the high-order device operated with no overall linearity inaccuracy, the operation would now be complete and the low-order incrementing could occur. However, the DAC device can vary by one LSB of the correct value. Figure 7-21 illustrates a graph of the best and worst case output. Note, that even in the worst case, the output may move only once every two or three state changes, but the output is always monotonic and within one LSB of the correct value.

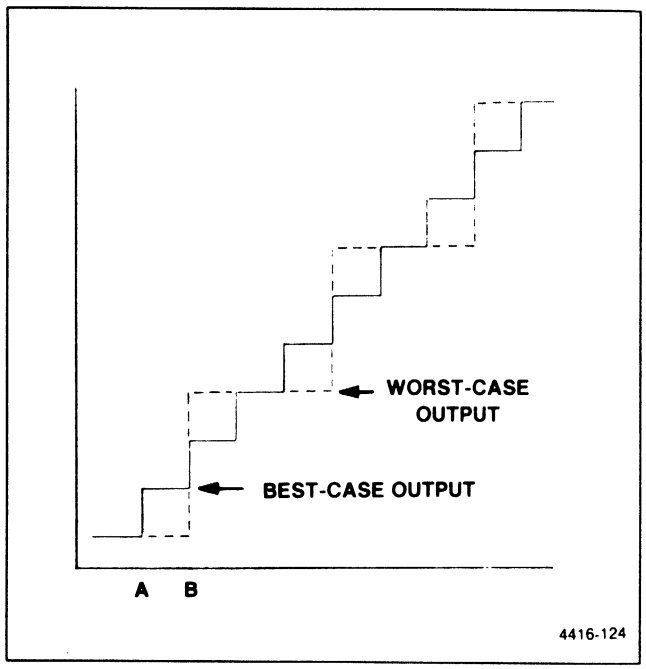


Figure 7-21. DAC Variance graph.

If, in the example shown previously, the high-order device is at point A in Figure 7-21, incrementing the device to point B has no effect on the output. If the MSB of the low-order device is set to zero, as shown in the first example, the combined output will actually decrease. Ordinarily, the Center Frequency Control circuit can increment and decrement whenever the microcomputer commands without going through a special routine. However, as just described, some microcomputer adjustment is necessary to compensate for the disparity that usually occurs between the low-order and high-order DAC units.

The first operating mode is the tracking mode, where the preamplifier and integrator are connected together by the disconnect stage, and the entire unit acts as an operational amplifier. Figure 7-22 illustrates the basic circuit. While the circuit operates in this mode, the amplifier tracks the DAC stage and sends the voltage out to the tuning circuits.

When the transfer of bits from the lower to the upper DAC is required, the microcomputer commands the circuit to shift to the hold mode. The command comes through the decoder to shut off the disconnect stage, and the preamplifier output is disconnected from the integrator. The integrator holds the voltage that was previously at the output for comparison, and the approximation cycle begins.

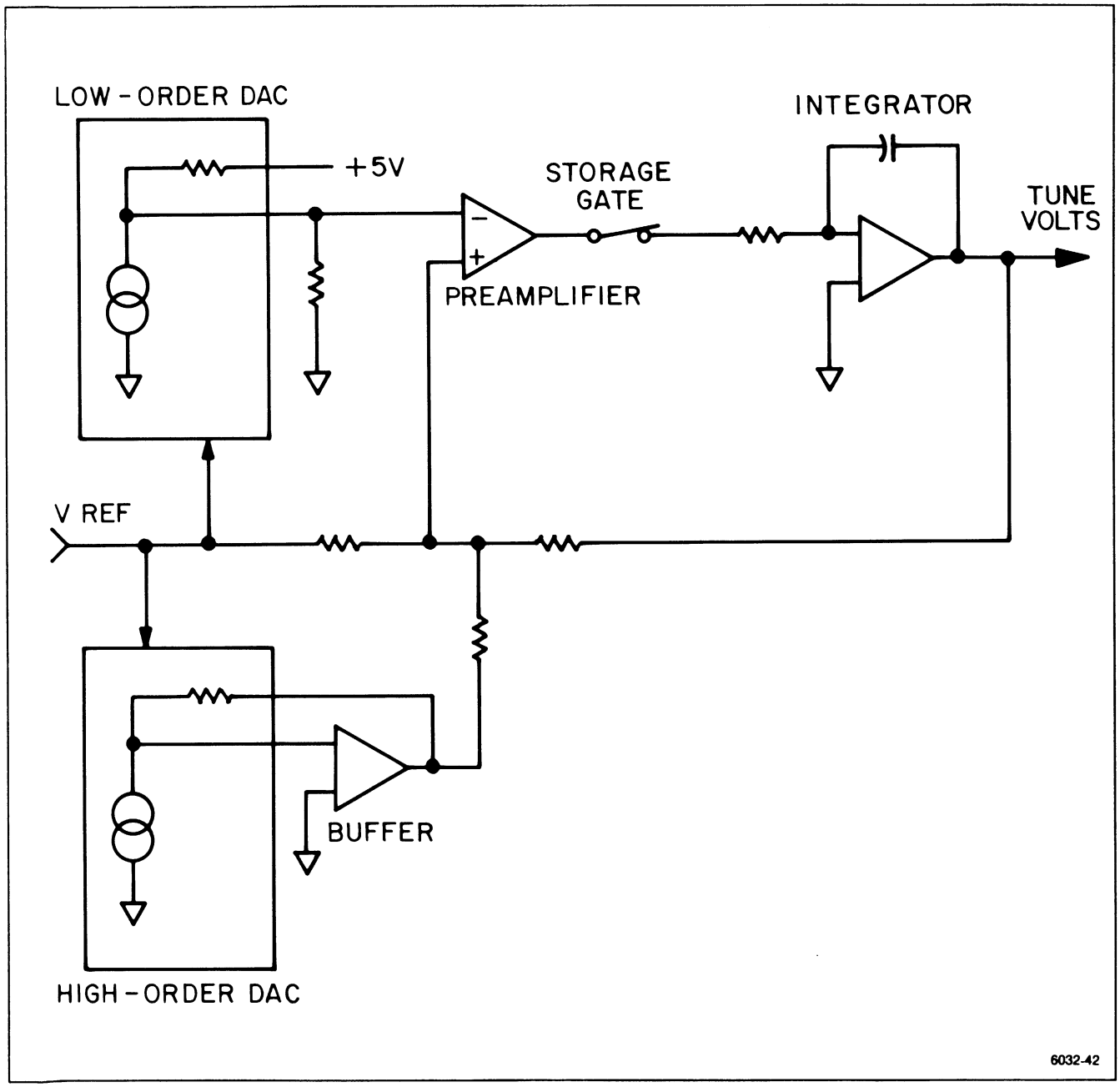


Figure 7-22. Simplified tune voltage converter.

The microcomputer resets the low-order DAC to zero. Then, the highest order bit in the low-order DAC is set to one, and the circuit is queried to find if the DAC output and integrator output is greater or less than required. If less, the microcomputer loads the next lower bit in addition and queries the circuit once more. This process goes on until the two values are the same. Had the microcomputer found that the DAC output was greater than the integrator output at the first inquiry, it would have set the highest order bit to zero and loaded the second-order bit into the low-order DAC, then continued to load successively lower order bits, one at a time, until the circuit signaled that the comparison had reversed. By this process, which is known as the successive approximation method, the circuit finally reaches the point where the outputs are equal, and the microcomputer commands the circuit to shift back to the track mode.

Digital Control

The digital control circuits consist of buffer U4035, address decoder U4045, steering register U4025, and the steering gates (U4015A, U4015B, U4015D, U4060A, U4060B, and U4060D). Because of the large amount of data that must pass through these circuits, a steering register that has a separate address is used. The first byte of data, the steering byte, is clocked into U4025 by the ADDRESS 70 signal. The output levels are applied to the steering gates, and the circuit waits for the next byte.

The microcomputer then furnishes the first byte of data to be sent to the low-order, fine-tune, DAC via the storage register. Latch U3015 and part of U3025 form one storage register for the low-order, fine-tune DAC. The byte is clocked into the register by the coincidence of low states at the inputs of the steering gate(U4015A or U4015B); one from the steering byte, and the other from ADDRESS 71 signal, which is used to clock the steered data bytes into the correct register. This continues until seven bytes of data have been clocked into the register, including the steering byte. The third output from U4045, ADDRESS 80, controls transistors Q1058 and Q2017, which enable the write-back function. In addition to the six steering lines that drive the steering gates, U4025 also controls, by means of the Q3 and Q7 lines, the hold/track selector transistor for each converter side.

Table 7-14 illustrates the format for ADDRESS 70. Addresses are expressed as hexadecimal numbers. Table 7-15 lists some of the significant states that are used to tune the DAC.

Storage Registers. Six storage registers are used in the circuit, U3015, U3025, U3035, U3050, U3060, and U3070. Since both sets are identical, only the coarse tune section will be described.

Data from U4035, the data buffer, is clocked into the registers each time a different tune voltage is required. U3050 feeds the lowest eight bits to the low-order DAC, U2055; U3070 feeds the highest eight bits of the high-order DAC, U2060. Register U3060 feeds the remaining bits of both units.

Table 7-14
ADDRESS 70 FORMATS

DB0	Fine Tune low byte enable
DB1	Fine Tune middle byte enable
DB2	Fine Tune high byte enable
DB3	Fine Tune hold
DB4	Coarse Tune low byte enable
DB5	Coarse Tune middle byte enable
DB6	Coarse Tune high byte enable
DB7	Coarse Tune hold

Digital-To-Analog Converters. Since both the coarse and fine tune circuits operate similarly, only the coarse tune section of the board will be discussed here. Figure 7-22 is a functional block diagram of the circuit.

Each side of the converter has two DACs summed together to produce an output of approximately ±10 V. The DACs are programmable current generators driving the preamplifier-integrator circuit. The high-order DAC provides 0 to 2 mA of current to the circuit via the buffer, while the low-order DAC provides approximately ±2.5 mV at the inverting input of the preamplifier. The preamplifier then drives the integrator via the storage gate.

An isolated ground system for each half of the circuit minimizes susceptibility to noise and extraneous signals. This is because the converters provide the dc voltages that tune the oscillators.

Track/Hold Amplifier

The amplifier consists of high-order DAC U2060, low-order DAC U2055, buffer U2050, preamplifier U1065, storage gate Q1065, and integrator U2070.

Table 7-15
DAC TUNING CODES

Tuning Point	Data	Address	Results
Positive full range	00	70	Enables all latches, track mode
	00	71	Loads zeros into all positions of both DACs
Mid-range	00	70	Enables all latches, track mode
	00	71	Loads zeros into all positions of both DACs
	33	70	Enables high byte latch, track mode
	80	71	Loads 80 into DACs. Midrange value
Negative full-range	00	70	Enables all latches, track mode
	FF	71	Loads FF into all positions of both DACs

The circuit output is required to tune approximately ±10 V for the full-scale range of U2060. When U2060 is off and the output of U2050 is at 0 V, the +10 V output level is set by 1 mA of current through R1055, and the combination of R1032, R1053, and R1070. When U2060 is fully on, and output of U2050 is at +10 V, the −10 V output level is set by 2 mA of current through R1052, less the 1 mA constantly flowing in R1055.

Full-scale gain is adjusted by R1032. Resistors R1052, R1053, and R1055 are matched for temperature coefficient to minimize output voltage drift as a function of temperature.

Low-order DAC U2055 tunes approximately ±2.5 mV at pin 1, and its gain is adjusted by R1028. The gain of preamplifier U1065 is set at approximately 10,000 by R1056 and the 5Ω combination of R2059 and R2060. The combination of CR1056, CR1058, R1054, and R1059 limits the gain of U1065 when the output exceeds approximately 0.7 V in either direction.

U1065 is connected to integrator U2070 via storage gate Q1065, which is on in the track mode. Transistor Q1065 is turned off any time a DAC is being tuned to allow the DAC output to settle before tuning the output of U2070. It is also turned off during the interval when a carry from the low-order DAC to the high-order DAC occurs. Transistor Q1065 is controlled by Q1061. When Q1061 is on, CR1064 is reverse-biased. The voltage at the gate of Q1065, which is developed by R1064, R1065, R1067, and R1066, is near 0 V and Q1065 conducts. When Q1061 is off, voltage to pinch off Q1065 is applied through R1062 and CR1064.

U2070 tracks the output of U1065 when the circuit is in the track mode and serves as the inverting amplifier in the feedback system shown in Figure 7-22. Normally the incoming signal is routed through R2067. To improve the slewing rate of the integrator, CR1067 and CR1069 conduct and connect R1068 across R2067 when input signals over 1 V are present.

Write-Back Circuit

This circuit consists of comparator U1055 and enabling transistor Q1058. When it is necessary to do a carry between the low- and high-order DACs, the circuit is put into the hold mode by turning off Q1065. U2060 is incremented one bit and U2055 is reset to all zeroes. The output of U1065 is now at something other than 0 V.

The purpose of the following approximation routine is to get output of U1065 as close to 0 V as possible before switching the circuit back into track mode by turning on Q1065. Comparator U1055 detects whether the output of U1065 is above or below coarse tune ground. The instrument microcomputer begins to exercise the low-order DAC bits one at a time from MSB to LSB. After each bit is turned on, U1055 is enabled by turning off Q1058. If U1055 detects that the output of U1065 has crossed 0 V, that bit is turned off and the next lower bit is turned on. This continues through all 12 bits and when completed, the output of U1065 should be close to 0 V. Transistor Q1065 can now be turned back on without causing excessive jumping of the signal on the screen.

−10 V Reference Buffer

The circuit uses the voltage reference developed on the 1st LO Driver board as a reference for the DACs. Differential amplifier U2045 receives the −10 V reference and −10 V reference return, and removes any common-mode signals present. Resistor pairs R1048/R1049 and R1050/R1051 are matched for temperature coefficient to minimize reference voltage drift over temperature.

COUNTER and PHASE LOCK SECTION (Diagram 7)

FUNCTIONAL DESCRIPTION

This section consists of a Counter, Phase Lock assembly, Phase Gate, Harmonic Mixer, and Auxiliary Synthesizer. The Counter, Harmonic Mixer, and Auxiliary Synthesizer, form the nucleus of the frequency control hardware for the instrument. Both the 1st LO and 2nd LO frequencies are controlled via a firmware based control loop that uses data from the Counter as feedback to control oscillator frequency. The 10 MHz IF is also counted to accurately calculate signal frequency.

The Phase Lock assembly stabilizes the 1st LO frequency. It consists of an outer and inner loop.

The inner loop uses the subharmonic of the 100 MHz reference frequency, from the 3rd Converter, to mix with the output from a 25.032 to 25.095 VCO and compares this IF difference with a +N number (between 32 kHz and 94 kHz) set by the processor. Any deviation is detected by a phase/frequency detector whose output error voltage is used to pull the VCO frequency and phase into lock with the inner loop reference.

The outer loop consists of the inner loop, a Strobe Driver, Phase Gate Detector, Error Amplifier, and the 1st LO. The frequency of the inner loop VCO is divided down and applied as a strobe pulse to the Phase Gate Detector. This strobe pulse contains energy at frequencies equally spaced throughout the spectrum. One of these frequencies will be within 2.5 MHz of the 1st LO frequency at the other input to the Phase Gate Detector. The Phase Gate Detector outputs an error signal proportional to the difference between the nearest strobe and the 1st LO frequency. This error signal is amplified and filtered by the Error Amplifier and applied to the FM coil of the 1st LO to pull it into frequency and phase lock with the strobe.

The Harmonic Mixer mixes the 1st LO frequency and a harmonic of a synthesized 200-220 MHz signal from the Auxiliary Synthesizer. The exact frequency of the synthesizer signal is a function of the +N factor from the processor. The Harmonic Mixer output is a signal within the 10 to 80 MHz range. This signal is divided in the Auxiliary Synthesizer and sent to the Counter. The microcomputer looks at the resultant count and decides which way to move the 1st LO to bring it to the correct frequency.

Phase Lock Assembly

As previously stated, the phase lock system consists of two frequency servo loops, called the outer loop and inner loop. In the inner loop operation, the 100 MHz reference signal from the 3rd Converter, is divided down to 25 MHz, on the Synthesizer board, and applied as the reference signal to the mixer on the Offset Mixer board. The 25 MHz signal is also applied as a clock signal to +N counter circuits, on the Synthesizer board, which output a frequency (depending on the +N number from the processor) between 32 kHz and 94kHz. This signal is applied to the phase/ frequency detector on the Offset Mixer board, where it is compared to the IF output (difference between the 25 MHz reference and the output from the VCO (voltage controlled oscillator) and any difference is output as an error voltage to the Error Amplifier.

The VCO operates between 25.032 MHz and 25.094 MHz, depending on the drive from the Error Amplifier. This signal is applied to the RF input of the mixer on the Offset Mixer board, where it mixes with the 25 MHz reference frequency. The difference frequency, which is between 32 kHz and 94 kHz, is applied to the phase/frequency detector and compared to the +N frequency. If the two signals are edge and frequency coincident, phase lock occurs. If they do not coincide, an error signal is generated, passed through the Error Amplifier, and applied to the VCO to shift the oscillator frequency until it is phase locked. This evolution typically lasts for only a few milliseconds, so the inner loop phase lock is, for all practical purposes, instantaneous.

The outer loop, which includes the inner loop circuits (Offset Mixer, Error Amplifier, and VCO) consists of the Strobe Driver, Phase Gate, Error Amplifier, and 1st LO. (The Harmonic Mixer, Auxiliary Synthesizer, and Counter, are a part of the operation, but are not considered a part of the loop.)

The signal between 25.032 MHz and 25.094 MHz from the VCO is applied to the Strobe Driver where it is divided by five, filtered, and sent to the Phase Gate Detector as a strobe signal between 5.006 MHz and 5.019 MHz. This strobe generates line spectra that are equally spaced approximately 5 MHz over the spectrum. At about the 400th line, which corresponds to 2 GHz, assuming that the 1st LO is tuned to a frequency near 2 GHz, one of these lines (at about the 400th line) will be within 2.5 MHz of the 1st LO frequency. The Phase Gate Detector will then output an error signal that is proportional to the difference between the 1st LO frequency and that of the nearest strobe line, if that difference frequency is less than approximately 1MHz.

For phase-lock acquisition, the microcomputer calculates the strobe frequency required for the desired 1st LO frequency. The strobe is set to this frequency and the 1st LO is set to the required harmonic of the strobe. The outer loop is closed, and the microcom-

puter tunes the 1st LO frequency through the following sequence; up 750 kHz, down 1.5 MHz, up 1.5 MHz, and down 750 kHz. During one of these "firmware searches" the 1st LO frequency passes through the strobe harmonic frequency and the loop acquires lock.

Any frequency difference between the strobe signal and the 1st LO will generate a low frequency correction voltage. This correction voltage is filtered by the F(s) amplifier, then used to drive the oscillator FM coil to pull the oscillator frequency back to the strobe position. If the 1st LO drifts beyond the error voltage range of the F(s) amplifier, comparators on the Error Amplifier board, that monitor the error voltage, will interrupt the microcomputer and indicate the direction of drift. The microcomputer then tunes the Center Frequency Control circuits to null out any FM coil current in the phase lock loop.

Frequency Control

The 21-bit counter and its associated control circuitry, on the Counter board, plus the Harmonic Mixer and Auxiliary Synthesizer, form the frequency control hardware nucleus for the spectrum analyzer. A firmware-based control loop, that uses data from the counter as feedback on the oscillator frequency, controls both the 1st LO and the 2nd LO frequencies. The 10MHz IF is also counted by the Counter to determine the input signal frequency to the analyzer.

A mix down counting scheme is used to count the 1st LO frequency, which varies between 2 GHz and 6 GHz. The 200-220 MHz output from the Auxiliary Synthesizer is positioned so one of the signal harmonics is approximately 45 MHz above the 1st LO frequency. This output drives the LO input to the Harmonic Mixer, the 1st LO drives the RF input. One of the IF outputs from the Harmonic Mixer is within the 10 to 80 MHz range (approximately 45 MHz). This IF signal is passed through a 10-80 MHz band-pass filter, divided by 100, then counted by the Counter. Since the Processor knows the Synthesizer frequency, the 1st LO frequency can be calculated if the Processor knows which harmonic of the Synthesizer frequency was used to generate the IF frequency being counted. The harmonic of the Synthesizer frequency is calculated from the 1st LO tuning DAC (digital-to-analog converter) code, since it indicates the 1st LO frequency to within approximately +/-10 MHz.

Counting the 2nd LO frequency is much simpler. The controllable 16-20 MHz VCO in the 2nd LO assembly determines the frequency of the 2nd LO; therefore, the 2nd LO frequency is calculated by directly counting the 16-20 MHz signal. The 2nd LO frequency is then calculated from this frequency.

Controlling the Oscillator Frequency. The frequency control loop is only closed between sweeps. After the completion of each sweep, the processor switches the span/div to zero and then counts the 1st LO and the 2nd LO frequencies. If they are not at the frequency required to generate the displayed center frequency, they are set to the correct frequency by repeating the process (i.e., the DACs are changed to tune the LO, the LO is counted, etc.).

In the single sweep mode, the oscillator frequencies are corrected after each single-sweep actuation, and before the sweep starts. In the manual sweep mode, or other non-recurring sweeps, the oscillators are corrected at periodic intervals.

Counting the IF. In addition to counting the frequency of the 1st and 2nd LO, the 10 MHz IF is counted when the Counter mode is actuated; thus, the incoming signal frequency can be calculated from the frequency conversion equation for the analyzer. The 1st LO is actually phase locked before the 2nd LO and IF are counted, in order to reduce FMing in the IF signal. This allows very accurate signal counting, even in wide spans.

HARMONIC MIXER (Diagram 32)

The Harmonic Mixer combines a portion of the 2-6 GHz 1st LO signal with harmonics of the 200-220 MHz reference signal from the Auxiliary Synthesizer to provide an output signal in the 10-80 MHz range. This signal is amplified and returned to the Auxiliary Synthesizer where it is counted to get an exact computation of the oscillator frequency. The Harmonic Mixer consists of a directional coupler, an input amplifier, the mixer, and an output amplifier, all on a hybrid alumina circuit. Figure 7-23 is a functional block diagram of the Harmonic Mixer.

Input signal level, from the 1st LO to directional coupler A25A1, is a about +10 dBm. The coupling ratio is 10 dB, therefore, the coupler will deliver about 1 mW (0 dBm) to the RF input of the harmonic mixer. The through-port contributes about 0.5 dB of loss for the 2-6 GHz signal.

The 200-220 MHz reference signal, at a level of about 10 mW from the Auxiliary Synthesizer, is amplified to a level of about 100 mW (+20 dBm) by a differential amplifier Q1 and Q2. Resistor R27 couples the emitters together and the current is set by R13 and R14. Output is transformer coupled to the input of the mixer. Input signal level to the amplifier is +7 dBm minimum.

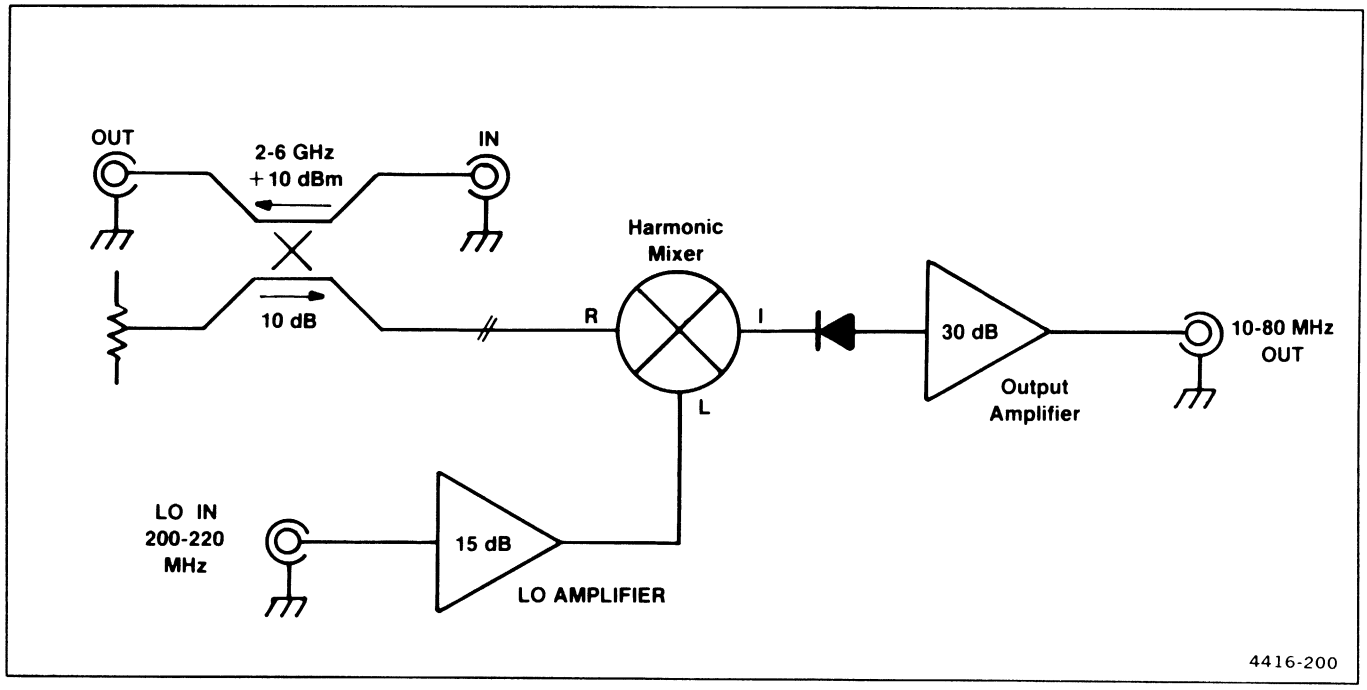


Figure 7-23. Simplified schematic of harmonic mixer.

Two additional directional couplers are used to couple the 2-6GHz signal into the mixer circuit. A power splitter (R1, R2, R3) splits the signal into two paths. Each signal (approximately −6 dBm each) is then coupled through these couplers to the mixer. The through ports are terminated in 50 ohms. Thus the 2-6 GHz signal is coupled into the mixer differentially at a power level of about −16 dBm.

The 200-220 MHz reference signal is also coupled differentially into the mixer circuit, since the output of transformer T1 is applied across the two terminating resistors R4 and R5. The level of this signal is high enough to drive the snap-off diode into its operational region. Harmonics of this 200-220 MHz signal mix with the 2-6 GHz signal to generate numerous IF products which are detected by diodes CR2 and CR3 and fed to the output amplifier.

The output amplifier is a two stage common-emitter cascade amplifier with dc coupling between stages. The standing current through the second stage (Q4) is higher than in the first stage (Q3) to provide better power and intermodulation performance. The amplifier is designed for a 10 to 80 MHz response. Signals above 80 MHz are rejected by a low-pass filter in the Auxiliary Synthesizer. Output level of signals in the 10-80 MHz range is typically -20 dBm for input signal levels as described.

AUXILIARY SYNTHESIZER (Diagram 33)

The Auxiliary Synthesizer is part of the spectrum analyzer's Direct Frequency Readout (DFR) system. This, along with a harmonic mixer, counter circuits, supporting filters and amplifiers, and appropriate firmware, make up the DFR. The DFR provides the means for measuring and determining the frequency of all oscillators and the center of the IF, so the center screen frequency is always known. Since the IF signal can be counted, this allows direct frequency measurement of any signal applied to the input port of the spectrum analyzer.

A functional block diagram of a simple or basic synthesizer is shown in Figure 7-24. The VCO frequency is divided by "N" in a programmable down-counter which outputs a pulse every Nth input pulse. This frequency along with a frequency reference is then fed to a phase/frequency detector. The difference between the two signals is filtered and fed back as a control voltage to the VCO to phase lock the oscillator to the reference. VCO frequency is related to the reference by, $F_{ref} = NF_{ref}$. As N is changed, the VCO frequency will change by F_{ref} for each step in N. This produces outputs separated by F_{ref}. To get closely spaced channels, in tuning the VCO, the reference frequency must be relatively low.

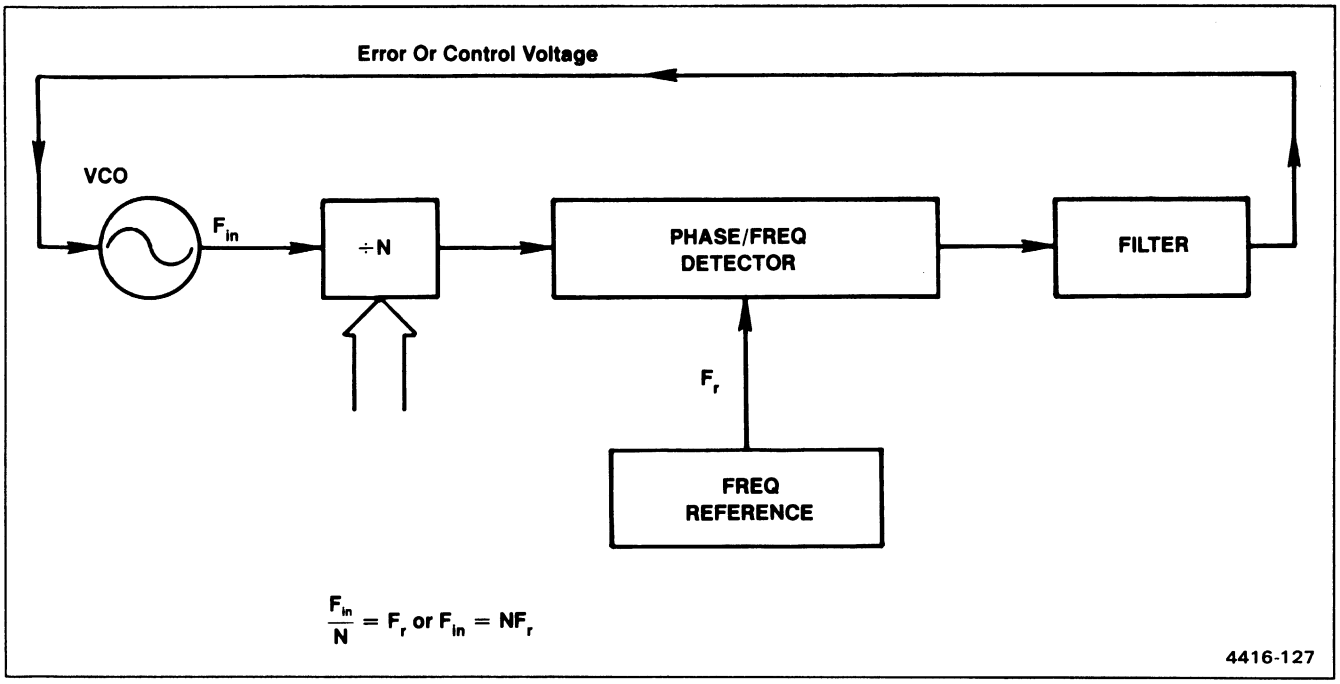


Figure 7-24. Block diagram of a basic synthesizer.

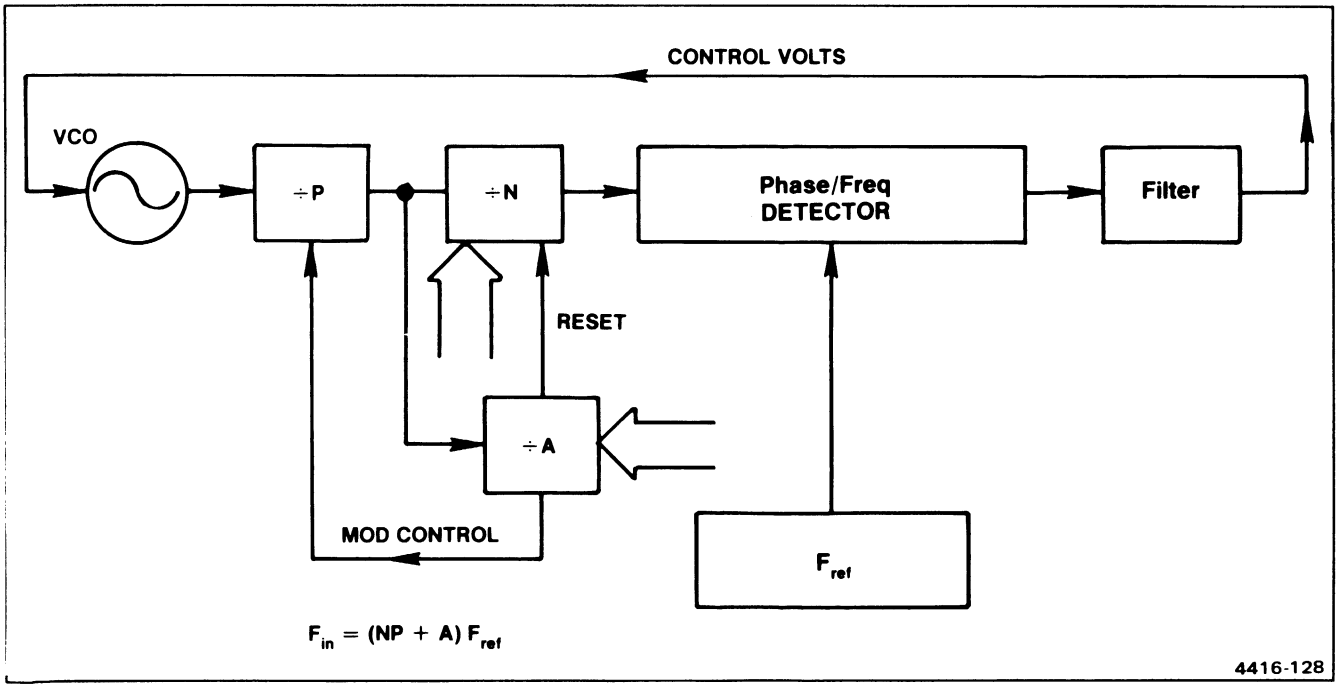


Figure 7-25. Basic block diagram of a ÷N synthesizer with a variable modulus prescaler.

This synthesizer uses a variable modulus prescaler to divide the VCO frequency before is processed by the "+N" counter, such as shown in Figure 7-25. The variable modulus prescaler is controlled by a modulus control input. When the line is high the prescaler is a divide by P+1 and when the line is low the division changes to P. A common type of prescaler is a +10/11. A cycle of system operation starts with all programmable counters loaded and ready to count. The variable modulus prescaler initially divides by P+1.

Two programmable dividers are used with this system, both triggered by the prescaler output. One is a +N, with N being a relatively large number, the other is a "+A", where A is a small number. One possible state includes A = 0.

The operation of this system is as follows. The lower case letters represent variables, the upper case letters represent the programmed values. At the beginning of the cycle, p=P+1, a=A, and n=N. After P+1 pulses from the VCO, one pulse is applied to the "a" and "n" counters and "a" and "n" decrease by 1 (a = A-1, n = N-1). This continues until a = 0 at which time the modulus control line changes state and p = P while n = N-A. The counting continues until n = 0. Both the "n" and "a" counters now return to the programmed condition. The total number of pulses applied from the VCO is:

$$N_{total} = (P+1)A + P(N-A) = A + PN$$

Both N and A are programmable such that $F_{vco} = (A + PN)F_{ref}$. This leads to a possible channel spacing of F_{ref}, obtained by changing A by 1.

A functional block diagram of the Auxiliary Synthesizer is shown adjacent to the schematic in the diagrams section. The VCO (Q2071) is configured in a Colpitts oscillator circuit with the inductance as a three turn air core coil with feedback provided by C2072 and C2071. Coarse tuning is accomplished with C1070, while the voltage control of the frequency comes from the varactor diode, CR2068. This diode provides a frequency shift of over 30 MHz from a voltage swing of +5 V to +11 V, which is ample overlap for the 20 MHz tuning range. The output power of the oscillator is 0 dBm into 50Ω. The oscillator is biased so it can be turned off and on rapidly.

The VCO is turned off by turning Q2076 on. In operation, the synthesizer is turned off during periods when information is presented on the CRT. Synthesis and counting is done during retrace time to prevent possible interference on the display from any radiated energy from the synthesizer.

The VCO output is split by a resistive power divider. One output drives transistor U2058, which provides +7 dBm of signal output to the Harmonic Mixer. This device is biased to a 20 mA collector current by transistor Q2055.

The other VCO output drives a low gain amplifier, Q2049, which is biased by transistor Q2051. Negative feedback, in the form of emitter degeneration and shunt current feedback, sets and stabilizes the gain to ensure stability with regards to spurious oscillations. The output of Q2049, to drive the variable modulus prescaler is 0 dBm. The variable modulus prescaler U3051, is a +32/33 IC that features an ECL input with a TTL or CMOS compatible output.

The major circuit of the synthesizer is U4041, a large-scale-integration, CMOS device for frequency synthesis applications with a variable modulus prescaler. The device contains three programmable counters; a +N, a modulus control counter +A, and a reference divider which divides an input from a crystal controlled source or other reference frequency down to a desired frequency. This device has a speed comparable to TTL. It also contains a phase-frequency detector which drives an external loop filter that uses an operational amplifier. U4041 will accept data for N, A, and R inputs from a 4-bit data bus while a 3-bit address bus selects the information to be loaded. Data contained on instrument bus lines DB4 to DB7 is loaded when the enable line goes high. Address information is contained on instrument bus lines DB0, DB1, and DB2. The appropriate 32 latches are also contained within this IC.

The output from the phase/frequency detector in U4041 is a chain of pulse signals at the reference frequency. The pulses contain both ac and dc components. The ac part of the signal causes reference sidebands to appear on the VCO output. These sidebands are suppressed by two active loop filters consisting of U2040A and U2040B. The detector outputs, ϕ_R and ϕ_V, which are similar but with reversed polarity, apply differentially to the input of U2040A. Slight differences in pulse width between the two outputs generate a dc voltage. This is further filtered by an active low-pass filter, U2040B, to suppress frequencies above 20 kHz. Then it is applied to the varactor diode CR2068 in the 200-220 MHz VCO.

U2040A is an integrator with a series resistor added to the feedback capacitor. This controls the slope of the loop gain at gain crossover. To provide additional suppression of the reference sidebands, an RC active two pole filter, U2040B, is added. Cutoff frequency is about 20 kHz. The loop filter (U2040A) and the VCO provide the dominant poles that determine the system response. A damping factor near unity provides the stability. Additional filtering in the form of passive components, with a high frequency cutoff, are added between the output of U2038B and the varactor diode

CR2068. CR1065 provides a clamp to prevent a control line voltage less than 5 V. Capacitor C1070 sets the low end of the control voltage to about 6 V. Range of the control voltage, over the 200-220 MHz VCO range, is about +6 V to +11 V.

The off/on status of the VCO is controlled by U4074 which is activated by D3 from the data bus. The value is latched in U4074 and its output turns Q2076 off or on. The output also controls the sensitivity of divider U5015. During the period when the VCO is off and there is no input signal, the divider sensitivity is lowered so stray signals will not activate the divider. This is done by turning Q5027 on and pulling input pin 6 of U5015 low.

The 100 MHz signal from the 3rd Converter is applied through a resistive power splitter to divider U2017 and to buffer amplifier Q1015. The 1 MHz output from the divider, U2017, is further divided by 5 within the synthesizer IC, to become the 200 kHz reference frequency for the synthesizer. The amplifier Q1015 has negative feedback for gain stabilization. Its output signal is applied to the counter board.

The 10-80 MHz signal from the harmonic mixer is passed through a 7-pole low-pass filter with 80 MHz cutoff. The signal is then amplified by U4021 with a broad band gain of about 24 dB.

COUNTER BOARD (Diagram 34)

The Counter board circuits and function are: 1) The address decoder which receives and decodes the talk and listen commands for the microcomputer. 2) The service request circuits that sense an impending loss of 1st LO phase lock and sends a service request to the microcomputer. It then cancels the request when directed by the microcomputer. 3) The data buffers transmit data to and from the microcomputer. 4) The input amplifiers and multiplexer amplify input signals up to TTL levels and then select which of the input signals is to be counted. 5) The $+2^n$ counter divides the selected input signal by some power of 2 as determined by the microcomputer. 6) The 21-bit counter counts at a 100 MHz rate for a given number of cycles of the selected input signal.

Address Decoder

The addresses from the microcomputer are decoded by address decoder U2040. The counter circuits have both a talk address, where the counter-buffer circuits are instructed to talk on the data bus, and a listen address, where U3024 is directed to receive data from the data bus. The talk address is F3; the listen address is 73.

Service Request Circuits

The service request circuits consist of multiplexer U3040, latch U3048B, and associated circuitry. This circuitry alerts the microcomputer in the event that the 1st LO has drifted too far. The UP and DOWN signals from the window comparator (located on the Error Amplifier board) drive NOR gate U3010C. Both signals are also sent to U3034, where their status can be read by the microcomputer. When one of these signals is high, it indicates that the Error Amplifier is approaching its operating limits and the microcomputer should adjust the 1st LO frequency so the Error Amplifier returns to the center of its range. A high at either input of U3010C produces a negative transition that is inverted by U3046C. C2050 pulls the set input of U3048B high for approximately 10 micros. The Q output of U3048B then goes high, causing Q4052 to pull the SR (service request) line low.

The Q-not output of U3048B pulls the G_1 and G_2 inputs of multiplexer U3040 low, enabling both sides. This device allows Q4034 and U3048B to respond to inquiries by the microcomputer to determine which address requested service. The microcomputer initiates the polling routine, which is to pull the POLL signal and AB7 high, then interrogate each data bus line in succession to determine which address requested service; i.e., which data line is low. To do this, the Y1 output of U3040 is set high, which causes Q4034 to pull the D2 line low. To affirm which address requested service, the microcomputer now causes the 7 address line to move low, which, via the Y2 line from U3040, clocks U3048B to the reset state as the microcomputer holds data bus line 2 low. This cancels the service request because it cuts off Q4052 permits its output to move high. In addition, the complement output of U3048B moves high, which disables the inputs to U3040. This brings the service request circuitry back to its original state.

Data Buffers

The data buffers consist of U3024, U3034, U3030, and U2026. U3024 is the listen buffer. When address decoder U2040 is addressed by the microcomputer to listen, it enables U3024, which passes on the buffered data to the other circuits in the Counter board. The function of each data bit is as follows:

D0—This line carries the serial data that selects which input signal is to be counted and what n numbers to use in the $+2^n$ counter. This data is loaded into shift register U1022. D0 also carries the data for the +N counter in the Phase Lock Synthesizer circuits.

D1—The N LATCH signal for the 1st LO phase lock is sent on this line.

D2—Reserved for future applications.

D3—This line resets the buffer sequencer at the outset of a talk cycle for the counters.

D4—This line (CONTROL LATCH) latches a control word into the output buffers of U2025 on the Error Amplifier board.

D5—This signal clears all the counter stages in the counter- buffer circuits in preparation for a count sequence.

D6—This line latches the N data in U1022.

D7—This line is used as a clock to step data into U1022 and U3048A, and for the data sent in the 1st LO phase lock. R3012 and C2010 act as a delay to provide adequate setup time for the data prior to the clock signal arriving.

Buffers U3034, U3030, and U2026 are the talk buffers that send data to the microcomputer. U3018 and U2030A make up a step-enabler that enables the talk buffers one at a time when requested by the microcomputer.

Input Amplifiers and Multiplexer

Q1018 brings the -5 dBm, 16 MHz to 20 MHz signal from the 2nd LO up to TTL levels. U2010 divides the 16-20 MHz by 32 and 256 before it sends it to multiplexer U1018. U2056 amplifies the -50 dBm, 10 MHz IF. L2056 and C2056 act as a 10 MHz bandpass filter on the input of U2056. R3056 provides current to the open collector output of U2056. C3052 couples the 10 MHz signal into U4056. U4056 acts as a divide-by-128 counter. The signal then goes to U1018.

All other input signals are at TTL levels and are connected directly to U1018. The ouput of U3010A is connected to U1018 so that the clock can be counted for diagnostic purposes. U1018 selects one of its inputs according to the data in U1022.

$\div 2^n$ Counter

The output of U1018 goes into a series of dividers made up of U1050 and U2050A. Various outputs of these dividers are connected to multiplexer U1046 to give a $+2^n$ counter where n = 1, 2, 4, 6, 8, 10, 11, or 12 (n is selected by the data stored in U1022). A strobe input to U1046 disables the multiplexer when pulled high.

21-Bit Counter

The 21-bit counter counts the 100 MHz reference frequency to give a measurement of the time required to complete a given number of cycles of the selected input signal. The counter itself consists of U1038, U2018, U1028, and U2034. U1038 is an ECL divider. Q1034 and Q1044 are ECL-to-TTL translators for the ÷2 and ÷4, respectively. The ÷4 goes to U2018 where it is counted with TTL dividers, and the divider chain continues through U2034. The output of each stage goes to an output buffer so the microcomputer can read the final number of counts. Therefore, measure the time period during which the counter was enabled. The counter is enabled by U2050B and U2046 for a time period equal to eight cycles of the output of the $+2^n$ counter.

At the start of a count, the microcomputer selects the input signal to be counted and selects the n number for the $+2^n$ counter. The COUNT/RESET line is then pulled high to reset all of the counters. U2046A is preset with Q in the high state, which disables the 21-bit counter. The COUNT/RESET line then goes high to start the measurement process. The output of U1046 goes to U2050B where it is further divided down. On the first rising edge at QA of U2050B, Q of U2046A goes low to start the 21-bit counter. On the eighth count of U2050B, U2046A steps back to its original state, which stops the 21-bit counter. At the same time, U2046B pulls the strobe to the $+2^n$ counter high to stop any further counts in U2050B. The microcomputer can now read the VALID COUNT line to determine when the count process is completed, and then read the data that is stored in the 21-bit counter.

PHASE LOCK SYNTHESIZER (Diagrams 35 and 36)

The Phase Lock Synthesizer provides frequency control and stability for the 1st local oscillator. The circuit consists of the Synthesizer and Phase Lock circuits. The Phase Lock assembly includes the Error Amplifier, Offset Mixer, Controlled Oscillator, and Strobe Driver. The Phase Gate Detector (shown on diagram 32) is also part of the phase lock ciruitry.

Synthesizer (Diagram 35)

The Synthesizer uses the 100 MHz reference frequency from the 3rd Converter to generate the 25 MHz reference frequency for the Offset Mixer and the +N frequency (determined by the N number from the Processor) for the phase/frequency detector in the Offset Mixer. The +N number is within the 32 kHz to 94kHz range.

The Synthesizer can be divided into three functional blocks: the 100 MHz divider, the 50 MHz divider, and the +N counter.

The 100 MHz divider consists of flip-flop U3030 and differential pair Q3040 and Q3041. The 100 MHz signal from the 3rd Converter stage is applied to the clock input of U3030. (One-half of U3030 is used to furnish a stable bias source for the clock input.) The 50 MHz signal from the Q output is applied through buffer amplifier Q3041 to P500; it is not used. The signal from the complement output of U3030 is applied through Q3040 to U1040B, the 50 MHz divider.

The 50 MHz divider consists of the flip-flop U1040B. The 50MHz from the collector of Q3040 is applied to the clock input of U1040B which divides the signal to 25 MHz. The signal from the Q output is sent to the Offset Mixer circuits. The complement signal is applied to the +N counter.

The +N counter consists of two shift register/latches U2020 and U2030; three counters, U2010, U1020, and U1030; and flip-flop U1040A. The circuit is controlled by three signals from the microcomputer via the Counter board. The output of the +N counter is a frequency within the range of 32 kHz to 94kHz which is applied to the phase/frequency detector in the Offset Mixer. When power is first applied, and before phase lock is selected, this counter typically outputs a frequency of approximately 6 kHz.

When phase lock operation is selected, the microcomputer sends data and a data clock to load a number into the latches, which accept and store serial data. The numbers that come from the microcomputer, range from about 3300 to 3830, so the count remaining, until the counters overflow, is from about 265 to 795. When the number is loaded, the N LATCH signal transfers the number from the input shift registers to the output registers of U2020 and U2030 where they are available to the counter stages. This presets the counters to a predetermined value, as just mentioned. Once loaded, the counters count at a 25 MHz rate to accumulate the remaining number of digits until they are full. The TC output of U1030 then moves high and U1040A changes state. This presets the N number in the counter stages for another count cycle. The TC output of U1030 is again simultaneously set low so the next cycle of the 25 MHz clocks U1040A back to the reset condition. The resultant output of U1040A is a series of positive pulses that range in period from 10 μs to 31 μs which is equivalent to 94 kHz to 32 kHz. This signal is sent to the phase/frequency detector in the Offset Mixer for comparison with the difference frequency generated in the mixer circuit.

Phase Lock (Diagram 36)

The Phase Lock circuits lock the 1st LO, using the Synthesizer as a reference. The circuits shown on this diagram include the Offset Mixer (A50A3, Error Amplifier (A50A4), Controlled Oscillator (A50A5), and Strobe Driver (A50A2). The 1st LO (A16) and the Phase Gate Detector (A24) are also major parts of the phase lock circuitry.

Offset Mixer. The Offset Mixer (A50A3) circuits mix the synthesizer and VCO outputs and compare phase and frequency with the divide-by-N frequency from the synthesizer. The resulting error signal drives the inner loop amplifier on the Error Amplifier board (A50A4).

The circuits consist of a ring diode mixer, differential amplifier, and phase/frequency detector. For this explanation, assume that the Controlled Oscillator (VCO) frequency is at 25.06 MHz and the +N signal is 50 kHz. The 25.06 MHz signal from the VCO enters the board at pin N of the Offset Mixer assembly. The signal drives the base of transistor Q2021 which drives transformer T2010. The transformer output connects across the ring diode mixer. The 25 MHz reference frequency is applied at pin K of the Offset Mixer and coupled through T1010 to the ring diode mixer. The four frequency components are picked off at the center tap of T2010. A low-pass filter passes the 60 kHz difference frequency and blocks the two fundamental frequencies and their sum.

Transformer T2030 couples the 60 kHz signal to differential pair Q1020 and Q1030. Then Q1040 amplifies the signal to TTL levels and applies it to the clock input of flip-flop U1050B, part of the phase/frequency detector.

The phase/frequency detector consists of flip-flops U1050A and U1050B, NAND gate U2050B, and inverter U2050A. Now, if the loop had been locked, the two flip-flop clock input signals would have been edge-coincident. Pin 4 and 5 inputs of U2050B would have moved high and after the signal at TP1058 goes low, the NAND gate would have reset both flip-flops. This results in a series of pulses of equal amplitude and width from each of the flip-flops which, when applied to the Error Amplifier, would not shift the frequency of the VCO.

However, in this example the +N signal is 50 kHz and the difference frequency from Q1040 is 60 kHz. Thus, Q1040's output leads the +N signal. In this case, U1050B will clock first, placing a high at the Error Amplifier's inverting input. This ramps the amplifier output low until U1050A switches a short time later. U2050B resets both flip-flops and the inner loop error amplifier will stop ramping until the next correction

cycle. At the next correction cycle, the error amplifier will have reduced the VCO frequency, therefore reducing the mixer difference frequency. This process continues until the two signals applied to the Phase/Frequency Detector are edge coincident, meaning that their frequencies and phase match.

Error Amplifier. The Error Amplifier board (A50A4) provides the inner and outer loop error amplifiers, enables the Strobe Driver (A50A2), and generates the UP/DOWN and F ERROR signals.

The inner loop amplifier integrates the error signals from the Offset Mixer and produces a correction voltage to pull the VCO to a frequency that is synchronous with the +N signal. The Output Mixer (A50A3) phase/frequency detector output drives integrating differential amplifier U3075. As the signals driving the amplifier continue toward one direction, the output continues to change the oscillator frequency in the appropriate direction. Zener diode VR2065 and CR3069 clamp the inner loop amplifier output so that it stays above +5 V. This prevents forward biasing the VCO varactor diodes.

The digital control circuits consist of shift register U2025 and quad analog switch U2037. Data from the microcomputer is fed serially, via the Counter board circuits, into the shift register, then transferred to the output lines by the CONTROL LATCH signal. Table 7-16 lists the purpose of the output lines.

Table 7-16
U2025 OUTPUT LINES

Line	High	Low
Q1	Window disabled[a]	Wide window[a]
Q2	Lock	Unlock
Q3	Wide loop	Narrow loop
Q4	Strobe enabled	Strobe disabled
Q5	Narrow window	Wide window[b]

[a]With Q5 low.
[b]With Q1 low.

The outer loop amplifier circuit consists of amplifier U2048 and surrounding components. The ERROR signal from the Phase Gate Detector and Error Amplifier is applied through LOOP GAIN adjustment R3082 to the inverting input of U2048. The signal (ERROR) is a result of the comparison of the 1st Local Oscillator frequency and the nearest multiple of the STROBE signal from the Strobe Driver circuit. The ERROR signal varies from zero to about 500 kHz, and is up to 4 V peak-to-peak in amplitude.

When phase lock is not required, data into U2025 sets output Q2 and Q4 low and Q3 high. This opens the connection between pins 11 and 10 of U2037 and the connection between pins 2 and 3. STROBE ENABLE line to the Strobe Driver goes high and disables the strobe pulse. The FM coil of the oscillator is opened by U2037 which opens the outer loop.

To establish phase lock, the microprocessor sets the 1st LO near the desired lock point and loads the proper N number into the synthesizer. The 5 MHz strobe is then turned on (Q4 and Q2 output of U2025 set high) and the microprocessor tunes the 1st LO up or down 750 kHz either side of the desired lock point at a 10 Hz rate. When the oscillator frequency crosses the desired lock point, the ERROR frequency is reduced to a dc voltage which results in U2048 pulling the 1st LO in the direction required to maintain a constant frequency. When the microprocessor measures the 1st LO frequency and finds it held constant, at the desired frequency, it then sets Q3 output of U2025 low to reduce the bandwidth of the phase lock loop.

The UP and DOWN signals alert the microcomputer that the drive current to the 1st LO FM coil is reaching its limit in holding the 1st LO in phase lock. The microcomputer then acts to bring the 1st LO frequency within the proper range. A window comparator, consisting of U1015 and the associated components, senses when U2048 has approached its operating limits. When the microcomputer causes the Q2 signal to close the path from U2048 to the FM coil, U2048 begins to furnish current to the coil which causes the 1st LO to track the stable strobe signal. That is, each time the 1st LO frequency drifts, the ERROR signal changes and U2048 shifts the FM coil current to bring the 1st LO back to its original frequency. At the same time, the microcomputer causes lines Q1 and Q5 to be low, closing the contacts that connect the output of U2048 to the input of the window comparator through a divider network. Now, as the 1st LO frequency drifts, the loop amplifier will compensate for the drift. If the drift is excessive, however, U2048 will approach its limits and will be unable to furnish any more current to the FM coil.

Window comparator U1015 is a dual comparator that senses a deviation of ±15 mV. For example, if a frequency shift forces U2048 to move positive enough (approximately 3 V), the upper half of the comparator conducts, and the UP line goes high. This triggers the service request circuits on the Counter board, which in turn alerts the microcomputer so it begins adjusting the TUNE voltage from the Center Frequency Control circuits to reduce U2048 output to zero. If the output drifts negative, the other half of U1015 conducts, causing reverse action to occur.

Normally, the input signal to the window comparator is attenuated by R2043, which reduces the voltage applied to U1015 to 0.3% of the output from U2048.

This allows U2048 to drift up and down without immediately triggering either comparator. When R2043 is in the circuit, it is called "wide window" operation. When phase lock is de-selected, the microcomputer selects narrow window (which bypasses R2043). The Center Frequency Control circuit is then instructed by the microcomputer to move the 1st LO frequency until the window comparator indicates that the FM coil current is near zero. This prevents the 1st LO frequency from shifting too far from the lock point when phase lock is canceled.

The F ERROR signal is used by the Counter board (A51) for diagnostics so that the microcomputer can determine the relationship between 1st LO frequency and the strobe line. The F ERROR signal is generated from the outer loop ERROR signal from the Phase Gate Detector (A24). The circuit consists of an active low-pass filter U2065 and Schmitt trigger U1035. This circuit filters and squares the incoming ERROR signal. The ERROR signal is applied through C2067 to an RC 500 kHz low-pass filter and amplifier U2065. After filtering, the signal is applied through Error Count Breakpoint adjustment R1061 to the input of U1035, a Schmitt trigger circuit. The squared output signal is then applied to circuits on the Counter board.

The STROBE ENABLE signal enables the strobe generator in the Strobe Driver circuit (A50A2). Shift register U2025 reads the instrument bus latch on the Counter board (A51) to determine the status of the STROBE ENABLE signal. Q2030 inverts the signal and converts it to TTL level to drive the strobe generator.

Controlled Oscillator (VCO). The Controlled Oscillator (VCO) is a voltage-controlled crystal oscillator whose frequency is controlled by the output of the Error Amplifier. The oscillator generates a reference signal that is used to stabilize the 1st LO frequency. Refer to the block diagram adjacent to Diagram 36 for a functional description of this part.

The control voltage from the Error Amplifier, which is a function of the difference between the microcomputer controlled +N signal and the Offset Mixer difference frequency, is applied to the VCO on the Controlled Oscillator board to regulate its frequency of operation. The circuit has two outputs: the first, which is part of the inner loop of the phase lock circuits, is fed to the Offset Mixer, where it is used to derive the difference frequency that is compared against the +N signal. The second output, which is part of the outer loop, is fed to the Strobe Driver circuits, where it is divided down to become the STROBE signal that is compared against the 1st LO signal in the Phase Gate.

The VCO consists of five major circuits, four of which are connected in a positive feedback loop to sustain oscillation. These circuits are the resonator stage, the differential amplifier, the bandpass filter, the isolation amplifier, and the output amplifier. The resonator stage operates at a frequency of 25.032 MHz to 25.094 MHz. The output signal from the resonator is applied to the input of a differential amplifier which drives the output amplifier and the bandpass filter. The output from the output amplifier is fed to the Offset Mixer and the Strobe Driver. The bandpass filter strips the signal of any spurii either side of center frequency and feeds the signal to the isolation amplifier. This stage furnishes the positive feedback drive to the resonator stage and isolates the bandpass filter from the resonator stage.

The resonator stage consists of crystal Y1012, varactor diodes CR1011 and CR1012, and related components. The stage operates within the frequency range of 25.032 MHz to 25.094 MHz, which is controlled by the voltage applied to varactor diodes CR1011 and CR1012. Feedback energy for sustaining oscillations comes from the isolation amplifier by way of coil L1025.

The resonator output signal is applied to a differential amplifier Q2033 and Q2041. The Q2033 side drives the output amplifier and serves to isolate the output load from the feedback loop. Gain from this side is less than one. The signal is fed from the collector of Q2041, following amplification, to the band-pass filter.

The band-pass filter consists of passive components, and is used to strip the signal of any frequency components more than about 40 kHz away from the center operating frequency, which is approximately 25.06 MHz. Capacitors C1041 and C1042 are adjusted at the factory to set the bandwidth and center the frequency of the filter.

The isolation amplifier, Q1028, is a common-base configuration, in order to match the impedance of the filter to the resonator. Output current from the stage furnishes positive feedback for the resonator.

The output amplifier, consisting of transistors Q2025 and Q2026, is connected as a differential amplifier with Q2026 driving one side of the Offset Mixer and Q2025 driving the input of the Strobe Driver circuit, for eventual application to the Phase Gate circuits.

Strobe Driver Circuit. The Strobe Driver circuit consists of counter U1022, bandpass filter FL2064, source follower Q2091, and AND gates U1091A and U1091B.

The VCO output is applied to the clock input of divide-by-5 counter U1022. The STROBE ENABLE line from the Error Amplifier permits the counter to operate

when the line is low and is the means by which the microcomputer can turn the strobe pulses on or off. The counter output couples through an impedance matching network consisting of C2030, L1031, C2033, and C1032, to the input of bandpass filter FL2064. The impedance matching circuit raises the line impedance to about 8200 ohms.

The output of the filter drives another impedance matching network for the gate input of Q2091. The output of Q2091 drives two buffer amplifiers U1091A and U1091B. U1091B drives the Phase Gate circuitry, and U1091A is reserved for future applications. Capacitors C1032 and C2105 are selected to provide maximum signal amplitude at TP2087.

DIGITAL CONTROL (Diagram 8)

The Digital Control section provides operator and digital controller interfaces. It translates changes in front-panel controls and also translates instructions received via the GPIB into codes that control the instrument.

The user interface to the digital control operating program is discussed in the Operators and Programmers manuals. This description focuses on the major circuits that make up the Digital Control section. Those circuits are:

- Microcomputer
- Addressable registers on the instrument bus
- Front panel
- Accessories Interface
- GPIB Interface

Microcomputer

The Microcomputer system receives inputs from the front-panel controls, the instrument circuits and the GPIB , and sends control codes to the instrument hardware to set it for desired operation. The Microcomputer consists of a microprocessor, memory, various input/output (I/O) circuits, and associated bus structures. The circuits are located on the Processor (A58), Memory (A54), and GPIB (A56) assemblies.

The microcomputer is centered around a microprocessor. Input/output (I/O) is provided by a Timer, a Peripheral Interface Adapter (PIA), a Direct Memory Access (DMA) controller and a General Purpose Interface Adapter (GPIA). System memory includes both read-only-memory (ROM) and random-access-memory (RAM). The ROM contains the instrument operating system and other firmware. Front-panel control settings, displays, and calibration information are stored in non-volatile RAM. This RAM has battery backup power to retain the data when instrument power is off. The instrument operating system uses additional RAM.

The microprocessor communicates with the memory and I/O ports via the microcomputer bus. Communication with the rest of the instrument is via the instrument bus.

Interrupts from various circuits can request processor service. The firmware contains a service routine for each of the interrupts. If necessary, the processor can mask, or ignore, all interrupts except for a power failure interrupt.

The accompanying illustrations show the address allocations for the microcomputer. These will be useful for the following descriptions. Figure 7-26 shows the entire address range of the processor. Figure 7-27 shows the I/O address range. Figure 7-28 shows PIA and Timer memory maps. Unless otherwise noted, all addresses are in hexadecimal.

Processor (Diagram 37)

The Processor board (A58) contains the microprocessor and most of its peripheral devices that compose the computer system.

Microprocessor. The microprocessor, U1025, processes data, generates addresses and control signals, and controls the operation of the instrument. The microprocessor, a 6808 (also known as 67127), has an 8-bit bi-directional data bus and a 16-bit address bus.

Output signals include the $\phi 2$ Clock (Enable), Read/Write (R/W), Bus Available (BA), and microprocessor Valid Memory Address (VMA).

The microprocessor divides the CRT Clock signal by four, producing an internal two-phase clock. This clock is available at the microprocessor's Enable output as a signal labeled $\phi 2$ Clock. The 853.3 kHz $\phi 2$ Clock drives the Timer, PIA, and DMA Controller, and it is one of the control lines available on the microcomputer bus.

The Read/Write line indicates to the peripheral and memory circuits whether the microprocessor is in the read state (high) or the write state (low). The read state is the normal standby condition and a response to a halt signal. U1030B and U2030F buffer the R/W signal to drive the various circuits.

The Bus Available signal goes high to indicate when the microprocessor releases the data bus. This occurs when the microprocessor executes a WAIT or when the HALT Input goes low.

A high VMA signal tells the memory circuits that there is a valid address on the microcomputer address bus. U3036D issues the VMA signal to the memory circuits from either the microprocessor or the DMA Controller.

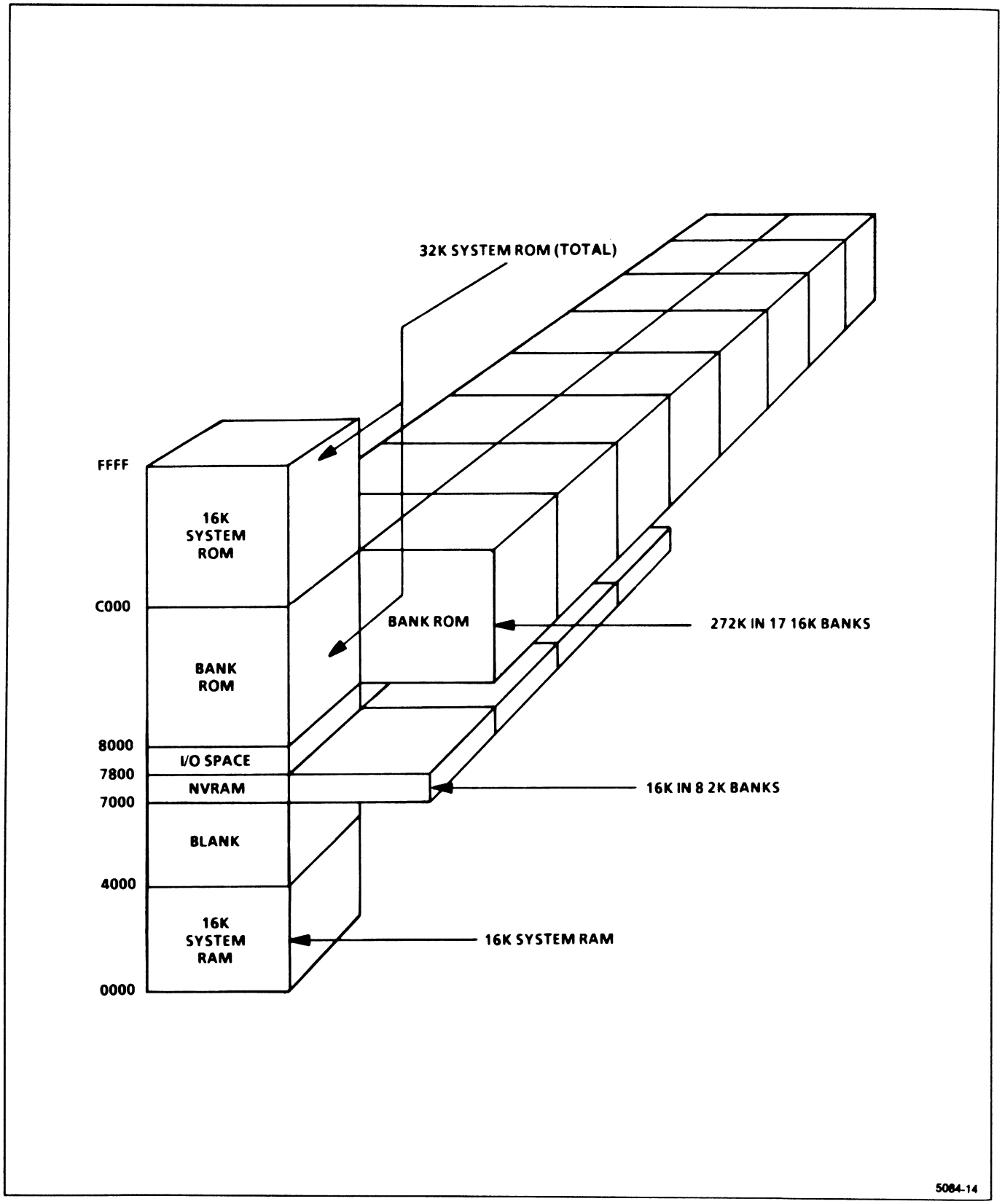


Figure 7-26. System memory map.

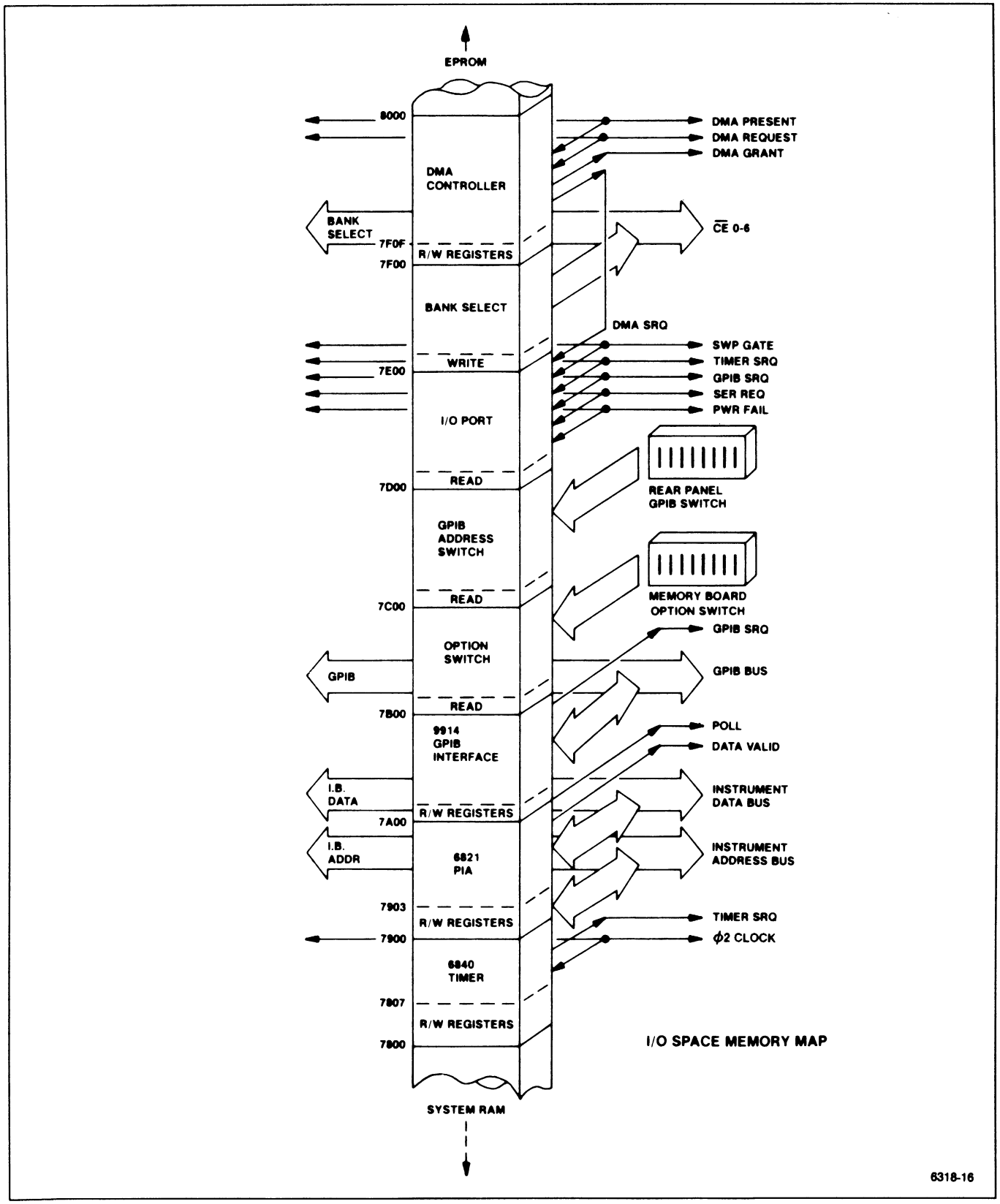


Figure 7-27. I/O address space.

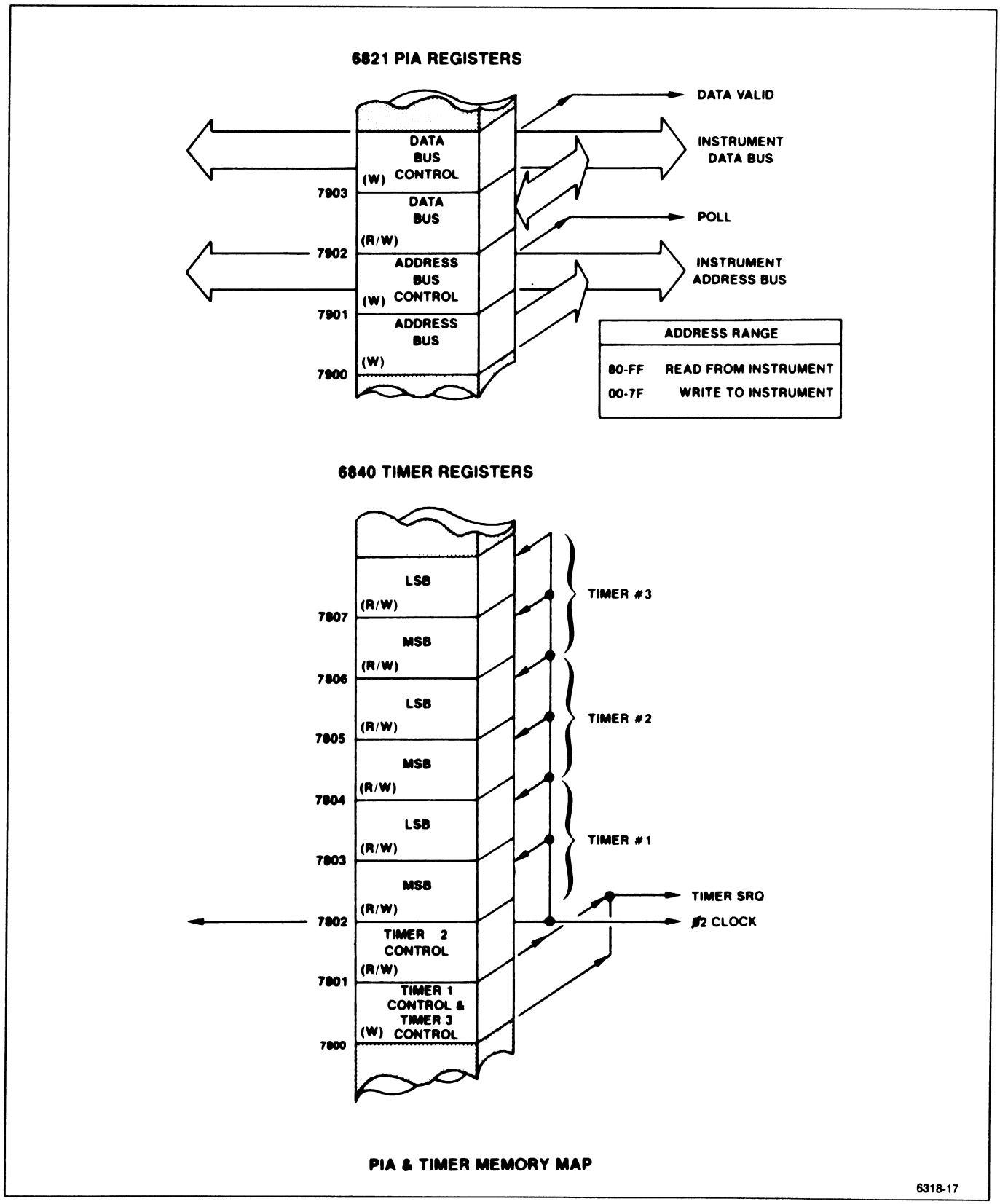


Figure 7-28. PIA and Timer address map.

Clock. This circuit generates the clock signal that drives the microprocessor, the GPIA transceiver on the GPIB board (A56), and the character generator circuitry on the CRT Readout board (A66A1).

Y1030, Q2035, and Q1030 form a clock circuit that oscillates at 3.4133 MHz. Q2035 and Y1030 form a Colpitts oscillator and Q1030 buffers the output, giving a TTL compatible clock signal. This signal is further buffered by U2030A.

Microcomputer Bus. Microcomputer communication with memory and I/O is via the microcomputer bus. The bus consists of eight data lines (D0-D7), sixteen address lines (A0-A15), the RESET line, the VMA (Valid Memory Address) line, the Read/Write (R/W) line, and the ϕ2 Clock.

The data lines connect from the microprocessor through bi-directional buffer U2025. The Read/Write line controls data direction through the buffer. When the microprocessor releases the address bus, the Bus Available line (BA) disables the data bus buffers through U3036A. Jumper P3015 is a test jumper that allows disabling the data buffer and forcing a CLR B instruction to the microprocessor. Diodes CR2020 and CR2025 pull data lines MD5 and MD7 low, issuing the CLR B instruction.

The address lines connect from the microprocessor through buffers U3030 and U3025. These buffers are disabled when the DMA Controller is granted the address bus. Then the addresses come from the DMA Controller, U1020, through DMA address buffers U1015 and U1024. U1015 is a bi-directional buffer, allowing the microprocessor to address the DMA Controller.

The RESET signal is a function of the Power Failure circuit. When a power failure is sensed, the RESET signal resets the Timer, PIA, DMA Controller, and circuits on the Memory (A54) and GPIB (A56) boards. The Power Fail circuit is discussed in more detail later. The VMA, R/W, and ϕ2 Clock signals have already been described.

Address Decoder. U3035 decodes the addresses for the I/O circuits on this board. When the microprocessor selects an address in the range of 7800-7FFF, the I/O line from the Memory board (A54) goes low, enabling U3035. The decoder then subdivides the address range to select each circuit. Figure 7-27 shows the I/O address map. Each circuit uses only one or a few addresses within its range.

Timer. The Timer circuit, U2015, is a 6840 programmable timer used by the microprocessor to generate variable time delays. The processor programs an interval into the timer. When the interval passes, the Timer generates an interrupt (Timer SRQ). The ϕ2 Clock synchronizes the Timer with the microprocessor. An address in the timer range selects the Timer. Address bits A0-A2 select internal Timer registers, counters, and latches. When the Read/Write (R/W) line is low, the Timer accepts data input from the data bus. When the line is high, the Timer puts its data on the data bus. See a 6840 data sheet for additional details. The Timer addressing is mapped in Figure 7-28.

PIA and Instrument Bus. The microcomputer communicates with the instrument through the Instrument Bus. The 6821 PIA, U1010, interfaces the Digital Control circuits to the Instrument Bus. This bus contains eight data lines (DB0-DB7), eight address lines (AB0-AB7), the DATA VALID line, the Service Request (SER REQ or SR) line, and the POLL line, all through the PIA.

The PIA receives Read/Write, ϕ2 Clock, and RESET control signals from the microprocessor. Figure 7-28 shows the PIA address map.

The address lines are buffered by U3015. The data lines are buffered by bi-directional buffer U3010. The buffer is gated on when data is valid. The most significant address bit selects data direction so that half of the address space is for writing to the instrument, and half is for reading from the instrument. The PIA CB2 port (U1010 pin 19) goes low when the data on the Instrument Bus is valid. A resistor-capacitor circuit delays the DATA VALID signal to the Instrument Bus, assuring the proper timing relationship with the other Instrument Bus signals.

The PIA issues the POLL and DATA VALID (or DV) signals in response to a service request from the hardware on the Instrument Bus. The requesting circuit responds to the POLL signal on the Instrument Data Bus.

The Internal Control (INTL CONT) signal comes from the Accessories Interface assembly (A30A76). This signal is normally high unless external control through the ACCESSORIES connector is desired. When low, the Bus Enable signal goes high, disabling the address and data buffers and the DATA VALID and POLL outputs. The Bus Enable jumper, P3010, may be removed to disable the Instrument Bus for test purposes.

DMA Controller. When the instrument transfers data through the GPIB interface, the DMA Controller, U1020, sets up direct transfers between system RAM and the

GPIA interface circuit on the GPIB board (A56).

Before each transfer, the microprocessor loads U1020 with the starting address of the RAM data and the number of data bytes to be transferred. When the GPIA interface circuit requires data, it pulls the DMA Request line, pin 4 of P1035, low. This causes U1030C to set U1020's Transfer Request input high, requesting a byte. In return, the DMA Controller sends a DMA request to the processor's HALT input, pulling it low. This also disables any maskable interrupt request to the processor. With HALT low, the microprocessor completes its currently executing instruction and then stops, signals that the bus is available (sets the BA line high), tri-states its data bus, and sets itself in the Read state (R/W line high).

The BA signal disables the microprocessor address buffers, U3030 and U3025, and enables DMA Controller access to the address bus via buffer U1024 and transceiver U1015. It also gives bus control to the DMA Controller. The least significant address lines are interfaced to U1020 through a transceiver because the processor uses addresses A0 through A4 to access the setup registers in the DMA Controller.

The DMA Controller sets the address, VMA, and Read/Write (R/W) lines to cause the RAM to place the proper byte on the data bus. Because U1030 is an open-collector gate, there is no conflict between the microprocessor and the DMA Controller over the R/W line.

The DMA Controller Transfer Strobe (TxSTB) output goes low giving the DMA GRANT signal to the GPIA circuit on the GPIB board. This informs the circuit that data is coming. After the transfer is completed, U1020 raises the HALT line, and normal processor operation resumes.

Ground from the GPIB board connects through pin 2 of P1035 as a signal that the Processor and GPIB boards are connected. If the GPIB board is not present, such as for test purposes, U1035 pin 12 goes low. This disables the DMA request.

Interrupt Processing. The microprocessor uses both maskable and non-maskable interrupts. The non-maskable interrupt is used only for sensing power-fail. The maskable interrupt is used to sense circuits requesting service. Although these interrupts may be masked by the processor, they are enabled most of the time. These interrupts can be requested by circuits on the Instrument Bus, the GPIB board, the DMA Controller, or the Timer. The instrument firmware contains service routines for each of the interrupts.

The maskable interrupts are sensed at the microprocessor's Interrupt Request (IRQ) input. Gates U2036, U1030, and U1035 set IRQ low if any of the interrupt lines go low. The Input Port buffer U3020 places the interrupt information and sweep information on the data bus. This allows the microprocessor to read the interrupt status.

If the interrupt is from circuits on the Instrument Bus, the microprocessor executes a poll routine to determine the exact cause of the interrupt. The Instrument Bus circuits interrupt the microprocessor by pulling the Service Request (SER REQ or SR) line low. The microprocessor responds by placing address FF on the Instrument Bus and setting the DATA VALID and POLL signals high. This causes the circuit that requested service to pull one of the data lines low.

Each circuit is assigned a different line, as shown in Table 7-17. It is possible that more than one circuit requests service at the same time. In that case, more than one data line will be low.

The microprocessor reads the data lines to determine the interrupting circuit or circuits. It then writes the corresponding bit pattern to the data bus while the address lines are set to 7F and DATA VALID and POLL are both high. When an interrupting circuit receives a low on its assigned data line with the address lines, DATA VALID, and POLL set as described, it resets its internal interrupt latch and releases the Service Request (sets SER REQ or SR high).

Table 7-17
POLL BITS

Bit 7	Not Used
Bit 6	Not Used
Bit 5	Not Used
Bit 4	End of Sweep
Bit 3	FREQUENCY knob
Bit 2	Phase Lock
Bit 1	Not Used
Bit 0	Front Panel

The non-maskable interrupt signals power loss. Circuitry on the Z-Axis assembly (A70) senses power loss and sets the PWR FAIL line low. This causes an interrupt and starts the microprocessor's power fail routine.

When PWR FAIL goes low, Q2030 turns on and C2030 begins to discharge through R1037. If the line stays low until C2030 discharges, the RESET line goes low and the microprocessor resets itself. As part of its power fail routing, the microprocessor monitors the PWR FAIL, along with other interrupts, through U3020. If the PWR FAIL line returns to a high state before the microprocessor is reset, the microprocessor does a

power-up initialization to ensure that the instrument operation will not be affected by a temporary power loss.

This power fail sequence can be disabled by removing jumper W2035. This may prevent false resets when operating the instrument on noisy power. However, power-down settings will not be stored.

Memory (Diagram 38)

The Memory board (A54) contains some of the ROM and all of the RAM used by the microprocessor. There are 64K[1] bytes of ROM in two 32K byte EPROMs and 32K bytes of RAM in four 8K byte RAMs. Battery backup power is supplied for 16K of the RAM. The board also contains the Options switch, which sets some instrument operations and selects processor test modes. Additional ROM is located on the GPIB board (A56).

Address Decoders. The address decoding circuits monitor the microcomputer bus to enable circuits on the board. Decoder U2045 is the main address decoder, selecting four 16K-byte blocks of address space:

0000-3FFF for RAM
4000-7FFF for NVRAM and I/O
8000-BFFF for Bank ROM
C000-FFFF for system ROM

The upper half of U2045 decodes the non-volatile RAM and I/O space. The lower half decodes the system RAM and ROM. The $\phi 2$ Clock signal clocks the lower half of U2045 to assure proper memory timing.

The system RAM address space is the 16K bytes from 0000-3FFF. The 2K space from 7000-77FF is switched between eight 2K banks of the 16K non-volatile RAM.

The system RAM address space is divided between two 8K RAMs, U1010 and U3020. The lower half of U2045 and the upper half of U3025 decode addresses from 0000-3FFF. This enables U1010 for addresses 0000-1FFF and U3020 for addresses 2000-3FFF.

The non-volatile RAM is bank switched into eight 2K banks addressed from 7000 through 77FF. This allows more memory than the processor can directly address. At address 7E00, the bank select circuit on the GPIB board (A56) enables latch U4020. The latch holds the RAM bank number from bits D5-D7 of the microcomputer data bus.

[1] $K = 2^{10} = 1024$

Latched bit D7, 1 $\phi 2$ clk, and 7000 address enable from U3040 drive the lower half of U3025 for the 7000-77FF address space. If D7 is low, U1030 is enabled; if high, U1020 is enabled. The other two bank select bits, D5 and D6, directly drive two address lines, creating four banks in each of the 8K RAMs.

The I/O space is decoded by the upper half of U2045, U3040, and U3045. The upper half of U2045 enables U3040 for addresses from 4000-7FFF. U3040 then decodes the 7800-7FFF address for Options circuit and other I/O space. This line is sent off the board as the I/O signal. The Options circuit is addressed at 7B00 by U3045.

ROM address decoding is performed by the lower half of U2045, data bit D4, some gates, and the bank select circuits on the GPIB board (A56). Half of ROM U3050 is addressed as bank ROM from address 8000 through BFFF. The other half of U3050 is system ROM addressed at C000 through FFFF. The bank ROM address space is shared with 16 other ROM banks. Latch U4020 stores data bit D4 at address 7E00 (Bank enable). When that bit is high, and when the ROM banks are addressed, U3050 is selected. The latched bit enables U3050 through U3030D. For system ROM addresses, the CXXX enable through U3030C and U3030D, and through U2040C and U2040D enables U3050.

U3060 is selected as banks 0 and 1 by the bank select circuit on the ROM Banks and GPIB board (A56). The upper and lower addresses are selected by data bit D0 latched by U4020 at address 7E00.

RAM. The RAM is divided into system RAM and non-volatile RAM. The microcomputer uses the system RAM for interim data storage while the instrument is operating. The non-volatile RAM stores changeable data such as waveforms, readouts, and front-panel set-ups. The non-volatile data is backed up by battery power when the instrument is not operating.

U1010 and U3020 form the main system RAM. Each IC contains 8K bytes of RAM, making 16K bytes total system RAM.

U1020 and U1030 form the battery-backed-up non-volatile RAM. When the instrument is operating, these RAMs are powered by the +5 volt supply. When the instrument is not operating, the RAMs are powered by lithium battery BT2040, or in option 39, silver batteries (Eveready 392 or equivalent). See the Maintenance section for replacement information.

Each of the non-volatile memory ICs require less than 2 μA. They will hold data as long as the battery voltage is above 2.5 V. In the battery circuit, R1030 and R2037 protect the battery against accidental short circuits. The jumper on pins 1 and 2 of P1040 provides an easy way to remove power, thus clearing all data in the RAM.

The microprocessor uses flip-flop U4030 to power-up and enable the battery-backed-up RAMs. Initially, U4030 is reset by the RESET line going low. This disables the non-volatile RAMs, U1020 and U1030. As part of the initialization sequence, the microprocessor writes to instrument bus address 73 to set U4030's output high. (U4040 decodes bus address 73). This allows C2030 to charge to +5 V, turning on Q2025, Q2035, and Q2037. Q2037 connects the +5 V supply to the RAMs' power-supply inputs, back-biasing CR1030 and disconnecting the battery. Q2025 turns on Q2030, pulling the CE inputs low, allowing the microprocessor to use the RAMs.

On power-down the microprocessor sets the output of U4030 low. After C2030 discharges, Q2025, Q2030, Q2035, and Q2037 switch off. R2032 pulls the CE1 lines high, to the RAM supply voltage, disabling the memory. As the supply voltage falls, CR2030 switches off, and the battery begins supplying power to the RAMs. R2036 and R3034 insure that the CE2 lines are grounded, not floating, in the standby condition, as is required for lowest current drain.

Options. The Options Switch settings tell the microcomputer which instrument options are installed so that the appropriate firmware is used. It also enables diagnostic checks and allows reporting settings over the GPIB in Talk Only mode. Figure 7-29 shows the switch settings. See the Maintenance section for more information about using the switches.

Octal switch S1050, buffer U2050, and decoder U3045 form the Options Switch circuit. The decoder enables the buffer at address of 7B00. An open switch is read by the microcomputer as a 1, and a closed switch is read as a 0. When addressed, the buffer places the switch data on the microcomputer data bus.

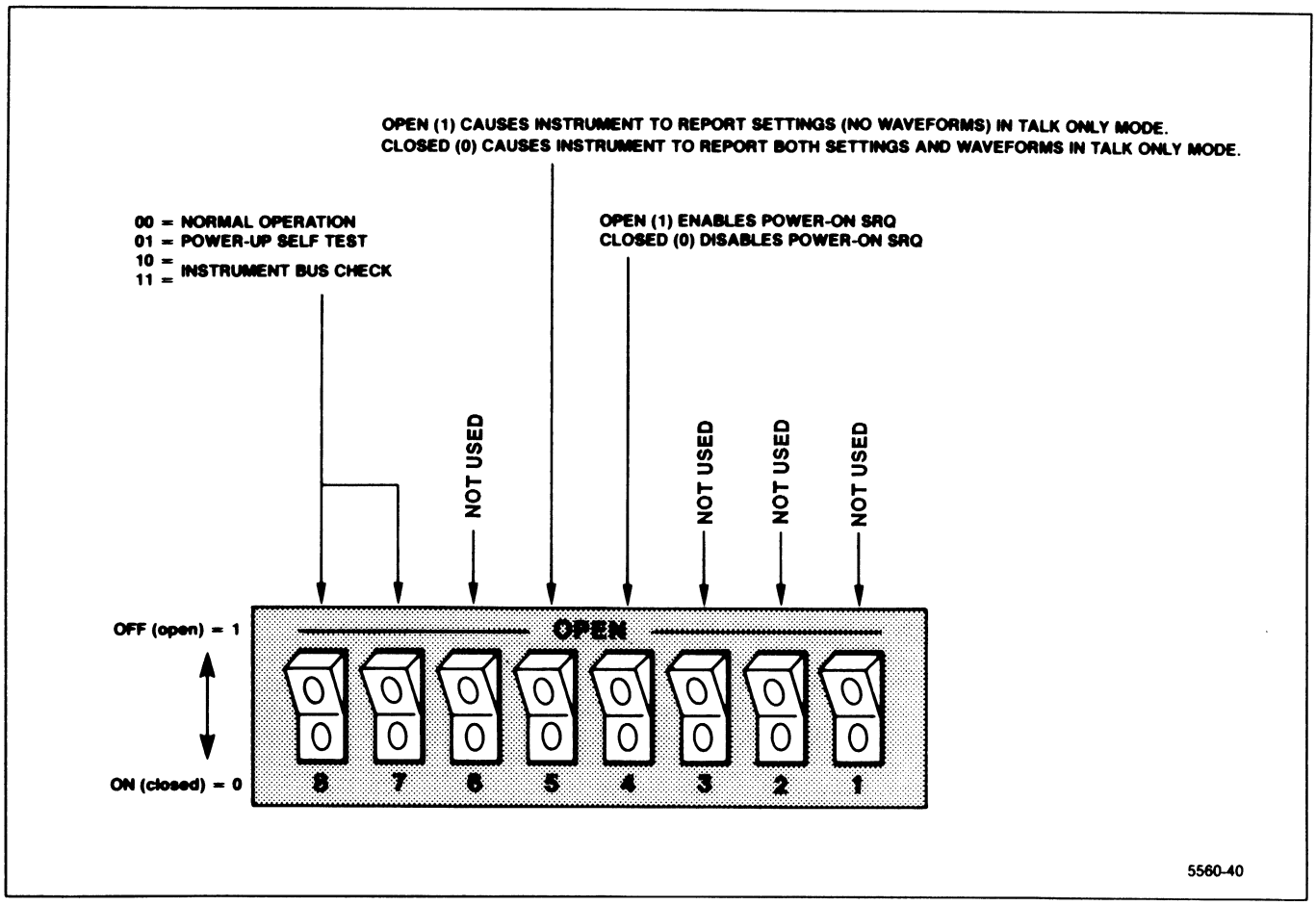


Figure 7-29. Options switch bank on the Memory board.

ROM. The ROM in this instrument is located on this board and on the ROM Banks & GPIB board (A56). The ROM consists of system ROM containing the instrument operating system and the program ROM containing the various measurements routines and crt messages. The system ROM is always accessible, while the program ROM is bank switched as necessary. Bank switching allows expanded memory within a limited address space. The system ROM and part of the bank-switched ROM are located on this board. The remaining bank-switched ROM and the bank switching circuitry are located on the GPIB board (A56).

The ROM ICs are 32K-by-8 bit erasable programmable read-only-memories with fifteen address lines and eight data lines. Each contain 32K bytes of data.

U3050 includes the system ROM and one bank of the bank-switched ROM. The ROM from C000-FFFF is the system ROM, always accessible from any of the bank ROMs. The ROM from 8000-BFFF is a ROM bank. U2040C and U2040D allow both the 8000 and C000 address selection lines from U2045 to select the same physical ROM. The two halves are selected by address bit A14. For addresses C000-FFFF, A14 is high. This address range is also enabled through U3030C and U3030D.

For the bank addresses, 8000-BFFF, A14 is low. Data bit D4 must be high when stored at the bank select address, 7E00, by latch U4020. This enables U3050 through U3030D.

U3060 comprises ROM banks 0 and 1. This IC is selected when the processor addresses the range 8000-BFFF and when the CE0 signal from the GPIB board (A56) is active (low). Selection between banks 0 and 1 is done by the bank-select bit latched from D0 by U4020. This latch is enabled when the BANK signal (at address 7E00) goes low from the GPIB board (A56).

ROM Banks and GPIB (Diagram 39)

The GPIB board (A56) contains most of the instrument's bank-switched ROM and the General Purpose Interface Bus (GPIB) circuits. The GPIB Interface board (A30A57) connects the instrument to the GPIB (IEEE Std 488 bus).

Address Decoder. Decoder U1055, gated by the $\phi 2$ Clock, is addressed at 7800 by the I/O line from the Memory board (A54). Address lines A8-A10 produce enable signals for starting addresses as follows:

7A00 for the 9914A GPIA
7C00 for the GPIB Switch Data Buffer
7E00 for the ROM Bank Select Enable

Bank Selector. Bank switching expands the addressing capabilities of the microcomputer. The Bank Selector circuit allows addressing 272K of ROM in seventeen 16K banks. Each ROM IC holds two banks in its 32K bytes of memory. Banks 0, 1, and 16 are located on the Memory board (A54). Banks 2 through 15 are located on this board.

Latch U2044 reads the data bus at address 7E00. Bit D4 selects between the first sixteen ROM banks and the seventeenth ROM bank (located on the Memory board). When high, bit D4 enables U3050 on the Memory board (A54). When low, bit D4 enables U1040 on this board.

When the lower ROM banks are selected, bit D0 selects even and odd banks by driving the most significant address line on each ROM IC. When D0 is low, the lower addresses in each ROM are selected. These are the even bank numbers. When D0 is high, the upper (odd bank) addresses are selected.

Bits D1 through D4 drive decoder U1040. Bit D4 enables the decoder, and bits D1 through D3 provide the chip enable signals for the ROMs. When a bank is selected, it is addressed in the 8000 through BFFF range. If another bank is selected, new data is written to the Bank Selector. Table 7-18 lists the ROM selection data for the lower sixteen banks.

The light-emitting-diodes (LEDs) on U1040's chip enable outputs are diagnostic indicators. When the instrument is placed in a self-diagnostic mode, the LEDs signal results of the tests. See the Maintenance section for further information.

Bank ROMs. The bank ROMs contain most of the firmware. This includes functions such as control programs, measurement routines, and crt messages.

The memory ICs are 27256 32K-by-8 bit erasable programmable ROMs. They each have 15 address lines, 8 data lines, a chip enable line, an output enable line, and a program voltage line. Normally, the ROMs will not be erased or re-programmed.

Table 7-18

ROM Bank Selection Data

Bank	D0	CE0-7	ROM
0	0	0	A54U3060
1	1	0	A54U3060
2	0	1	A56U1010
3	1	1	A56U1010
4	0	2	A56U1020
5	1	2	A56U1020
6	0	3	A56U1025
7	1	3	A56U1025
8	0	4	A56U1035
9	1	4	A56U1035
10	0	5	A56U3015
11	1	5	A56U3015
12	0	6	A56U3020
13	1	6	A56U3020
14	0	7	A56U3030
15	1	7	A56U3030

GPIB Switches. At address 7C00, buffer U2045 writes the rear-panel GPIB switch data onto the data bus. A resistor-capacitor combination decouples each switch line to minimize noise and unwanted pulses picked up on the long circuit board lines to the rear panel.

GPIA. General Purpose Interface Adapter (GPIA) U2050 translates microprocessor commands on the microcomputer bus into appropriate codes and protocol for the GPIB bus. It also decodes data from the GPIB for the microcomputer bus. Interrupts are generated by pulling down on the GPIB SRQ line. The CRT CLK line provides the clock reference. This IC is accessed at address 7A00.

The GPIB Interface board (A30A57) connects the rear-panel IEEE 488 PORT (GPIB connector) to the GPIB board, through the GPIB Extender board (A56A1). The interface board contains two octal transceivers, U1011 and U1012, that transfer GPIB data between the rear-panel connector and the GPIA circuit.

Accessories Interface (Diagram 40)

The Accessories Interface board (A30A76) provides access to the instrument bus, and the external MARKER/VIDEO input and control line. The MARKER/VIDEO input is through a coaxial connector. The other lines are available through the ACCESSORIES connector.

To display an external signal that is applied to the MARKER/VIDEO input, pull the EXT VIDEO SELECT line (pin 1 of the ACCESSORIES connector) low.

The instrument bus is buffered and brought out to the rear panel with the lines named to indicate their relation to the internal bus: ADV for DATA VALID, APOLL for POLL, etc.

Two lines, INT CONT and DATA BUS ENABLE, define the instrument bus/external device interface. An external controller gains control by pulling the INTERNAL CONTROL line low. This disables the internal microcomputer's instrument bus buffers and sets the data direction of buffers U2015 and U2033. In this state, the external controller sends addresses and the DATA VALID and POLL signals to the instrument. It also allows the instrument circuits to send a service request (SR) signal to the external controller. For internal control, the buffers reverse direction.

Data buffer U2038 transfers data to and from the external instrument bus. Data direction depends on whether control is internal or external and on what the address is. The buffer senses the most significant address bit, AB7, so that when in external control, the upper addresses (AB7 high) send data to the instrument and the lower half of the addresses (AB7 low) receive data from the instrument. For internal control, the data direction reverses.

The DATA BUS ENABLE line is asserted low by an external device to enable the data buffer. As long as this line is unasserted, the data buffer is set to its high impedance state and the data direction input has no effect on its output.

Front Panels (Diagram 41)

The Front Panel boards (A38 and A39) act as an interface between the user and the instrument. These circuits translate operator actions on front-panel controls, into data for the microcomputer to read and implement. They output data showing current operating modes to the user via LED's (light emitting diodes) and crt readout.

Output of data is provided by seven shift registers that drive LED's to light various front-panel pushbuttons and indicators to show the instrument operating mode. Operator input information, via pushbuttons or rotary switches, is read by the front-panel CPU. The CPU then outputs the data to the master microprocessor for action. The front-panel CPU scans all push buttons and rotary selectors on the keyboard matrix plus the coder for the FREQUENCY knob looking for changes in the keyboard codes or frequency coder. It then translates

these changes for the master microprocessor for appropriate action. The following is a description of the hardware and a brief description of the software used by the front panel CPU.

Potentiometers. The following controls or adjustments generate analog signals used by other functions of the instrument. These controls are non-programmable.

INTENSITY is an input to the Z-Axis/RF Interface board to control trace brightness.

PEAK/AVERAGE is a digital storage input that causes signals to be either peak detected above or averaged below a displayed cursor line that tracks this control.

MANUAL SCAN sweeps the spectrum or display in manual sweep mode.

POSITION centers the horizontal and vertical deflection on the crt.

LOG/AMPL CAL varies the video signal level prior to the Video Processor board and adjusts 10 MHz IF gain to calibrate the log display.

Output Mode Shift Registers and LEDs. As previously described, LEDs mounted behind a pushbutton or below front-panel labels indicate the mode of operation. Some versions of the spectrum analyzer may not use all indicators; for example, the non-programmable versions do not have a RESET TO LOCAL button.

The LEDs are driven by shift registers (U2010, U2020, U2061, U3060, U5060, U6040, and U6070) that reside at address 74 (H) on the instrument bus. The shift registers that drive the LEDs are reloaded each time a LED changes state. The master microprocessor changes the appropriate bit in the LED code then reloads all registers. The shift register U5060 that drives the GRAT ILLUM LED also controls the voltage regulator U5080, which provides power for the graticule lights.

Processor. The CPU is an 8741 self-contained 8-bit microprocessor with on-chip EPROM and RAM. Refer to Intel UPI Users manual for a complete description of this microprocessor (Intel 8741).

The IC has a self-contained clock and a timer. The clock uses a 6 MHz crystal, Y6030, as the resonator. The timer functions either as a programmable timer or counter.

The CPU has two input/output ports. Port P10-P17 is input only and P20-P27 in an input/output port. Each port is 8-bits wide. In addition, the CPU has an 8-bit data port (D0-D7) called the output buffer, which talks to the master microprocessor. In this application all data is output only with U3030 being a buffer between the CPU and the instrument bus. Information that the CPU wishes to relay to the master microprocessor, is loaded into a latch connected to the output buffer U3030. The master microprocessor accesses the CPU by pulling address F4, out of decoder U2040, low to activate the output buffer and enable U3030 so data is passed onto the instrument bus.

The CPU is reset by the master microprocessor. When DB3 is selected for more than 10 ms (same as writing 08 at address 74) C5021 charges and U5020A output resets the CPU.

Scanning the Keyboard. The front-panel keyboard is arranged in a matrix of 6 rows of 5 columns and 6 rows of 7 columns (see Table 7-19). The RESOLUTION BANDWIDTH, SPAN/DIV, TIME/DIV, MIN RF ATTEN dB, and REFERENCE LEVEL selectors are rotary switches where each contact occupies a position in the keyboard switch matrix. Except for TIME/DIV and MIN RF ATTEN, the rotary switches are independent. The master microprocessor notes the current setting of these selectors by noting which contacts are closed. When a change is made the master microprocessor notes which direction the selector was moved by noting the relative position of the current contact closure with the previous setting. Pull up resistors, within R1030 through R1037, on each column of the row currently being read, will pull that column high if the switch is open. The basic algorithm of scanning is to pull one row at a time down and note which columns have a 1 or 0. Port one, P10-P17 (pins 27-34), read the columns. Part of port two (pins 21-24) are responsible for activating the rows. Basically the process consist of pulling one row at a time down to a logic 0 and then reading all the columns. If a switch contact is open it reads a "1" and if it is closed it reads a "0".

Since there are 16 rows to scan and only 4 pins (P20-P23) available at the number 2 port, the output is multiplexed through U2050 (U2060) and U1060 (U1061). These IC's are open collector output, TTL compatible multiplexers. They decode data out of P20, P21, P22, and P23 (pins 21-24) and their output pulls the appropriate row of keys down. Table 7-19 is a chart showing the switch matrix codes, and which keys correspond to a given address in the matrix code. Note that column 6 contains the MIN RF ATTEN settings, column 7 the SPAN/DIV and RESOLUTION BANDWIDTH settings, column 8 the REFERENCE LEVEL settings, and columns 1 & 2 are devoted entirely to the TIME/DIV selections.

Due to the characteristics of the switch matrix, if two keys, in any row or column are closed, and a third is closed so three corners of a rectangle are established in the key matrix, the CPU will see a phantom closure at the fourth corner. For example; if Y6/X3, Y6/X7 are closed, and then Y3/X7 is closed, the CPU will see a phantom closure at Y2/X3 as it scans the key matrix. To suppress these phantom key closures, diodes have been added in series with the RESOLUTION BANDWIDTH, MIN RF ATTEN, SPAN/DIV, and certain other keys in column 6 and 7 of the key matrix. In addition, an error detection algorithm is used in the CPU to eliminate additional phantom key closures that might occur.

Scanning the FREQUENCY Control Coder. The FREQUENCY control contains a pair of phototransistors that output a gray code through U5020B and U5020C to P27 and P26 (pins 38 and 37) of the CPU. This gray code signifies the direction the control is turned. During a scan cycle, the CPU looks at the status of the FREQUENCY control code and if it detects a change, the CPU performs a shift and exclusive-OR operation which derives the correct code to output over the instrument bus to the master processor to tell it which direction to tune the center frequency.

Outputting the Correct Code. The remaining two bits out of port 2 (P24 and P25) drive the appropriate hardware and initiate an SRQ on the instrument bus. When the SER REQ line is pulled down, the master microprocessor will service either the keyboard or the frequency coder. The front panel CPU (U5030) initiates a SRQ by pulling down P24 or P25. A low out of P24 (pin 35) will initiate a keyboard SRQ. The master microprocessor will now service the request by reading the keyboard data in output buffer U3030. A low out of P25 (pin 36) initiates a FREQUENCY control SRQ and causes the master microprocessor to service the request by reading the frequency code in the output buffer.

A low out of P24 is inverted by U4010E so it clocks the flip-flop U5011B. The resultant low on the Q(bar) output pulls the SER REQ line down. (Refer to the instrument bus POLL sequence described under the master microprocessor description for the service request sequence.) The master microprocessor now raises both the POLL line and AB7. This is gated through U3010A (U6030A) as a low to DB0 on the instrument bus. The master microprocessor reads the bus and sees a low on DB0. This indicates that a keyboard interrupt has occurred and it must read the new keyboard code. The master processor first clears the interrupt by pulling AB7 and then the POLL line low. DB0 now goes high. The master microprocessor now writes a 0 to DB0, the same as it read, and raises the POLL line. This clocks U5011A and resets U5011B which removes the SRQ(bar). The instrument processor now reads the data in the output buffer, U3030, at address F4. The front panel CPU now recognizes that its output buffer has been read and it resets P24 to a 1. It is now ready for another cycle.

A similar process occurs when P25 (pin 36) of the CPU is pulled low by a FREQUENCY coder interrupt. A low on P25 is propagated through U4010E, U5010A, U5010B, and U3010C (U6030C); only this time DB3 is involved in the poll. U4010D and U3010B (U6030B) decode a low on AB7 and high on POLL line to clock U5010A and U5011A.

Software. The algorithm that the CPU follows consists of a main scan routine, which is an endless loop, and four subroutines that can be called. One subroutine runs the on-chip timer that is used to debounce the keys, another reads the frequency knob coder and derives the proper code to output to the master processor, the third subroutine reads the keyboard and stores the address of all keys that were closed, and the fourth subroutine looks at the keycode from the key addresses that were stored, and outputs the key codes and/or frequency code for the master processor. There are also a number of checks and tests that have to be done in each routine in addition to the obvious tasks.

Main Scan Routine. There are two types of scan; the first is made after a reset, the second type consists of the following scans; the keyboard, frequency coder, and the output data. During the first scan, data in the CPU is initialized. The CPU reserves part of its RAM to store and remember all key and frequency knob coder settings. During all scans, the CPU reads the frequency code and each row of keys on the keyboard. It compares what it read to that stored in RAM and if there is a difference, the CPU calls the appropriate subroutine for either the keyboard or the frequency coder knob. After a complete scan, the CPU checks to see if new information needs to be output to the instrument processor. If it does the CPU calls up the output subroutine.

Prior to the first scan, after reset, the CPU puts all 1's (highs) into its keyboard memory. This corresponds to open keys. On the first scan, the CPU will note five apparent closures due to the TIME/DIV, MIN RF ATTEN, SPAN/DIV, RESOLUTION BANDWIDTH, and REFERENCE LEVEL selectors. These closures are noted and output to the master processor. Because the master processor memory knows the position of each selector to close a key, the processor calls these the power-up settings. When a front

panel knob changes position the master processor can determine which direction the knob changed and what it must do to respond to the change. A complete scan, without detecting any key closures takes about 800 us.

Keyboard Check Subroutine. This subroutine is called when the main scan routine detects a change in the keyboard matrix which occurs when a key opens or closes. A key opening usually signifies that an action has been completed, whereas a closure indicates that an operation or action is requested by the user; therefore, the two are treated differently by the CPU.

Because mechanical keys tend to bounce when they open or close, the subroutine must debounce each key change. To debounce, the subroutine calls up the timer subroutine. This sets a number into the internal timer and starts it running. When the timer has timed out, in about a millisecond, the keyboard subroutine again scans the row and compares this scan with the scan before the debounce check. If the scan does not compare, the routine assumes the key change was a bounce or fluke, and it returns to the main scan routine. If it does compare, the routine then recognizes that a key state has changed. It then checks to see if this is the first scan that looked for a key change after it has outputted previous information to the master processor. If it is the first pass then the routine causes the CPU to re-scan the full keyboard matrix to ensure that there is not a phantom key closure. If this is the second or subsequent pass and an actual key change has occured, the routine then notes if the key change was an opening or closure. If it was an opening the CPU memory is updated to the fact that the key is open. If a closure has occurred, the routine will then check the column that has the closure and output a new key address onto the output stack. This address consists of the key's row and column location. After outputting the address, the subroutine returns to scanning the remainder of the keyboard matrix.

Frequency Coder Subroutine Check. This subroutine is called when the main scan routine detects a change in the frequency coder switch. Like the keyboard subroutine, this routine also debounces the frequency coder switch after every change to ensure that the switch code has changed. If a real change is noted, the routine proceeds to determine the direction of the change. The frequency knob outputs a two-bit code with only one bit at a time changing as the control is rotated. The direction the knob is rotated is determined by the property of a gray code, generated by an exclusive-OR logical operation within the CPU. The previous state of one bit is compared with the current state of the other bit. Down (counterclockwise rotation) yields unequal inputs, while up (clockwise rotation) yields the opposite. The bit that indicates direction is inserted as the MSB for the frequency coder byte. This byte is then loaded into the output stack. The subroutine then returns to the main scan routine.

Output Subroutine. After each scan, the CPU checks its output register to see if any information needs to be output. If it needs to be output, the output subroutine is called up; if not, another scan is started. The output subroutine checks a number of things before it outputs any information to the output register. It first determines if the CPU is on its first or initial scan after a reset. The first scan will contain more than one closure. All of these closures must be output before it continues. On all scans that follow, the routine looks for more than one closure by checking the number of entries into the output stack. If more than one closure has been entered, the output routine aborts. This eliminates outputting phantom key closures.

The routine is now ready to output information. It pulls a key address from the output stack and looks up the code from a look-up table in ROM. This key code is loaded into the data port or output buffer. The appropriate port P24 or P25 (pins 35 & 36) is pulled low. The routine continuously reads the frequency coder and updates its memory while it is waiting for the master processor to read the data in the output buffer. Once the data has been read, P24 or P25 goes high and the subroutine starts to check the output stack for more key closures. When the output stack is empty, the first scan flag is rescinded and the CPU returns to its main scanning routine.

Table 7-19
FRONT PANEL SWITCH MATRIX CODE/FUNCTION TABLE

ROW	COL	HEX CODE	MAIN FUNCTION	<SHIFT> FUNCTION	DATA ENTRY
X1	Y1	00	20 μs TIME/DIV		
X1	Y2	01	50 μs TIME/DIV		
X1	Y3	02	0.1 ms TIME/DIV		
X1	Y4	03	0.2 ms TIME/DIV		
X1	Y5	04	0.5 ms TIME/DIV		
X1	Y6	05	1 ms TIME/DIV		
X1	Y7	06	2 ms TIME/DIV		
X1	Y8	07	5 ms TIME/DIV		
X1	Y9	08	10 ms TIME/DIV		
X1	Y10	09	20 ms TIME/DIV		
X2	Y1	0A	50 ms TIME/DIV		
X2	Y2	0B	0.1 s TIME/DIV		
X2	Y3	0C	0.2 s TIME/DIV		
X2	Y4	0D	0.5 s TIME/DIV		
X2	Y5	0E	1 s TIME/DIV		
X2	Y6	0F	2 s TIME/DIV		
X2	Y7	10	5 s TIME/DIV		
X2	Y8	11	AUTO		
X2	Y9	12	MNL		
X2	Y10	13	EXT		
X3	Y1	14	EXT TRIG		
X3	Y2	15	SINGLE SWP		
X3	Y3	20	SAVE A		
X3	Y4	17	2 dB/DIV	dB/Hz	
X3	Y5	16	B-SAVE A		
X3	Y6	19	10 dB/DIV	dB/DIV	
X3	Y7	1A	START/STOP	MKR START/STOP	Hz dB
X3	Y8	2F	MAX SPAN		
X3	Y9	1C	– STEP	STEP SIZE	
X3	Y10	1D	FINE		
X3	Y11	60	FIND PEAK↑		
X3	Y12	61	1		
X3	Y13	62	5		
X3	Y14	63	9		
X3	Y15	64	BANDWIDTH	dB BW	
X3	Y16	65	FIND PEAK MAX	FIND PK & CENT	
X4	Y1	1E	INT TRIG		
X4	Y2	1F	FREE RUN		
X4	Y3	22	NARROW		
X4	Y4	21	LIN	MKR–>REF LVL	
X4	Y5	18	VIEW B		
X4	Y6	23	WIDE		
X4	Y7	2A	ZERO SPAN		
X4	Y8	25	AUTO RES		
X4	Y9	26	+ STEP		
X4	Y10	1B	MIN NOISE/DIST		
X4	Y11	66	FIND PEAK <–	xdB<–	
X4	Y12	67	2	(Plotter type)	
X4	Y13	68	6		

Table 7-19 (Continued)
FRONT PANEL SWITCH MATRIX CODE/FUNCTION TABLE

ROW	COL	HEX CODE	MAIN FUNCTION	<SHIFT> FUNCTION	DATA ENTRY
X4	Y14	69	0	(Diagnostic menu)	
X4	Y15	6A	SIGNAL TRACK		
X4	Y16		Not used		
X5	Y1	28	Not used		
X5	Y2	29	GRAT ILLUM	RESET	
X5	Y3	2B	MAX HOLD	(Display errors)	
X5	Y4	30	SPAN/DIV	BAND▽	MHz/+dBx
X5	Y5	2C	REF LEVEL	REF LEVEL UNITS	kHz/−dBx
X5	Y6	24	VIEW A		
X5	Y7	2D	SHIFT	(Shift cancel)	
X5	Y8	27	FREQUENCY	BANDΔ	GHz
X5	Y9	2E	TUNE CF/MKR	MKR OFF	
X5	Y10	31	(75Ω in Opt. 07)		
X5	Y11	6C	FIND PEAK−>	xdB−>	
X5	Y12	6D	3	(Plotter B-A offset entry)	
X5	Y13	6E	7	(Disable corrections)	
X5	Y14	6F	.	(Display errors)	
X5	Y15	70	RECALL DISPLAY	STORE DISPLAY	
			MIN RF ATTEN dB		
X6	Y1	32	0		
X6	Y2	33	10		
X6	Y3	34	20		
X6	Y4	35	30		
X6	Y5	36	40		
X6	Y6	37	50		
X6	Y7	38	60		
X6	Y8	39	RECALL SETTINGS	STORE SETTINGS	
X6	Y9	3A	ΔF	STEP ENTRY	
X6	Y10	3B	COUNT (Option 05)	CNT RES (Option 05)	
X6	Y11	72	FIND PEAK↓		
X6	Y12	73	4		
X6	Y13	74	8		
X6	Y14	75	BACK SP		
X6	Y15	76	PULSE STRETCHER	IDENT	
X6	Y16	77	THRESHOLD	MENU	
X7	Y1	3C	FREQUENCY SPAN/DIV		
X7	Y2	3D	FREQUENCY SPAN/DIV		
X7	Y3	3E	FREQUENCY SPAN/DIV		
X7	Y4	3F	FREQUENCY SPAN/DIV		

Table 7-19 (Continued)
FRONT PANEL SWITCH MATRIX CODE/FUNCTION TABLE

ROW	COL	HEX CODE	MAIN FUNCTION	<SHIFT> FUNCTION	DATA ENTRY
X7	Y5	40	RESOLUTION BANDWIDTH		
X7	Y6	41	RESOLUTION BANDWIDTH		
X7	Y7	42	RESOLUTION BANDWIDTH		
X7	Y8	43	RESOLUTION BANDWIDTH		
X7	Y9	4A	RESET TO LOCAL	SRQ	
X7	Y10	45	LINE		
X7	Y11	78	READOUT	CAL	
X7	Y12	79	BASELINE CLIP		
X7	Y13	7A	ΔMKR	MKR–>CF	
X7	Y14	7B	1<–MKR–>2		
X7	Y15	7C	RUN/STOP (Option 05)	MAC MENU (Option 05)	
X7	Y16	7D	PLOT	(Select plotter)	
X8	Y1	46	REFERENCE LEVEL		
X8	Y2	47	REFERENCE LEVEL		
X8	Y3	48	REFERENCE LEVEL		
X8	Y4	49	REFERENCE LEVEL		

POWER SUPPLY (Diagram 9)

The Main Power Supply furnishes all the regulated voltages for the spectrum analyzer, except the crt high-voltage supply. The high-efficiency design of the Main Power Supply reduces total weight and conserves energy. The power supply circuits are divided into the primary circuits and the secondary and fan drive circuits.

Primary Circuits (Diagram 42)

The power supply primary circuits consist of the following: the line input circuit, which rectifies and filters the incoming line voltage; and the inverter, which drives the primary of the power transformer.

Line Input Circuits

Power is applied through line filter FL301, line Fuse F301, and through FL302 (for additional normal mode/common mode EMI filtering) to POWER switch S300. The power is then sent through line selector connector J1091. The line filter prevents power-line interference from entering the power supply, and it also prevents internally-generated signals from radiating out the power cord.

Line selector switch S302 allows instrument operation from either a 15 V nominal or 230 V nominal line voltage source. With S302 is in the 115 V position, pins 1 and 2 of P1091 are connected to the input power, and rectifiers CR3096 and CR4094 operate in conjunction with energy storage filter capacitors C6101 and C6111 as a full-wave doubler; thus, the voltage across the two capacitors is the peak-to-peak value of the line voltage. With S302 in the 230 V position, pins 2 and 3 of P1091 are connected to the input power and CR3096, CR4095, CR3098, and CR4094 operate as a bridge rectifier. As a result, the output voltage applied to the inverter is about the same for 115 V or 230 V operation.

WARNING

Because C6011 and C6101 discharge very slowly, hazardous potentials exist within the power supply for several minutes after the POWER switch is turned off. A relaxation oscillator formed by C5113, R5111, and DS5112, indicates the presence of voltages in the circuit until the potential across the filter capacitors is below 80 V.

Thermistors RT2093 and RT2097 limit current surge at turn on. After the instrument warms up, the current demand drops. The increase in temperature decreases the resistance value of the thermistors so they have minimum affect on the circuit.

Thermal cutout switch S2103 opens if the interior of the instrument reaches 103°C to prevent overheating in case the cooling fan fails.

E1094 and E2095 are surge voltage protectors. When the line selector switch is in the 115 V position, only E1094 is connected across the line input. If a peak voltage surge in excess of 230 V occurs across the input, or if the instrument is accidentally connected to a 230 V source, E1094 will break down and demand enough current to open the line fuse. When the instrument is operated with the line selector at 230V, E1094 and E2095 operate in series to protect the input against line surges of approximately 460 V peak.

The voltage for the line trigger is taken across CR3096. This 48 Hz to 440 Hz voltage drives optical isolator U5043. The pulsating 5 V output is ac coupled, then sent both to the Sweep circuit to provide instrument triggering at the line frequencies and to the Z-Axis board for the Power-Fail Detector circuit.

Inverter Circuit

The inverter consists of a multivibrator that produces a rectangular shaped signal to drive the ramp generator and the inverter logic circuits. The ramp generator produces a low-level sawtooth ramp that is applied to the primary regulator circuit. The inverter logic circuits control the duty cycle of the inverter driver and the inverter output stage. The primary regulator circuit compares the +17 V supply output with a reference voltage, then gates the inverter logic circuits off and on to control the inverter duty cycle and the effective primary voltage. The inverter driver stage amplifies the signal from the inverter logic circuit and drives the output stage. The output stage consists of two power switching transistors that drive the primary of main power transformer T4071. The primary overcurrent sense and soft start circuits add protection.

Multivibrator. U6059, a low-power 555 timer, is a multivibrator that operates at approximately 66 kHz and 90% duty cycle. Oscillator frequency is adjusted by R6061. The rectangular-shaped output signal is applied through R6052 to the primary of T6044 in the ramp generator and also directly to U6053, U6063A, U6063B, and U6069.

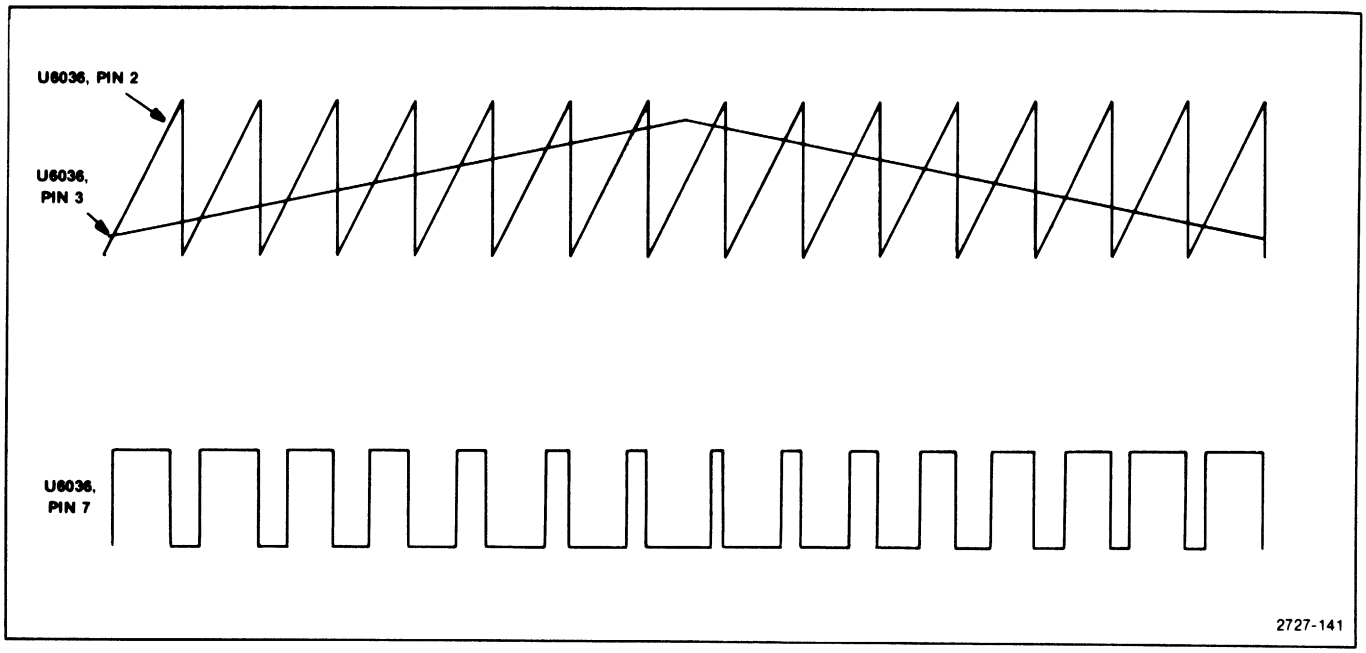


Figure 7-30. Primary regulator input and output waveforms.

Ramp Generator. The ramp generator circuit is a gated sawtooth generator that consists of T6044, Q5023, Q6034, Q5032, and related components. The negative excursion of the rectangular shaped signal from U6059 is coupled across T6044 to force Q6034 into conduction. This forward-biases Q5032. Its collector moves toward +17 V to charge C5038 to this value. Q6034 loses drive (since the pulse coupled across T6044 has died away) and the two transistors cut off. Q5023 acts as a constant-current drain to linearly discharge C5038. This signal is coupled across divider R5036/R6032, then applied through C6039 to the input of comparator U6036, which is part of the primary regulator.

Primary Regulator. The primary regulator circuit consists of comparator U6036 and U6046, photocoupler U6043, and related components. The circuit varies the duty cycle of the driving signal for the inverter. The +17 V is divided by R6038 and R6037 to approximately +4.8V and applied to the inverting input of U6036. The +5 V reference is applied through R6022 to the noninverting input of U6036, where it is combined with the ramp signal from the ramp generator stage. The noninverting input receives a sawtooth signal of approximately 500 mV peak-to-peak superimposed on a +5 V dc level. This is compared with the +4.8 V on the other input, so the comparator switches with each sawtooth cycle. Note in Figure 7-30 that as the level at pin 3 (which corresponds to the +17 V supply variations) rises and falls, the duty cycle of the output waveform varies accordingly.

The output signal of U6036 is applied to optical isolator U6043, which drives the input of U6069.

Inverter Logic. This stage consists of steering flip-flop U6063B and dual quad input NAND gate U6069. The flip-flop is connected so it toggles to enable first one gate then the other. The square-wave output from the multivibrator drives the clock input of U6063B. The signal also enables each gate to ready it for the other signals that arrive later. The output state of U6063B determines whether the upper or lower section of U6069 will be ready for the enabling signal.

Assume that the Q output of U6063B is holding pin 2 of U6069 high. This means that the complement output of the latch is holding the opposite side of the gated pair disabled. When the output of U6043 moves high, U6043 controls the duty cycle of the inverter, the upper section of U6069 produces a low state. This causes current to flow through half the primary and Q6078 only. On the opposite cycle of the multivibrator signal, the latch is reset, so the lower half of U6069 is enabled and Q6077 is now in the conduction path.

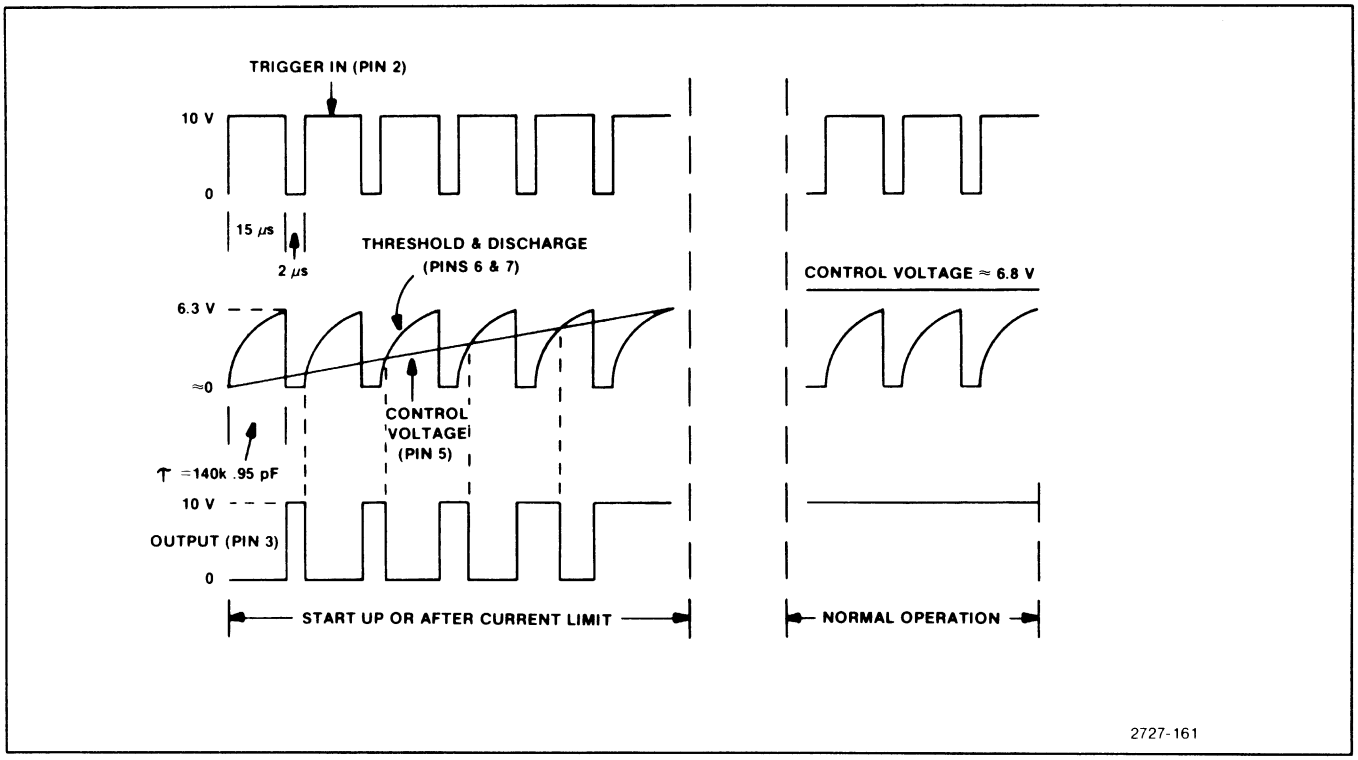


Figure 7-31. Timing waveforms for soft-start circuit.

Inverter Driver. The inverter driver consists of transistors Q6077 and Q6078, transformer T6081, and related components. This is a push- pull amplifier with diode protection in the collector circuits to prevent damage from voltage transients during operation. The drive signal is induced into the two secondary windings of T6081 and coupled to the output stage.

Output Stage. This circuit consists of transistors Q2071 and Q2061, series LC tank L1081/C1063, and transformer T4071. The output transistors are connected in a half-bridge configuration. The two transistors drive the series tank, which acts as an energy storage element and an averaging circuit. Output transformer T4071 is driven by the tank circuit, and it, in turn, drives the secondary circuits.

Primary regulation, as discussed previously, occurs when the duty cycle of the inverter driver main switching transistors is varied. Maximum duty cycle occurs at low input line (90 V) and fully loaded output. At maximum duty cycle, both transistors are off for only 10% of the period, or 1.5 μs. This short interval allows any stored base charge to deplete, so there is no chance both transistors will conduct at the same time. Minimum duty cycle occurs at high input line (132 V) and minimum loaded output. At minimum duty cycle, each transistor is off for approximately 6 μs, or 40% of the total period.

Soft-Start and Primary Over-Current Circuits. The soft-start circuit consists of U6053 and associated components. Soft-start gradually increases the switching transistor's duty cycle at turn-on or after over-current shutdown to prevent excessive transistor current due to charging output capacitors. Refer to Figure 7-31 for timing waveforms.

The primary over-current circuit protects against secondary shorts that could destroy the switching transistors. T2080 senses the collector current in Q2071 and creates a voltage on pin 5 of U6046B. If the bias on pin 5 surpasses the 2.5 V reference on pin 6, at approximately 6 A through Q2071, the output of U6046B sets U6063A. U6063A is a D-type flip-flop used as a timer to shut down the inverter logic for approximately 1 s and to reset the soft-start circuit.

Secondary & Fan Drive Circuits (Diagram 43)

The secondary circuits include the rectifier-filter circuit, which rectifies and filters the secondary voltages; the voltage reference circuit, which furnishes a stable and precise reference for the regulators; and the regulator circuits, which control the voltage and current for the supplies that require precise regulation.

The Fan Driver board (A30A1) contains the Fan Driver circuit, which furnishes the appropriate drive current for the fan motor. It also contains the Over-Voltage Protection circuit, which shuts down the +5 V supply in case of over-voltage.

Rectifier-Filter Circuits

Transformer T4071 has three secondary windings. The first furnishes current to the +300 V and +100 V supplies; the second furnishes current to the −7 V, +7 V, and +9 V supplies; and the third furnishes current to the +17 V and −17 V supplies. The linear regulated supplies (+5 V reference, +5 V, −5 V, +15 V, and −15 V) derive their current from the rectifier-filter circuits.

The ac voltage from pins 7 and 8 of T4071 is applied to a bridge rectifier composed of CR3053, CR3056, CR3055, and CR3054. The output of this rectifier is filtered, then applied to the remainder of the instrument as the +100 V supply.

The +300 V supply is derived by stacking a 2X multiplier on the +100 V supply. CR3052, CR1042, CR1034, CR1022 and associated capacitors, compose this circuit.

The ac voltage from pins 9 and 10 supply current to full-wave rectifier CR4061/CR4062. The output is filtered and sent to the rest of the instrument as the +9 V supply. Two other taps off the same winding (pins 11 and 12) supply current to the bridge rectifier that consists of CR4063, CR4057, CR4053, and CR4065. The output divides across filter capacitors C3051 and C4051 to become the +7 V and −7 V supplies. The +7 V supply is only used on the Main Power Supply board; the −7 V supply is used by other circuits in the instrument.

The third winding of T4071 (pins 13, 14, and 15) furnishes current to full-wave bridge rectifier CR5052, CR5062, CR5065, and CR5055. The output is divided to become the +17 V and −17V supplies. The −17 V supply is used only on the Main Power Supply board; the +17 V supply is used both on the Main Power Supply board and elsewhere in the instrument.

+5 V Voltage Reference Supply

The +17 V is divided down by a voltage divider to Zener diode VR6026. The 6.2 V from VR6026 is divided across R6029, R6028, and R6023. CR5031 provides a regulated source of bias to VR6026 after +15 V comes up. The +5 V REF adjustment, R6028, is set by monitoring the +15 V supply and setting it for a precise +15.00 V.

Regulator Circuits

The +15 V, −15 V, +5 V, and −5 V are regulated. Since all four regulators are basically the same, only the +5 V regulator is described. Significant differences are discussed following this description.

U2037A, the voltage regulator part of the circuit, compares the +5 V[REF and +5 V SENSE voltages, amplifies the difference, and applies the change to driver transistor Q2023. The change is amplified by this stage and applied to the base of series-pass transistor Q2024 to change its conduction and correct for the original change to the +5 V. The +5 V sense samples the +5 V at a distribution point on the Mother board. This signal compensates for voltage (IR) losses to that point.

U2037B is the current limiter portion of the regulator. The amplifier detects the voltage differential across the current sensing resistor R2017, which is in series with the output load. When the overload threshold is reached, as set by R2017, R2039, R3032, and R3031. U2037B removes bias current from driver transistor Q2023 and Q2024. The negative bias on R3031 allows the limiter to remain active under short circuit conditions.

The +15 V regulator is identical to the +5 V regulator, except that the current limiter, U2037D supplies additional positive bias for Q2031 when it is not active. The −15 V regulator is virtually identical to the +5 V regulator. The −5 V regulator differs from the others in that a driver stage is not required, so the preamplifiers drive series-pass transistor Q5013 directly.

+5 V Over-Voltage Protection Circuit

Zener diode VR1015 and SCR Q1010 form the over-voltage protection circuit. If the +5 V supply exceeds +6 V, the potential on the gate of Q1010 biases it into conduction. This forces the +5 V supply to ground potential; it remains at ground potential until the mains power is turned off and turned on again.

Fan Drive Circuit

The fan drive circuit provides a temperature- controlled current drive to the fan motor. The circuit produces a three-phase drive current of approximately 240 Hz operating frequency. The actual drive circuit operates as a ring counter.

Transistors Q1038 and Q1044 form a voltage regulator controlled by thermistor RT2045. The value of RT2045 varies inversely with the internal temperature of the analyzer. The thermistor and resistor R2042 fix the turn-on voltage at the emitter of Q1044 at approximately −13 V. The voltage goes more positive as the analyzer warms up. In Option 30 and 31 (rackmounted) instruments, Zener diode VR2038 is connected with jumper P2043 when the rackmount fan is used to prevent the output voltage from going below approximately 9 V.

The ring counter consists of three stages. Because of circuit imbalances, when the analyzer is first powered up one of the stages begins to conduct before the others. The stages consist of Q1025 and Q1020, with R1031/C1032 and R1027/C1018 as the frequency-determining components; Q2025 and Q1018, with R1033/C1033 and R2019/C1019 as the frequency-determining components; and Q2030 and Q2020, with R2014/C2012 and R2016/C2018 as the frequency-determining components.

Assume that the stage with Q1025 and Q1020 begins to conduct first. The collector voltage of Q1025 is near −17 V, which fixes that point as the most negative in a ring consisting of R1032, R1029, R1028, R2036, R2034, and R1036. Since the emitter voltage of the three control transistors (Q1020, Q1018, and Q2020) is the same, the voltage division around the resistive ring is such that Q1018 and Q2020 remain cut off. When the capacitive charge that holds Q1020 in conduction bleeds off, the transistor cuts off and the next stage can begin to conduct. Operation of the other two stages is prevented until the RC combination discharges. The fan motor inductance works in conjunction with the RC components to regulate the switching of the stages.

This ring-counter action builds up slowly until the circuit produces a three-phase drive signal of approximately 240 Hz. The inductance of the motor coils round off the otherwise sharp corners of the drive signal; so, the current waveform at P2020 pins 1, 2, and 3 looks similar to the output of a half-wave rectifier. The fan drive signals are phased approximately 120 degrees apart.

OPTIONS

This section describes the options available at this time for the spectrum analyzer. Changes in specifications, if any, are described in this section. Contact your local Tektronix Field Office or representative for additional information and ordering instructions (unless otherwise indicated).

Options are usually factory installed; however, field kits are available for some options. Contact your local Tektronix Field Office or representative for information on field kits and their installation.

Options A1, A2, A3, A4, and A5 (Power Cord Options)

There are five international power cord options offered for the spectrum analyzer. The physical descriptions of the cord plugs are illustrated in Figure 8-1. For ordering purposes, refer to the Replaceable Mechanical Parts list in the Service Manual, Volume 2, for the Tektronix Part Number.

Option B1 (Service Manuals)

Option B1 includes a set of service manuals with the instrument.

Options M1, M2, and M3 (Extended Service and Warranty Options)

There are three extended service and warranty options offered for the spectrum analyzer (see Table 8-1) that go beyond the basic one-year coverage. Contact our local Tektronix Field Office or representative for additional information to satisfy your specific requirements.

Table 8-1

EXTENDED SERVICE AND WARRANTY OPTIONS

Option	Description
M1	Two routine calibrations to published specifications; one each in years two and three of warranty coverage, plus two years remedial service
M2	Four years remedial service
M3	Four routine calibrations to published specifications; one each in years two, three, four, and five of product ownership, plus four years of remedial service

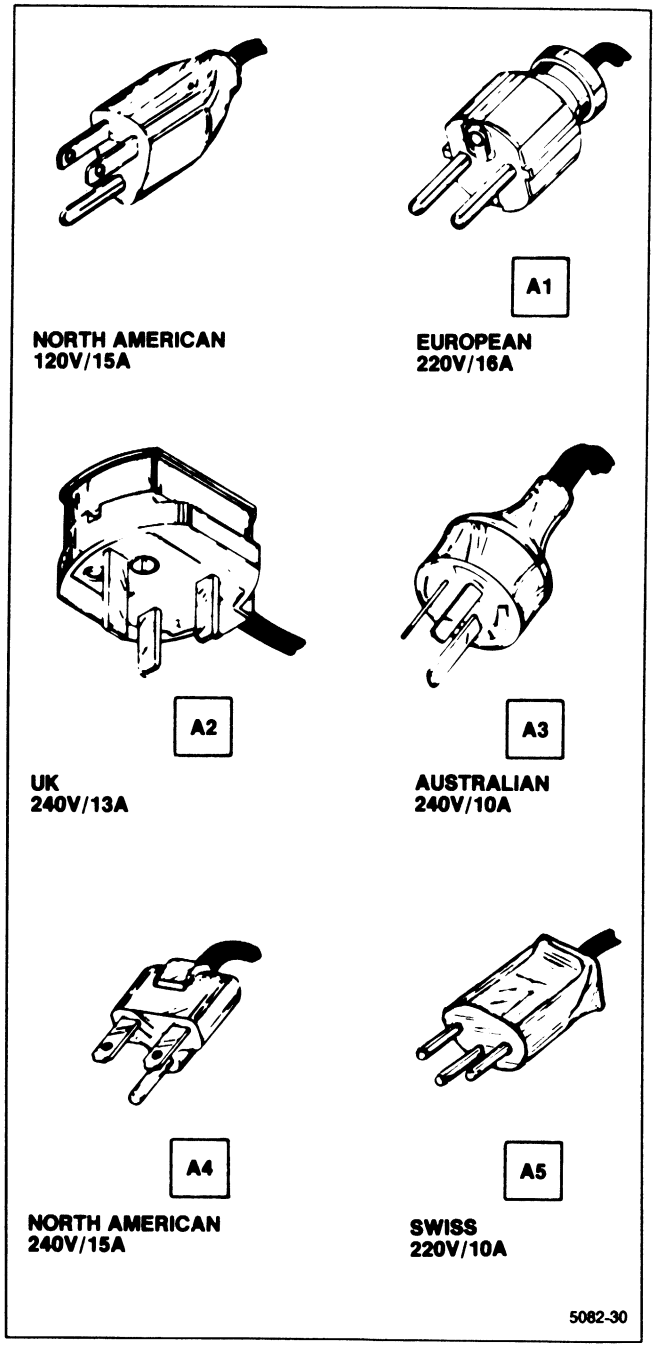


Figure 8-1. International power cord options for the spectrum analyzer.

Option 05 (Counter and Macros)

Option 05 adds a frequency counter with an accurate internal reference and an external reference input, as well as the capability to have eight user-designed programs stored in memory.

Tables 8-2 and 8-3 list additional instrument specification changes and additions when Option 05 is installed.

Table 8-2
Frequency Related Characteristics for Option 05

Characteristic	Performance Requirement	Supplemental Information
Signal Counter		
Accuracy (after 30 minute warmup)	±[(Counter frequency × reference frequency error) + 12 Hz +1 count	Count at either center or marker.
Sensitivity	Signal level, at center screen or at marker, must be 20 dB or more above the average noise level and within 60 dB of the reference level.	
Readout Resolution		1 Hz to 100 MHz; selectable with COUNT RESOLUTION.
Reference Frequency Error		$\leqslant 1\times10^{-9}$ per day
Aging Rate First six months		$\leqslant 1\times10^{-7}$ in first six months
After the first six months		$\leqslant 1\times10^{-7}$ per year
Accuracy during warmup at 25°C and 30 minutes after power on		Within 5×10^{-8} of the frequency after 24 hours
Temperature sensitivity		Within 2×10^{-8} over the instrument operating range of 0°C to +55°C (referenced to +25°C)

Table 8-3
Input Characteristics for Option 05

Characteristic	Performance Requirement	Supplemental Information
Center Frequency and Marker Initial Accuracy With SPAN/DIV >200 kHz (1st LO unlocked)	±[20%D + (CF × Ref) + 15 kHz Where: D = SPAN/DIV or RESOLUTION BANDWIDTH, whichever is greater CF = Center Frequency Ref = Reference Frequency Error	Allow a settling time of one second for each GHz change in CF.
With SPAN/DIV ≤200 kHz (1st LO locked)	±[(20%D) + (CF × Ref) + 15 Hz Where: D = SPAN/DIV or RESOLUTION BANDWIDTH, whichever is greater CF = Center Frequency Ref = Reference Frequency Error	
Calibrator (CAL OUT) Frequency		100 MHz (phase locked to reference oscillator)
EXTERNAL REFERENCE		Rear-panel bnc input.
Frequency	1, 2, 5, or 10 MHz ±5 ppm	
Power	−15 dBm to +15 dBm	
Waveshape		Sinewave, ECL, or TTL. (Allowable duty cycle symmetry is 40% to 60%)
Input Impedance ac		50Ω
dc		500Ω

Option 07 (75Ω Input)

Option 07 provides a 75Ω input in addition to the standard 50Ω input.

Table 8-4 lists the changes and additions to the standard instrument electrical characteristics. These characteristics apply to the 75Ω Input.

Table 8-4

OPTION 07 ALTERNATE SPECIFICATIONS

Characteristic	Performance Requirement	Supplemental Information
INPUT Input Impedance Return Loss 5 MHz–800 MHz		75Ω 17 dB (1.35:1 VSWR)
800 MHz–1000 MHz		13 dB (1.6:1 VSWR) with ⩾10 dB attenuation
Maximum Input Level With 0 dB Attenuation		 +78 dBmV
With 20 dB or More Attenuation		+78 dBmV, 100 V_{dc} maximum (dc + peak)
FREQUENCY Center Frequency Operating Range		 0–1000 MHz
Resolution Bandwidth	Within 20% of 300 kHz bandwidth (6 dB down)	300 kHz resolution filter replaces the 100 kHz filter.
Frequency Response 5 MHz–1000 MHz Coaxial Input	±2.0 dB about the midpoint between two extremes	Frequency response is measured with ⩾10 dB RF attenuation. The response figure includes the effects of: • input vswr • gain variations Variations in display flatness contribute about 1 dB to the response figure.
1 MHz–5 MHz		Typically <3 dB down from the 5 MHz response
AMPLITUDE Reference Level Range (Full Screen, Top of Graticule		−68 dBmV to +79 dBmV +89 dBmV is achievable in minimum noise mode

Table 8-4 (Continued)

OPTION 07 ALTERNATE SPECIFICATIONS

Characteristic	Performance Requirement	Supplemental Information
SENSITIVITY Equivalent Input Noise Sensitivity 5 MHz to 1000 MHz 75Ω INPUT 30 Hz	−81 dBmV	Measured with: • 0 dB attenuation (Min Atten 0 dB) • Narrow Video Filter • 2 dB/Div Log mode • Digital Storage on • Max Hold off • Peak/Average in Average • 1 sec Time/Div • Zero Span • Input terminated in 75Ω (terminated in 50Ω for 50Ω Input)
100 Hz	−76 dBmV	
1 kHz	−66 dBmV	
10 kHz	−56 dBmV	
300 kHz	−41 dBmV	
1 MHz	−36 dBmV	
50Ω RF INPUT 300 kHz	−90 dBm	
OUTPUT Calibrator Output (CAL OUT) Level	+20 dBmV ±0.5 dB	100 MHz comb of markers provide amplitude calibration at 100 MHz.
Impedance		75Ω nominal

Option 30

This is a 19-inch wide rackmount version of the 2753P.

Option 31

This is a 19-inch wide rackmount version of the 2753P with semi-rigid cabling to provide access to all connectors previously on the front panel at the rear of the instrument. Table 8-5 lists the changes from the standard spectrum analyzer.

Table 8-5

OPTION 31 ALTERNATE SPECIFICATIONS

Characteristic	Performance Requirement	Supplemental Information
FREQUENCY Residual FM		Degrades according to rack frame, typically by a factor of two
AMPLITUDE Frequency Response		Typically 1.5 dB more variation
Residual Spurious Responses		−90 dBm or less
Sensitivity 10 kHz–1.8 GHz	−85 dBm	Equivalent maximum input noise for the 100 kHz resolution bandwidth

Option 39 (Silver Batteries)

Option 39 provides silver batteries for the instrument's battery-powered memory. The battery life at +55°C is 1–2 years and 2–5 years at +25°C. We recommend removing the silver batteries during long-term storage.

Option 42 (110 MHz IF Output)

This option provides a 110 MHz IF output with bandwidth greater than 5 MHz for broadband, swept receiver applications. Table 8-6 lists the changes from the standard instrument.

Option 45 (MATECO)

This option provides the spectrum analyzer with the software/firmware necessary to meet Modular Automated Test Equipment Compatibility Options (MATECO). A MATECO Programmers Manual is included as an accessory with this option.

Option 52 (North American 220V)

Option 52 provides a North American 220 V configuration with the standard power cord. The fuses are replaced with 2A slow blow.

Table 8-6

OPTION 42 ALTERNATE SPECIFICATIONS

Characteristic	Performance Requirement	Supplemental Information
FREQUENCY		
Center Frequency	108.5 MHz to 111.5 MHz	
3 dB Bandwidth	>5 MHz	
Bandpass Ripple	≤0.5 dB	
Symmetry about 110 MHz	±1.0 MHz	
POWER		
Power Out With −30 dB Input and Signal at Full Screen		Nominal output impedance is 50 Ω 1 dB compression of output ≥0 dBm, in Minimum Distortion Mode only.